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Submodule Topologies and PWM Techniques Applied in Modular Multilevel Converters: Review and Analysis

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Abstract. Nowadays electrical energy presents itself as the most promising solution to satisfy the energy needs of smart cities. For electrical energy to be managed efficiently and sustainably, the use of power electronic converters is essential. The evolution of semiconductors, in terms of blocking voltages, conduted current and switching frequencies, led to the emergence of new topologies for more robust and compact power electronics converters with high-frequency galvanic isolation. However, for high and medium voltage applications, such as electric railways, wind turbines, solar photovoltaic, or energy distribution systems, the semiconductor blocking voltages are still below the values in demand. In order to solve this problem, modular multilevel converters (MMC) has been implemented, requiring more sophisticated control algorithms and complex pulse width modulation (PWM) techniques, such as space vector modulation.
In this paper, different topologies to be integrated into an MMC are presented, as well as PWM techniques for MMC, making a comparative analysis based on computer simulations of different PWM techniques developed in PSIM software. An MMC consisting of 4 full-bridge DC-AC power converters connected in series was considered as the study basis for the analysis of the PWM techniques.

Keywords: Level-shift PWM, Hybrid PWM, Modular multilevel converter, Phase-shift PWM, Phase disposition PWM, Pulse width modulation techniques.

Nomenclature

v_{outx}	Instantaneous output voltage of the power submodule number x of the MMC.
v_{out}	Instantaneous voltage at the MMC output.
v_{load}	Instantaneous voltage on the load connected to the MMC.
v_{m_x}	Modulator waveform x.
v_{c_x}	Carrier waveform x.

1 Introduction

Electricity is an essential asset for humanity, having a strong impact on the economic development of nations, on increasing the quality of life, and on sustainability. With the increase in population and the improvement in the quality of life, there is an incessant need for the availability of electricity, which makes it irreconcilable with existing energy sources [1]. Smart cities appear as an innovative concept in response to current needs, allowing the integration of renewable energy sources, energy storage locations, as well as the interface with a fully electrified transport network, as is the case with the rail system. That said, the importance of developing power electronics solutions that allow the gradual integration of new concepts and functionalities in smart cities becomes evident.

The topologies of two and three-level power electronics converters, similar to the half-bridge [2], full-bridge [2], or the basic cell structure of the neutral point clamping (NPC) [3], the T-type NPC (TNPC) [3], or the flying capacitor multilevel converter (FCMC) [4], are presented as the most used power electronics solutions in the most diverse applications. Its simple structure, with low voltages and power (up to 1 MVA), present interesting characteristics for various industrial applications, e.g., for driving motors, for interfacing renewable energy sources with the power grid, for charging of electric vehicles, among others [5]. However, for high/medium voltage or high power applications, such as large solar photovoltaic or wind turbine parks, and electric railway systems, these conventional solutions are no longer viable.

Analyzing the integration of high/medium voltage semiconductors (some kV) in conventional topologies, it is expected to have low switching frequencies. These factors are reflected in the high harmonic contents induced around the low switching frequency. In order to mitigate this problem, bulky passive filters are necessary, which increases the costs, as well as the losses of the converter. Additionally, in the conventional topologies, the DC-link voltage is applied to the converter output at high frequencies. Adopting these topologies to very high voltage applications, it is expected that the output voltage variations will be more accentuated, which would cause greater stress not only at the level of the semiconductors but also at the level of the galvanic isolation of any system connected to these terminals [6].

Modular multilevel converter (MMC) solution will allow significant mitigation of the aforementioned problems. MMC solutions are made up of different submodules connected in series and allows lower DC-link voltages. Additionally, it is possible to obtain different voltage levels depending on the number of submodules in the MMC. In this way, it is possible to obtain better sizing in terms of semiconductors and passive components. Nevertheless, and taking advantage of the concept of modularity, it is possible to easily adapt the solution to the voltage and power levels required by the final application. Barros et al. present in [7] different configurations for the MMC. Other MMC configurations are also presented in [8] and in [9].

Despite its applicability in high and medium voltage applications, the control of a modular system like MMC presents some complexity. In the literature, it is possible to find several scientific review papers that list the different pulse width modulation (PWM) techniques for MMC. However, the gap lies in comparing the performance of

these different PWM techniques for MMC. The lack of this analysis makes it difficult to choose the best PWM technique to be implemented.

The purpose of this paper is to aid the implementation of MMC solution, presenting a comparative analysis for different PWM techniques for the MMC. In this sense, this paper is structured as follows: in Section 1, an introduction to the research topic is made, presenting some of the drawbacks of the conventional power converters; Section 2 presents the MMC concept, some of the applications as well as some power converters topologies to be integrated into the MMC solution; Section 3 is used to present some PWM techniques to be used in MMC application; Section 4 is dedicated to present the simulations results for different PWM techniques in a 4 full-bridge submodules connected in series developed in PSIM, as well as a comparative analyses are presented; Section 5 presents the main conclusions of this work.

2 Modular Multilevel Converter (MMC)

DC-AC power electronics converters, commonly referred to in the literature as "power electronics inverters", have the main purpose of synthesizing an AC output waveform, from a DC source on the input DC-link, using fully controlled semiconductors (e.g. isolated-gate bipolar transistor – IGBT, metal-oxide-semiconductor field-effect transistor – MOSFET, etc.). With the aid of control algorithms and the consequent activation of power semiconductors, it is possible to control the magnitude and the frequency of the synthesized waveform. The total control of these variables makes this type of converter ideal for motor drives, adjustable speed applications, active power filters, uninterruptible power supplies (UPS), and interface with AC power transmission/distribution systems (the public power grid) [2]. For the following explanations, an IGBT is used as a power switching device but the concepts is valid for other semiconductor devices.

DC-AC power electronics converters can be classified, according to the DC-link configuration, as a voltage source inverter (VSI) or current source inverter (CSI). This type of converters is characterized by discrete values at the output, requiring some precautions during their implementation in order to safeguard the integrity of the system. That is, these power converters are normally controlled by PWM, synthesizing a switched waveform with a switching frequency equal or multiple of the switching frequency of each device. This fact is characterized by the modulation technique used, normally having a carrier wave with the desired switching frequency. One of the most used techniques is the sinusoidal PWM (SPWM), where the modulating waveform is compared with a carrier, resulting in square pulses that will drive the IGBT with different actuation times, as used in [10]. Although the output does not have a sinusoidal waveform, as intended, the frequency of the fundamental component is close to the desired frequency. This fact takes some restrictions on its application as discussed in following.

In the case of VSI, it has high discrete values of dv/dt at the output. As a consequence, the load must be inductive in order to smooth the current waveform. If the load is capacitive, high current peaks will appear [2]. Thus, it is necessary to include an

inductive filter between the load and the output of the VSI. On the other hand, in the case of CSI, it presents high discrete values of *di/dt* at the output. As a consequence, the load must be capacitive in order to smooth the voltage waveform [2]. If the load is inductive, high voltage peaks will appear. Thus, it becomes necessary to include a capacitive filter between the load and the CSI output [2].

Considering the integration of these conventional solutions in high voltage applications, in the case of VSI, it is necessary to increase the voltages in the DC-link. To be more specific, the DC-link voltage should be higher than the peak value of the power grid voltage at the point of common coupling for the correct operation of the DC-AC power converter [10].This requirement depends on the solutions available in the market, both at the level of semiconductor switching devices and at the level of high voltage capacitors. The available quantity of electronic components is one of the most important criteria for the development of power electronics converters in companies, and these specific characteristics have a limited stock. High voltage electronic components are not very common in large quantities at suppliers. On the other hand, increasing the operating voltage level on the DC-link will cause even greater *dv/dt* variations in the output of the VSI. Consequently, bulkier filters are needed.

MMC appears as a scalable solution for high voltage applications. This converter consists of several submodules that allow a better distribution of voltage stress and switching stress. The more the number of submodules, the higher the voltage level of MMC, and higher quality waveforms can be synthesized. Consequently, it is possible to reduce the output *dv/dt* variation, allowing the integration of smaller passive filters. Additionally, also enables the use and selection of more commercially available and robust power electronics components due to their wide applicability in the most diverse applications [7]. In other words, mature medium voltage technologies due to their strong applicability in other applications. Nevertheless, with the integration of MMC solutions, it is possible to increase the resulting output frequency without changing the switching frequency, taking advantage of the complementarity of the different submodules that constitute the MMC. As a consequence, the harmonic contents will be concentrated at high frequencies, being easily filtered [6]. Additionally, being a modular system, replacing a damaged submodule is easier as well as to adapt to the final application, adding submodules as much as need. Nevertheless, redundant protection mechanisms can be implemented [7].

Fig. 1 illustrates some of the concepts mentioned in the previous paragraphs. By analyzing this figure, it is possible to conclude, both in the time domain and in the frequency domain, the impact of the number of levels that MMC can synthesize. It should be noted that, in the given example, the switching frequency of the fully controlled semiconductors in each power submodule is 20 times higher than the frequency of the fundamental component. Thus, it can be seen that the lower the number of levels of the output voltage, the more ample the harmonic spectrum will be, with a high concentration at low frequencies. In turn, with the increase in the number of voltage levels of the MMC, it can be seen that the harmonic content begins to tend towards high frequencies and with low amplitudes.

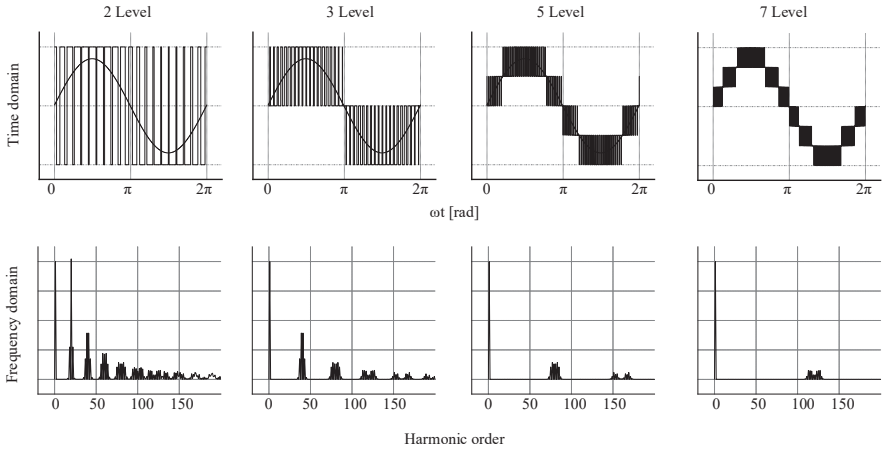


Fig. 1. Influence of the voltage levels that a power electronics converter can produce on the quality of the synthesized waveform.

2.1 MMC Submodule Topologies and Applications

Regarding the configurations of submodules that constitute the MMC, different approaches have been explored. Perez et al. present in [8] different configuration approaches for different submodules. Furthermore, they also present different topologies of power electronics converters that can be integrated into the different MMC power submodules. Similarly, Feng et al. present in [9] different MMC solutions that reputable companies related to railway traction, such as ABB, Alstom, Siemens, and Bombardier have been adopting in the implemented concepts. Barros et al. present in [7] some trends in the MMC configurations.

Fig. 2 shows examples of topologies of power electronics converters to be used as an MMC submodule. A more detailed analysis of the functionalities of each topology, highlighting advantages and challenges of implementation, is presented in the following items.

2.1.1 Half-Bridge Submodule

The half-bridge power electronics converter with split dc-link, represented in Fig. 2 (a), has a simple structure among the other power converter submodules, consisting of only two capacitors on the DC-link and two IGBT devices connected in series. The midpoint of the capacitors in the DC-link is used as a reference for the output voltage, v_{out}, of the converter. Consequently, for a maximum output voltage of V_{DC_link}, the DC-link of the converter will have to withstand twice that voltage with each capacitor having a DC

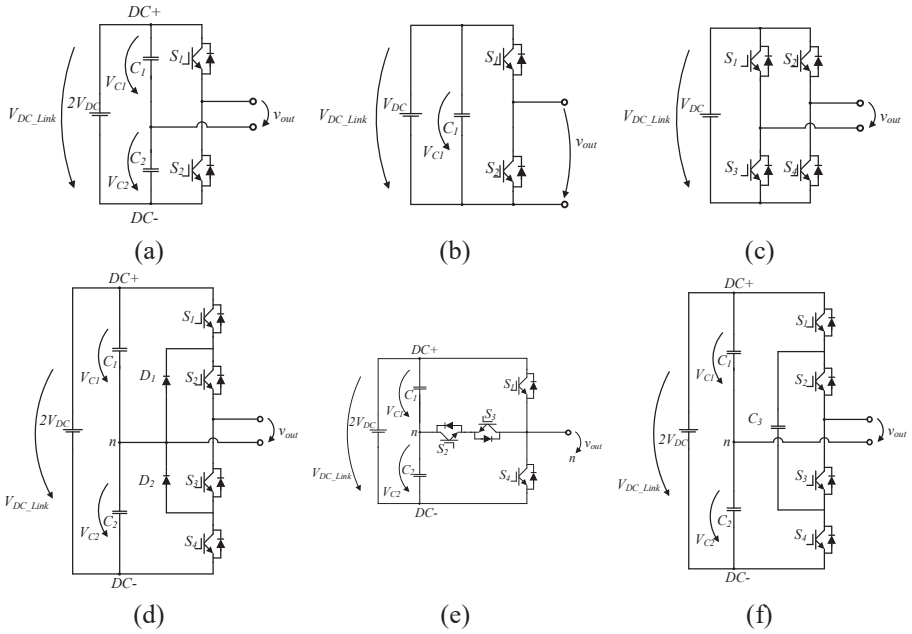


Fig. 2. Power converter topologies used in MMC applications: (a) Half-bridge with split DC-link; (b) Half-bridge; (c) Full-bridge; (d) NPC; (e) T-NPC; (f) FCMC.

voltage of V_{DC_link} at its terminals. The operation principle as well as the permitted operating states are presented in [2].

Another approach of the half-bridge converter is shown in Fig. 2 (b), the difference here is being used a single capacitor on the DC-link. The operation principle as well as the permitted operating states are presented in [2]. Although it only can create an output voltage with a DC component, the half-bridge topology with a single capacitor on the DC-link, is one of the most used typologies for MMC applications. In order to allow the synthesis of an AC waveform without a continuous component, it is necessary to have a complementary submodule. Thus, a submodule is responsible for synthesizing the positive semi-cycle, the second module being responsible for synthesizing the negative semi-cycle. This submodule only works in the first two quadrants (positive voltage only and bidirectional current). It has the simplest structure among the other MMC submodules.

An example of an MMC based on half-bridge submodules with a single DC-link acting as a railway power conditioner (RPC) in railway applications is presented by Tanta et al. in [32]. A 50 kVA three-phase prototype with 10 submodules per phase is presented in [33], where Moranchel et al. presents a comparison of different modulation techniques.

The biggest implementation challenges based on this topology lies essentially in balancing the DC-link voltage of each submodule. In this context, deadbeat predictive current control methodology to reduce the circulating currents and balancing the submodule voltages in the MMC is presented in [11]. Moreover, each submodule will contribute to a portion of the total power, which causes currents circulating in the submodules.

Additionally, and in order to generate an AC component, the duplication of submodules, as well as capacitors, is expected, which will inflate the cost of implementation as well as the complexity of the system [34].

2.1.2 Full-Bridge Submodule

The full-bridge DC-AC power converter, commonly known as H-bridge converter, consists of a DC-link and two arms, each arm being composed of two IGBT devices. The output of the converter is at the midpoints of each arm, as shown in Fig. 2 (c). Each IGBT device that constitutes a converter arm works in a complementary way. The operation principle as well as the permitted operating states are presented in [2]. Due to the semiconductor arrangement, two separate arms in parallel, and with a unipolar modulation technique, it is possible to obtain a resulting frequency at the power converter output voltage with twice the value of the switching frequency imposed on the IGBT devices. This feature is especially important in practical development, making it possible to reduce the passive output filters.

In relation to the practical implementation of this topology, it can be seen that for the same level of output voltage, the voltage on the DC-link is half the level obtained in solutions with a split DC-link. Additionally, due to the existence of two IGBT devices referenced to the same potential, it allows the development of cheaper and more robust driver circuits. In fact, one interesting topology consists of connecting in parallel different full-bridges, sharing the same DC-link. The output of each submodule is connected to a low-frequency power transformer, as presented in [12], with the secondary windings connected in series. The power transformers can have different turns ratio, which gives a variety of output levels even with few submodules. Note that this solution has several IGBT devices connected to the same electrical potential, which allows the implementation of more robust and cheaper gate driver circuits. In order to synthesize all voltage levels, this solution requires a control algorithm capable of detecting the combination of states that allows the greatest reduction in the output error of the generated voltage. One solution is to implement space vector modulation (SVM). However, the lower the switching frequency of the submodules, the greater the transferred power. In [12], the authors state that the module with less frequency can transfer up to 80 % of the total power. Thus, it is concluded that this type of solution would not be the most suitable for a modular implementation.

In [9], different implemented MMC solutions composed of full-bridge power converters are presented, highlighting the combination of these converters with solid-state transformers (SST).

2.1.3 Neutral Point Clamped Submodule

The neutral point clamped (NPC) power converter, illustrated in Fig. 2(d), is essentially made up of an arm with capacitors, with two sets of capacitors connected in series, which constitute the DC-link, and another arm made up of power semiconductors.

Regarding the operating mode, each IGBT device that constitutes a converter arm is activated in a complementary way, in order to control the output voltage. This topology

has the versatility of obtaining two or three voltage levels at the output, v_{out}, depending on the unipolar or bipolar PWM technique adopted. Due to the greater predominance of semiconductors in this topology, being the only passive components in the DC-link, only the conduction and switching losses caused by the diodes and the IGBT devices are considered [3].

Regarding the complexity of implementation and system performance, with the increase in voltage levels generated by the converter, the number of capacitors on the DC-link also increases. Despite the similarity of the components, there will always be voltage imbalances in different capacitors caused by system impedances. In addition, the PWM technique adopted may intensify this imbalance [3]. Due to this intrinsic characteristic, the voltage imbalance on the DC-link presents itself as the main disadvantage of this topology. Different balancing techniques have been developed, namely active control solutions [3], [13], [14], active auxiliary circuits [3], [15], or passive auxiliary circuits [3], [16]. With regard to balancing techniques based on control algorithms, they make the system more complex. In turn, solutions with auxiliary circuits result in greater energy losses, greater complexity of implementation, and higher costs due to peripherals and additional components.

2.1.4 T-type Neutral Point Clamping Submodule

The T-type NPC (TNPC), also known as a neutral point pilot (NPP) [17], [18], has a structure similar to the half-bridge converter with a split DC-link. In addition, T-NPC contains fully controlled bidirectional switches between the ac terminals. The fully controlled bidirectional switches essentially are two anti-series IGBT devices, as presented in Fig. 2 (e). Regarding the DC-link, and similar to the NPC, T-NPC consists of two sets of capacitors connected in series. The upper bus is connected between the positive terminal and the neutral point, and the lower bus is connected between the neutral point and the negative terminal. The midpoint of the capacitors in the DC-link represents not only the neutral point of the circuit but also the reference point for output voltage. Despite the T-NPC is considered as a multilevel converter, the authors of this paper could not find relevant research implemented with the T-NPC as MMC. However, being to be associated in review papers as a potential submodule of an MMC [18].

2.1.5 Flying Capacitor Multilevel Converter Submodule

The flying capacitor multilevel converter (FCMC), introduced by Meynard and Foch, has a similar structure to the NPC, replacing the pair of diodes with a capacitor, as shown in Fig. 2 (f) [19]. Consequently, the operating state in which the two IGBT devices in the middle are conducting is no longer allowed, as it would cause a short circuit to the capacitor [4]. Consequently, the blocking voltage for each IGBT device should be at least V_{DC}. For the correct operation of the power converter, the flying capacitor, C3, must have a voltage at its terminals equal to the voltage of each DC-link capacitor [20]. Regarding the DC-link, and similar to the NPC, it consists of two sets of capacitors connected in series. The upper bus is connected between the positive terminal and the neutral point, and the lower bus is connected between the neutral point and the negative

terminal. The midpoint of the capacitors in the DC-link represents not only the neutral point of the circuit but also the reference point of the output voltage.

Due to the predominance of capacitors in this topology, inrush currents at the start of operation may occur. For this reason, and in order to mitigate large current transients and safeguard the integrity of the system, it is necessary to implement pre-charge circuits [3]. A common practice in order to minimize inrush currents is to insert a series resistor between the capacitors and a DC source during the pre-charge process. Once the minimum voltage value of the capacitors has been obtained, a switch in parallel with a resistor is activated in order to bypass and, consequently, to minimize the energy losses, caused by the resistor, during the system's steady-state operating regime.

Continuing with the topology analysis, it can be seen that the capacitors will play an important role in the system. In fact, the amount of energy stored in the capacitors is directly related to the voltage ripple in each capacitor and, consequently, the performance of the converter. In experimental tests carried out in [21], the authors found that it would be possible to decrease the capacitors' capacity by increasing the switching frequency. However, this approach leads to problems with electromagnetic compatibility. Nevertheless, the reliability of the capacitors, namely electrolytic ones, in power electronics circuits is a major concern. In addition, it is important to consider the space occupied by electrolytic capacitors compared to the space occupied by the diodes of, for example, the NPC topology [3].

2.1.6 MMC Submodules Topologies Comparison

In this item, a comparative analysis of the different topologies addressed is carried out. As it was possible to verify, the different topologies present several modes of operation, restrictions, and requirements for their correct functionality. Table 1 presents some comparative topics between the topologies. It should be noted that the analysis is done from the application point of view, with a requirement for a given minimum voltage value at the converter output, which is the same in all, being necessary to size or adapt the remaining system variables, as is the case of the voltage level on the DC-link. In [22] a more detailed study of more topologies is presented.

By analyzing Table 1, it can be seen that the existence of additional IGBT devices allows the creation of more voltage levels at the converter output. In the case of the half-bridge power converter, since it only has two IGBT devices, it can only generate two voltage levels. In turn, the remaining topologies take advantage of 4 IGBT functionality to be able to generate 3 voltage levels. Nevertheless, the constitution of a single capacitor on the DC-link is simpler in the full-bridge topology, providing robust voltage regulation and simple DC-link control algorithms. Despite the similarity in the DC-link level of the half-point topology with a single bus, for AC applications, it is necessary to insert an additional module responsible for the negative semi-cycle. This fact makes it necessary to duplicate the electronic components used, as well as greater complexity in terms of control algorithms. Additionally, it is possible to conclude that topologies with split DC-link require double the voltage of the DC-link in order to generate the same output voltage level as the full-bridge can.

Table 1. Comparative table of power converter topologies.

	Half-Bridge (i)	Half-Bridge (ii)	Full-Bridge	NPC	TNPC	FCMC
Number of output levels	2	2	3	3	3	3
Number of DC-link capacitors	2	1	1	2	2	2
Number of IGBT	2	2	4	4	4	4
Number of Diode	0	0	0	2	0	0
Unipolar Operation	no	no	yes	yes	yes	yes
Max voltage block	V_{DC}	V_{DC}	V_{DC}	V_{DC}	2 V_{DC}	V_{DC}
DC-link voltage	2 V_{DC}	2 V_{DC}	V_{DC}	2 V_{DC}	2 V_{DC}	2 V_{DC}
Output frequency	f_s	f_s	2 f_s	f_s	f_s	f_s
Cell design complexity	*	**	*	**	**	**
Cell control complexity	**	**	*	**	**	***

*simple; **moderate; *** complex

Another interesting fact for practical implementation resides in the resulting frequency of the output voltage from the topologies. Since the full-bridge is the only one that has two arms with IGBT devices in parallel, it can provide a resulting frequency from the output wave with twice the value of the frequency used for switching. This characteristic is quite advantageous in terms of practical implementation and it can result in a reduction in terms of passive filters which consequently translates into the reduction of losses essentially in the core of the magnetic components.

3 PWM Technique for MMC application

In the literature, there are several PWM techniques for controlling different power electronics converters with 2, 3 or more voltages levels. Regarding the MMC, the PWM algorithms are more complex, with different stages for each power submodule in order to synthesize multilevel waveform. Thus, this topic is dedicated to study the PWM techniques for MMC.

3.1 Level-Shift PWM Technique

The level-shift PWM techniques were initially proposed for the control of MMC based on topologies such as NPC or FCMC. In turn, when these modulation techniques were implemented in MMC solutions consisting of full-bridge submodules, it caused power imbalances in different submodules. In addition to the imbalance in the level of operation functioning between submodules, this fact also causes circulating currents between

submodules as well as the injection of harmonics into the power grid. However, different changes to the PWM techniques have been made in order to provide a greater balance of power in each submodule [23].

Within the level of modulation techniques deviation, one can enumerate the phase disposition (PD), phase opposition disposition (POD), and the alternate phase opposition disposition (APOD). In general, carrier waveforms have the same amplitude and frequency but are arranged vertically with different average values (offsets). The carrier waveforms of the PD modulation technique have the same phase angle, as represented in Fig. 3 (a). The carrier waveforms of the POD modulation technique have symmetry in relation to the zero reference line, with the carrier waveforms lower than this value in phase with each other but 180º out of phase in relation to the upper carrier waves, as can be seen in Fig. 3 (c). Finally, the carrier waveforms of the APOD modulation technique are alternately 180º out of phase, as shown in Fig. 3 (d). Adaptive modulation technique to balance the interface powers in each submodule when PD modulation technique is presented in Fig. 3 (b). For this balanced technique, where can be used with different PWM techniques, a carrier permutation is necessary [24].

Another variant of the level-shift modulation technique consists of overlapping carrier waveforms, being designated in the nomenclature as carrier overlapping (CO). In this modulation technique, the carrier waveforms share the same value of frequency and phase angle, varying the value of amplitude and offset. The overlap value is defined as half the amplitude of the different adjacent carrier waveforms, as shown in Fig. 3 (e). The correct sizing of the modulation index for the CO modulation technique allows a better performance at the level of harmonic content when compared with the aforementioned modulation techniques. This fact is accentuated with modulation indices below 70 %. Due to the overlap of the carrier waveforms, the reference wave intercepts more times minimizing the dispersion of the harmonic content. However, for a modulation index above 80 %, the harmonic distortion begins to approach between the different techniques [23]. Despite its existence in the literature, there is no scientific content that portrays its practical implementation.

The most common practice regarding the implementation of level-shift modulation techniques, consists only of the variation in the vertical axis, amplitude, and average value, always keeping the frequency of the carrier waves constant. However, with variable frequency (VF), it is possible to obtain new features. By varying the frequency of the carrier waves, it is possible to change the harmonic spectrum of the output waveform through harmonic cancellation. Thus, in MMC applications, when the output current reaches peak values, the voltage of the capacitors in the peripheral submodules tends to fluctuate [23]. In order to mitigate this phenomenon, a higher frequency in the peripheral carrier waves of the levels was considered as represented in Fig. 3 (f). With the increase of the frequency in the peripheral submodules, it is possible to decrease the voltage ripple of the existing waveform in the DC-link capacitors and, consequently, improve the quality of the output waveform. In turn, another variant of this control, the VF2, was initially created in order to equalize the losses along with the NPC topology [23]. Since the IGBT devices positioned on the periphery of the converter switch at a higher frequency, the frequency of the intermediate carrier waves was increased in order to equalize the transitions, as illustrated in Fig. 3 (g).

3.2 Phase-Shift Carrier PWM Technique

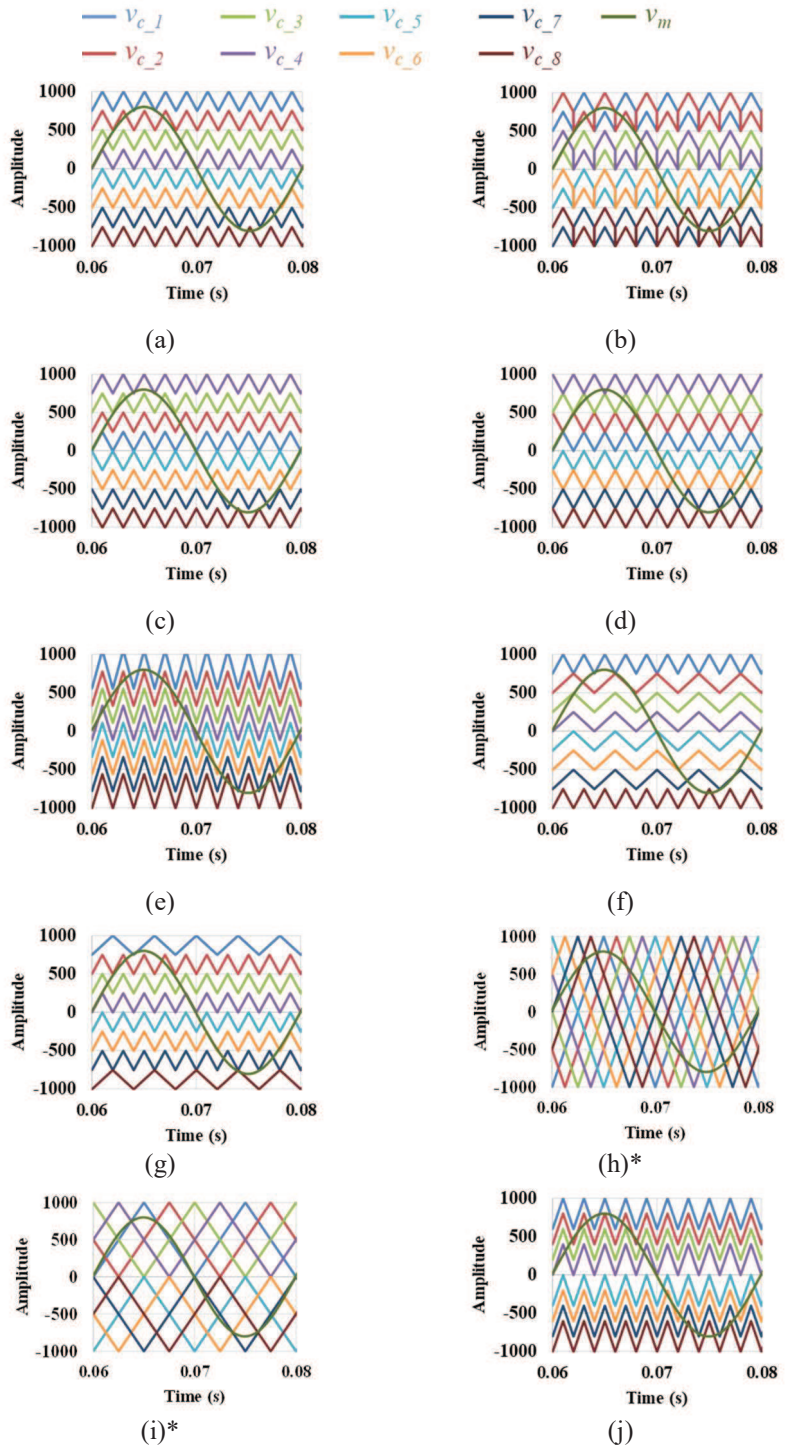
The phase-shifted modulation technique is presented as the pioneering modulation technique for the control of multiple modules of power electronics converters. In this modulation technique, all carrier waveforms share the same amplitude, frequency, and offset value, varying the phase angle between them. This method is exemplified in Fig. 3 (h), where the carrier waveforms are displaced $2\pi/N$ between them. N represents the number of submodules in one MMC arm. This modulation technique minimizes the voltage ripple in the DC-link capacitors, as well as eliminates some harmonic contents in the output voltage waveform. From the point of view of practical implementation for MMC solutions, this modulation technique provides a greater balance in terms of power of the different submodules. However, it has no sensitivity in the fluctuation of the DC-link voltages, unlike the VF technique [23].

3.3 Hybrid Carrier PWM Technique

Hybrid modulation methods take advantage of the best features of previous techniques. However, due to the restrictions of this modulation technique, the number of levels, M, of the converter output has to be odd. Within the hybrid modulation techniques, it is possible to highlight the phase-shift disposition (PSD), carrier overlapping disposition (COD), carrier overlapping phase disposition (CO-PD), Carrier overlapping opposition disposition (CO-POD), Carrier overlap-alternate phase opposition disposition (CO-APOD).

The PSD technique arises from the combination of PSC and PD modulation techniques to control an MMC with M voltage levels. This is characterized by the existence of (M-1)/2 carrier waves with values above the zero reference value and with the disposition of PSC. For the remaining (M-1)/2 carrier waves with values below the zero reference value, these show symmetry with the upper carrier waves, as can be seen in Fig. 3 (i). This modulation method is characterized by the existence of harmonic content concentrated in the value fc (M-1)/2, where f_C represents the carrier frequency. Studies have shown that whenever the modulation index of this control technique exceeds 70 %, the system presents less switching losses than PD, POD, APOD, CO, PSC, and COD [23].

The PWM carrier overlapping disposition (COD) modulation technique results from the combination of the CO technique with the level-shift technique. Considering a converter with M levels, it is necessary to implement two groups of (M-1)/2 carrier waves, configured as shown in Fig. 3 (j). The combination of the carried waves with different lags results in the modulation techniques seen below. Maintaining the phase angle between the carrier waves, the carrier overlapping-phase device (CO-PD) modulation technique is obtained, as represented in Fig. 3 (j). In turn, by changing the phase angle of the group of carrier waves that are below the x-axis, as shown in Fig. 3 (k), the carrier overlapping-opposition disposition (CO-POD) modulation technique is obtained. In turn, maintaining the 180º offset in relation to the adjacent waves, the carrier overlapping alternate phase opposition disposition (CO-APOD) modulation technique is obtained, as can be seen in Fig. 3 (l).


v_{c_1}
v_{c_2}
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v_m
Amplitude
1000
500
0
-500
-1000
0.06
0.07
0.08
Time (s)
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(f)
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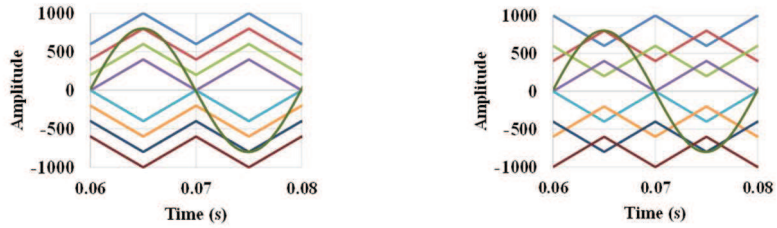
(h)*
(i)*
(j)



(k)* (l)*

***Note:** Using 100 Hz carrier waveforms on Figures (h), (i), (k), and (l) for visualization purposes.

Fig. 3 PWM techniques: (a) PD; (b) Balanced PD (c) POD; (d) APOD; (e) CO; (f); VF (g) VF2; (h) PSC; (i) PSD; (j) CO-PD; (k) CO-POD; (l) CO-APOD.

It should be mentioned that the *y*-axis represents the amplitude of the carrier waves and the modulating waves. For digital programming, the amplitudes of the carrier waves would represent the maximum value of the counter register used in the PWM peripheral. Regarding the modulating wave, this represents the control variable originated in an output current control algorithm, for example, requiring its vertical displacement to be positive values.

4 Simulation Results

The topology adopted for the object of study is composed of four power submodules connected in series that integrate a full-bridge in each one. A DC source is connected to the DC-link of each submodule in order to maintain a stable DC-link voltage, as shown in Fig. 4 (a). The circuit used to generate the PWM signal are represented in Fig. 4 (b). The parameters used for the simulation developed in PSIM are shown in Table 2. That said, in the following topics description and analysis of different modulation techniques are made, as well as a practical comparison, based on computer simulation results, of the PWM strategy with the best results for the adopted topology. For the simulation, two switching frequency were considered, one of 500 Hz for visualization and comparative analysis reasons, and another one of 20 kHz for a more realistic real application approach

Table 2. Main parameters of the computer simulation for different PWM techniques

Description	Variable	Value
Fundamental frequency	F	50 Hz
Modulation Index	m_a	0.8
Output inductance	L_s	5 mH
Internal resistance	R_s	2 Ω
Load	R_{load}	10 Ω
DC-link voltage	V_{DC}	175 V
Switching frequency	f_s	500 Hz and 20 kHz

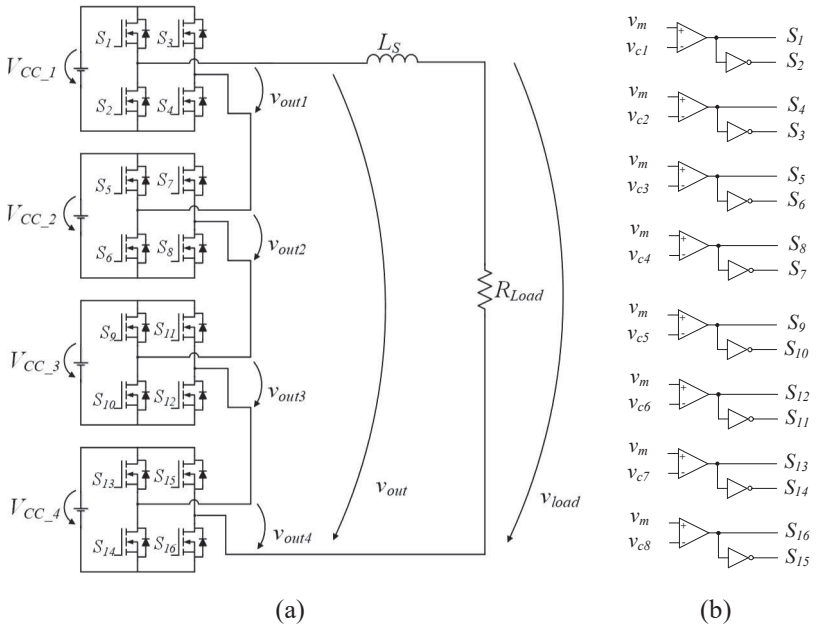
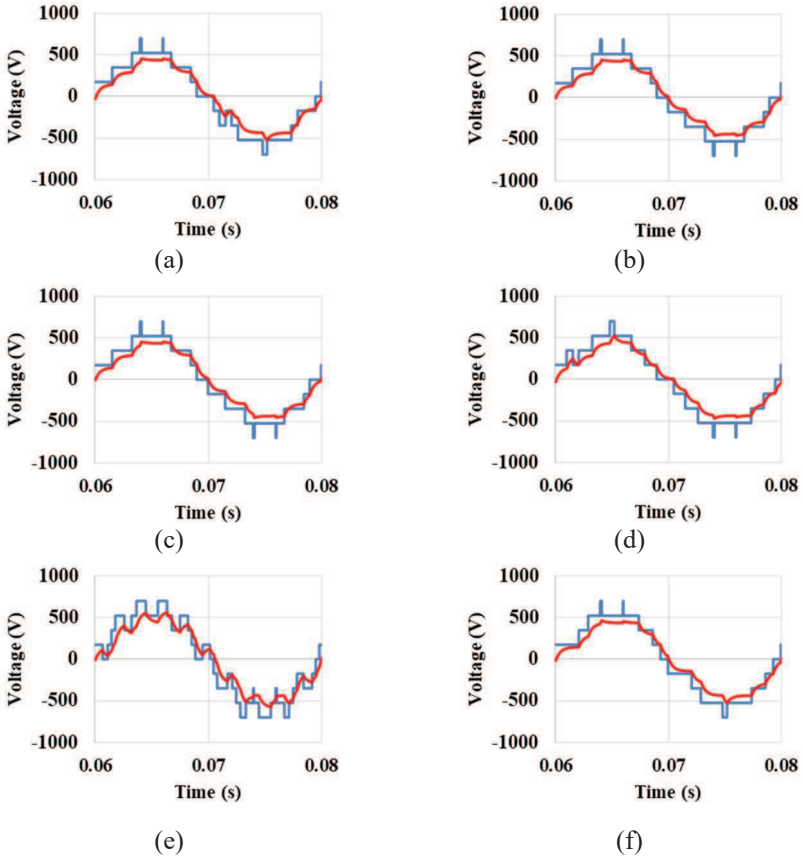


Fig. 4. Electrical schematic of: (a) MMC composed of 4 full-bridge submodules; (b) Control circuit to generate the PWM signals.

Fig. 5 shows the voltage waveforms at the output of the MMC, v_{out}, and in the load, v_{load}. Analyzing the waveforms of Fig. 5 (a) representative of the PD PWM technique, it can be seen that it presents an asymmetry in relation to the *x*-axis. However, using the technique of permutation of carrier waves to balance the interface power of each submodule, represented in Fig. 5 (b), it can be seen that it does not have a significant impact on the waveforms. In turn, when the POD technique is implemented, Fig. 5 (c), it imposes to be symmetric in relation to the *x*-axis. Analyzing the remaining level-shift techniques, the APOD represented in Fig. 5 (d), the CO represented in Fig. 5 (e), VF in Fig. 5 (f), and VF2 in Fig. 5 (g), it can be seen that all of them have an asymmetry of operation. It should be noted that with the CO technique, there is a greater number of v_{out} waveform transitions due to the overlap of the carried waves, which results in a greater number of interceptions with the modulating wave. Regarding the PSC technique, Fig. 5 (h), and since the carrier waves are all arranged horizontally, it can be seen that v_{out} tends to obtain a sinusoidal waveform even at low frequencies. Additionally, there is a total symmetry in its operation. In turn, with the PSD, represented in Fig. 5 (i), and since the carrier waves are grouped into two groups, the intersections will be smaller in each half-cycle, resulting in a slight degradation of the v_{load} waveform. However, it is still possible to verify the existence of an operation symmetry. Finally, the hybrid techniques CO-PD, CO-POD, and CO-APOD, illustrated in Fig. 5 (j), Fig. 5 (k), and Fig. 5 (l), respectively, present the best characteristics of each original technique: a greater number of v_{out} transitions due to the overlap of the carrier waves that results

in a v_{load} waveform close to the sinusoidal even at low frequencies; and a symmetry of operation originating from the POD technique.

For practical implementation, the PSC PWM technique presents as the best PWM technique for controlling an MMC. In addition to presenting good results even at low switching frequencies, it is easy to implement in a dedicated digital signal controller (DSC) platform for power electronics converters. Considering the Texas Instruments DSC C2000 real-time controllers, these have specific registers for horizontal displacement, which facilitates the implementation. In turn, the implementation of vertical displacement in digital control platforms presents greater difficulty, requiring the segmentation of the modulating waveform, v_m, within a certain interval (imposed by the period counter register) and its restructuring in order to maintain the same points of comparison (imposing symmetries in order to maintain the same pulse sequence). Nevertheless, the PWM techniques with asymmetry operation will equally impose an asymmetry operation of the control system when implementing an output current control algorithm and, in some situations, the need for different gains for control of the output signal at the maximum and minimum values. In other words, the PWM techniques with symmetric operation will facilitate the adjustment of gains of the control algorithm used.



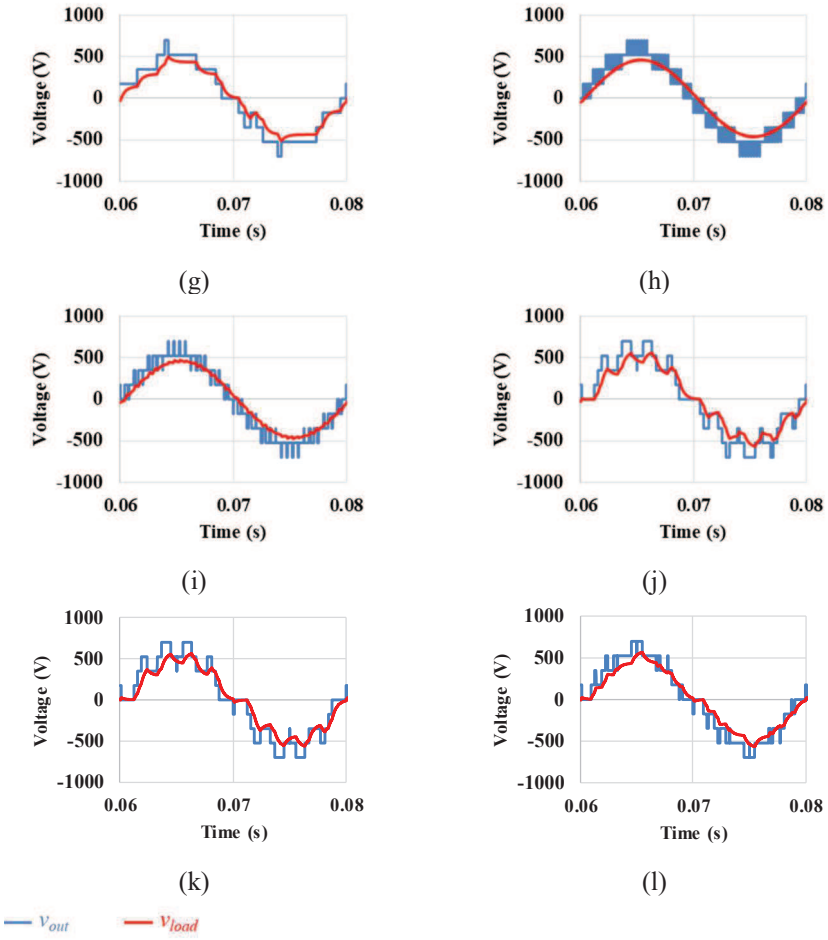


Fig. 5. Output voltage and load voltage using the PWM technique: (a) PD; (b) Balanced PD (c) POD; (d) APOD; (e) CO; (f); VF (g) VF2; (h) PSC; (i) PSD; (j) CO-PD; (k) CO-POD; (l) CO-APOD.

Proceeding with the study, an analysis of the total harmonic distortion (THD) ratio of the waveforms v_{out} and v_{load} was performed for a switching frequency of 500 Hz and 20 kHz in order to determine which of the PWM techniques performs better. The final results of the THD ratio analysis are shown in Table 3. Considering the resistive load, the THD of the output current has a value equal to the THD of the v_{load}. As expected, it is possible to verify that THD ratio of v_{out} is much higher than the THD ratio of v_{load}, measured after the inductive filter, L_s. In addition, it should be noted that overlapping PWM techniques have a higher THD ratio. Analyzing the data, it is possible to conclude that the PSC and PSD PWM techniques have the lowest values of THD ratio for v_{load}, with 0.0768 % and 0.0782 % respectively. The comparison is relevant since the THD of v_{load} also represents the same feature for the output current.

Table 3. $THD_{\%}$ of the MMC output voltage (v_{out}) and the load voltage (v_{load}) for different PWM techniques.

	500 Hz		20 kHz	
	v_{out}	v_{load}	v_{out}	v_{load}
PD	17.3 %	9.67 %	17.2 %	0.261 %
PD-Balanced	17.3 %	9.42 %	17.3 %	0.343 %
POD	17.3 %	10.7 %	17.2 %	0.261 %
APOD	17.3 %	10.7 %	17.2 %	0.261 %
CO	26.3 %	14.9 %	24.6 %	0.944 %
VF2	17.6 %	9.93 %	17.3 %	0.303 %
VF	16.9 %	11 %	17.2 %	0.500 %
PSC	17.4 %	2.71 %	17.2 %	0.0768 %
PSD	17.4 %	2.71 %	17.2 %	0.0782 %
CO-PD	27 %	16.1 %	26.2 %	6.03 %
CO-POD	27.5 %	17.3 %	26.2 %	6.03 %
CO-APOD	20.8 %	12.2 %	18.8 %	6.02 %

5 Conclusions

This paper presents a study of different power electronic converter topologies that can integrate the power submodules of a modular multilevel converter (MMC). The paper also presents different PWM techniques for the control of an MMC, presenting simulation results to highlighting the difference between them. Within the simulation results obtained, it is possible to characterize the mode of operation (symmetry, number of levels and voltage variation), as well as to analyze the total harmonic distortion ratio originated in each modulation technique for a certain case study of MMC. The MMC in this paper is composed by 4 full-bridge submodules connected in series, with an inductive filter and a resistive load.

Based on this study, it was possible to verify the PWM techniques whose carrier waveforms are symmetrical in relation to the *x*-axis, allowing to synthesize symmetrical output waveforms. In addition, it was found that modulation techniques with overlapping carrier waveforms result in a greater number of interceptions with the modulating waveform and, consequently, more transitions in the MMC output waveform. Regarding the THD ratio, it was found that the phase-shift carrier (PSC) and the phase-shift disposition (PSD) PWM techniques allow to synthesize an output waveform with low THD ratio. Consequently, this allows to reduce the passive filters used. Additionally, the PSC is presented as a technique that is easy to implement in a digital signal controller platform, where there are dedicated registers for the horizontal offset of the carrier waveforms. Thus, and for the MMC applications, more specifically made up of full-bridges submodules, the PSC modulation technique is recommended both for its ease of implementation and for the results obtained.

Due to the advantages they present in relation to conventional topologies, MMC will contribute to greater sustainability of electrical systems, the most promising energy source of future smart cities.

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References

[1] L. A. M. Barros, "Desenvolvimento de um microinversor com armazenamento local de energia para aplicações solares fotovoltaicas," M.Sc. Thesis, 2016.

[2] M. H. Rashid, *Power electronics handbook*. Butterworth-Heinemann, 2017, ISBN: 978-0-12-382036-5.

[3] A. I. Maswood and H. D. Tafti, *Advanced multilevel converters and applications in grid integration*. John Wiley \& Sons, 2018, ISBN: 978-1-119-47589-7.

[4] M. Brenna, F. Foiadelli, and D. Zaninelli, *Electrical railway transportation systems*, vol. 67. John Wiley & Sons, 2018, ISBN: 978-1-119-38680-3.

[5] A. Steimel, *Electric Traction - Motive Power and Energy Supply: Basics and Practical Experience*. Oldenbourg Industrieverlag, 2008, ISBN: 978-3-8356-3132-8.

[6] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, *Design, control, and application of modular multilevel converters for HVDC transmission systems*. John Wiley & Sons, 2016, ISBN: 978-1-118-85156-2.

[7] L. A. M. Barros, M. Tanta, A. P. Martins, J. L. Afonso, and J. G. Pinto, "Opportunities and Challenges of Power Electronics Systems in Future Railway Electrification," *IEEE CPE - POWERENG 2020: 14th International Conference on Compatibility, Power Electronics and Power Engineering*, 2020, doi: 10.1109/CPE-POWERENG48600.2020.9161695.

[8] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE transactions on power electronics*, vol. 30, no. 1, pp. 4–17, 2014, doi: 10.1109/TPEL.2014.2310127.

[9] J. Feng, W. Chu, Z. Zhang, and Z. Zhu, "Power electronic transformer-based railway traction systems: Challenges and opportunities," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 3, pp. 1237–1253, 2017, doi: 10.1109/JESTPE.2017.2685464.

[10] L. A. M. Barros, M. Tanta, T. J. C. Sousa, J. L. Afonso, and J. G. Pinto, "New Multifunctional Isolated Microinverter with Integrated Energy Storage System for PV Applications," *Energies*, vol. 13, no. 15, p. 4016, 2020, doi: 10.3390/en13154016.

[11] M. Tanta, J. Pinto, V. Monteiro, A. P Martins, A. S Carvalho, and J. L Afonso, "Deadbeat Predictive Current Control for Circulating Currents Reduction in a Modular Multilevel Converter Based Rail Power Conditioner," *Applied Sciences*, vol. 10, no. 5, p. 1849, 2020, doi: 10.3390/app10051849.

[12] M. B. Latran and A. Teke, "Investigation of multilevel multifunctional grid connected inverter topologies and control strategies used in photovoltaic systems," *Renewable and Sustainable Energy Reviews*, vol. 42, pp. 361–376, 2015, doi: 10.1016/j.rser.2014.10.030.

[13] Z. Ye, Y. Xu, X. Wu, G. Tan, X. Deng, and Z. Wang, "A simplified PWM strategy for a neutral-point-clamped (NPC) three-level converter with unbalanced DC links," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 3227–3238, 2015, doi: 10.1109/TPEL.2015.2446501.

[14] J. Pou, J. Zaragoza, P. Rodriguez, S. Ceballos, V. M. Sala, R. P. Burgos, and D. Boroyevich, "Fast-processing modulation strategy for the neutral-point-clamped converter with total elimination of low-frequency voltage oscillations in the neutral point," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 2288–2294, 2007, doi: 10.1109/TIE.2007.894788.

[15] A. Filba-Martinez, S. Busquets-Monge, and J. Bordonau, "Modulation and Capacitor Voltage Balancing Control of Multilevel NPC Dual Active Bridge DC-DC Converters," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 4, pp. 2499–2510, 2019, doi: 10.1109/TIE.2019.2910035.

[16] R. Stala, "Application of balancing circuit for DC-link voltages balance in a single-phase diode-clamped inverter with two three-level legs," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, pp. 4185–4195, 2010, doi: 10.1109/TIE.2010.2093477.

[17] H. Akagi, "Multilevel converters: Fundamental circuits and systems," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2048–2065, 2017, doi: 10.1109/JPROC.2017.2682105.

[18] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1631–1656, 2017, doi: 10.1109/JESTPE.2017.2742938, ISSN: 2168-6777 .

[19] T. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *PESC'92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, 1992, pp. 397–403, doi: 10.1109/PESC.1992.254717.

[20] S. A. Gonzalez, S. A. Verne, and M. I. Valla, *Multilevel converters for industrial applications*. CRC Press, 2016, doi: 10.1109/MIE.2014.2299500, ISSN: 1932-4529 .

[21] S. S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and comparison of 4-kV neutral-point-clamped, flying-capacitor, and series-connected H-bridge multilevel converters," *IEEE Transactions on Industry Applications*, vol. 43, no. 4, pp. 1032–1040, 2007, doi: 10.1109/TIA.2007.900476.

[22] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18–36, 2015, doi: 10.1109/TPEL.2014.2327641, ISSN: 0885-8993 .

[23] A. Antonio-Ferreira, C. Collados-Rodriguez, and O. Gomis-Bellmunt, "Modulation techniques applied to medium voltage modular multilevel converters for renewable energy integration: A review," *Electric Power Systems Research*, vol. 155, pp. 21–39, 2018, doi: 10.1016/j.epsr.2017.08.015.

[24] P. Sochor and H. Akagi, "Theoretical and experimental comparison between phase-shifted PWM and level-shifted PWM in a modular multilevel SDBC inverter for utility-scale photovoltaic applications," *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4695–4707, 2017, doi: 10.1109/TIA.2017.2704539, ISSN: 0093-9994 .