On-chip array of thermoelectric Peltier microcoolers


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Abstract

This article reports on the theoretical modelling, the finite element modelling (FEM) simulation, the fabrication process and preliminary results of the first on-chip thermoelectric microcooler array (64 pixels arranged in an 8 × 8 array), with each pixel independently controlled. This microcooler array uses co-evaporated V–VI compounds of Bi2Te3 and Sb2Te3 as thermoelectric layers, and can be fabricated using planar thin-film technology, lithography and wet etching, on top of a silicon wafer where the CMOS electronic circuits were previously made. © 2007 Elsevier B.V. All rights reserved.

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1. Introduction

Integration of efficient solid-state thermoelectric microdevices with microelectronics is desirable for local cooling and thermoelectric microgeneration, since they can be used to stabilize the temperature of devices, decrease noise levels and increase operation speed. An array of such devices can also be used for lab-on-chip applications or energy harvesting microsystems. Despite the range of exciting applications, only few approaches to manufacture thermoelectric devices with small dimensions were reported up to now [1–4].

Due to silicon fabrication compatibility, polycrystalline SiGe alloys and polycrystalline Si are commonly used in thermopile applications. Their use in microcoolers has been attempted [5] but the performance is very low compared with that of tellurium compounds, which have been used for many years in conventional large area Peltier devices. Tellurium compounds (Bi2Te3 and Sb2Te3) are well-established room temperature thermoelectric materials and are widely employed in conventional thermoelectric generators and coolers. Different deposition techniques were tried to obtain thin-films of these materials. Thermal co-evaporation, co-sputtering, electrochemical deposition, metal-organic chemical vapour deposition and flash evaporation are some examples. Thin-films of n-type Bi2Te3 and p-type Sb2Te3 were obtained by the authors by thermal co-evaporation [6,7], with thermoelectric figure of merit (ZT) 0.84 for n-type and 0.5 for p-type. Best n-type films have Seebeck coefficient of 220–250 μV K−1, resistivity of 10–15 Ωm, thermal conductivity ≈1.3 W m−1 K−1 [8], carrier concentration ≈6 × 1019 cm−3, Hall mobility from 80 to 120 cm2 V−1 s−1 and EDX analysis revealed a stoichiometric composition. p-Type films have Seebeck coefficient of 160–200 μV K−1, resistivity of 10–15 Ωm, thermal conductivity ≈1.7 W m−1 K−1 [8], carrier concentration ≈4 × 1019 cm−3, Hall mobility from 120 to 170 cm2 V−1 s−1 and are slightly Te-rich (67–73%, measured by EDX) [6,7]. These values are similar to the best found in literature for the bulk materials [9]. Figure of merit can be calculated according to the following equation:

\[
ZT = \frac{\alpha^2 \rho}{\lambda} T
\]

where \(\alpha\) is the Seebeck coefficient, \(\rho\) the electrical resistivity, \(\lambda\) the thermal conductivity and \(T\) the temperature [9]. It is demonstrated that 15 °C cooling is possible to achieve at room temperature using such thin-film materials in an array of microcoolers. Böttner et al. [1,4] uses dry etching to pattern thermoelectric devices in a two wafers process. Power factors of 3 × 10−3 W K−2 m−1 and 4 × 10−3 W K−2 m−1 were obtained, respectively, in n-type and p-type telluride compounds. Verti-
cal columns of thermoelectric materials using lift-off on SU-8 photoresist, was achieved before by Silva et al. [2]. But thermoelectric properties of Bi$_2$Te$_3$ and Sb$_2$Te$_3$ films incorporated in the devices are worst than those obtained in bulk materials. A MEMS-like electrochemical process was also found in literature [3], but figure of merit obtained in materials deposited by this process is still very low. In the present work, high-figure-of-merit films are deposited by co-evaporation, and low cost wet etching techniques are used to pattern thermoelectric devices.

2. Design and simulation

The array of microcooler was designed to accommodate 64 pixels organized in $8 \times 8$ structure (Fig. 1). Each pixel can be independently controlled to heat or cool. Fig. 2 represents a single pixel cross-section. When a current flows from the n-type thermoelectric element (TE) to the metal cold pad and from this to the p-type TE, by Peltier effect, heat is absorbed in the metal–TE element junctions. The reverse applies to contact pads on electronics, where heating is generated by Peltier effect.

FEM simulation was used to calculate the expected temperature drop on each pixel. A temperature drop of $15 \, ^\circ C$, bellow room temperature was obtained (Fig. 3). To obtain this cooling capacity, a membrane (200-nm thick) of silicon nitride supports four pairs of thermoelectric elements (40 $\mu$m $\times$ 100 $\mu$m $\times$ 10 $\mu$m), powered with 14 mA current. Contact resistivity (between thermoelectric elements and metal pads) of $10^{-10} \, \Omega \, m^2$ was assumed on simulations [10,11]. Radiation and convection was considered on the cooled surface (10 W m$^{-2}$ K$^{-1}$). Thermoelectric properties of n-type and p-type elements were considered as achieved on previous experimental results [6,7]. Results obtained from FEM simulation on a single pixel microcooler agree with theoretical calculations [12].

All the cold junctions of the Peltier device are on the Si$_3$N$_4$ membrane. All the hot junctions of the Peltier device and the electronics are positioned on top of the silicon wafer (Fig. 2). The silicon wafer is used as thermal path to distribute all the heat generated by thermoelectric elements and electronics to an heatsink glued around the chip. Fig. 4 shows the overall expected heating of the backside of the chip due to the control electronics, Peltier effect and Joule heating. A power dissipation of 1 mW was considered for the electronics in each pixel and a current of 14 mA is supplied to each microcooler. A 500-$\mu$m thick silicon wafer was used, and the borders of the array were bounded to a fixed temperature of 25 $^\circ C$ (heatsink). A maximum temperature of 27.4 $^\circ C$ was obtained on the backside of silicon wafer.
A CMOS microchip was designed, with the electronics to address and control each pixel of the array, memorizing the state of microcooler. Figs. 5 and 6 show the circuit repeated for 9 (of the 64) pixels. If the duty-cycle of the input signal is greater than 50%, the voltage across the capacitor becomes positive. By the other hand, if the duty-cycle is lesser than 50%, the voltage across the capacitor becomes negative. When the voltage across capacitor is positive, the voltage between the gate and the source of Q1 increases and the same of Q2 decreases. This causes an increase in Q1 current and a decrease in Q2 current. By the other hand, when the voltage across the capacitor is negative, the voltage between the gate and the source of Q1 decreases and the same of Q2 increases. This causes a decrease in Q1 current and an increase in Q2 current. Q5 and Q4 work as constant voltage sources biasing Q1 and Q2, once their currents are imposed by Q3. This solution allows controlling the power applied to each pixel. To minimize heating of Q1 or Q2, their dimensions and the power supply (Vdd and Vss) should be chosen in order to supply the maximum current to the microcoolers (14 mA), while keep Q1 or Q2 in the triode region. Working on saturation region will produce more heating on these transistors, rising the substrate temperature, if many pixels are turned on.

3. Fabrication steps

Fig. 7 presents the fabrication steps of the microcooler array. The backside of the wafer is covered with patterned Si3N4 layer which will act as a mask during etch on last step. The Si wafer (with electronics already fabricated) is also covered with a Si3N4 top layer where two vias are opened to access the contact metallic pads on top that will provide connection between electronics and thermolectric elements. This Si3N4 layer will be used to fabricate the membrane where cool areas will be located. Metal pads to provide interconnection between TE elements are deposited and patterned. The p-type thermolectric material is deposited by co-evaporation and patterned by photolithography on top of the wafer. An etchant with composition 10:6:26 HNO3:HCl:H2O (fuming 99.5% HNO3 and 37% HCl) is used to etch Sb2Te3 p-type film without etching the metal contact pads [13] (etch rate below 0.1 nm/s was measured on contact pads). Bi2Te3 n-type film is deposited by co-evaporation and

<table>
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<th>Table 1</th>
<th>Thermoelectric properties of selected films at room temperature</th>
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<tr>
<td>Film</td>
<td>Te (%)</td>
</tr>
<tr>
<td>Bi₂Te₃</td>
<td>62</td>
</tr>
<tr>
<td>Sb₂Te₃</td>
<td>70</td>
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Fig. 7. Fabrication steps of the microcooler array.

Fig. 8. SEM photo of Bi$_2$Te$_3$ (left) and Sb$_2$Te$_3$ (right) thin-films.
patterned by photolithography. Table 1 presents thermoelectric properties and Fig. 8 shows a cross-section SEM photo of Bi$_2$Te$_3$ and Sb$_2$Te$_3$ films. HNO$_3$ (30% diluted in water) etches Bi$_2$Te$_3$ at etch rate of 250 nm/s and Sb$_2$Te$_3$ at etch rate of 5 nm/s, allowing selectivity of 50 times [13]. Fig. 9 plots the etch rate as function of etchant composition (pure HCl content divided by pure HNO$_3$ content), presenting the composition where best results are obtained. The etch rate observed on aluminium or chromium pads is also less than 0.1 nm/s. Etch rate measurements were all performed on Kapton polyimide substrate. Similar results are expected on top of Si$_3$N$_4$ substrate layer. Photoresist is removed and a passivation layer of Si$_3$N$_4$ is used to avoid degradation of the thermoelectric films in contact with atmospheric oxygen. The last step of fabrication is the etching of the back side of the Si wafer using KOH, to fabricate a membrane of Si$_3$N$_4$ on each pixel that supports the microcooler elements. This membrane achieves significant reduction of thermal conduction between the cold and the hot sides of the Peltier device. Electronic circuits in the wafer are confined to the regions between the microcoolers to prevent damage during the last KOH fabrication step.

4. Experimental results

An enlarged microcooler individual pixel was fabricated and tested on top of a polyimide substrate that emulates the Si$_3$N$_4$ membrane (Fig. 10). The fabrication of these enlarged microcooler pixel allowed a rapid demonstration prototype. The working principle of the microcooler and the quality of materials were demonstrated and evaluated. The performance of the microcooler was analyzed by use of a thermal image map generated with an infrared microscope. An image was obtained with a 4 mA current through the device and cold and hot sides are clearly identified (Fig. 11). A temperature difference of 5°C was measured between the hot and the cold sides, under vacuum. The distance from expected results is due to high contact resistances between metal pads and thermoelectric elements. A contact resistance of $10^{-6}$ Ω m$^2$ was measured, with a method [7] based on TLM (transmission line model) method. This value is expected to be reduced to less than $10^{-9}$ Ω m$^2$ using an interface layer in the fabrication process [2,11]. The high temperature achieved on the hot side of the device results from the low dissipation capability due to the low thermal conductivity of the substrate used in the prototype (polyimide) compared with the substrate used in simulation (silicon covered with silicon nitride). The low thermal conductivity in contact pads also contributes for this higher temperature on the hot side of the device.

5. Conclusions

An array of microcoolers, with 64 pixels, with each pixel controlled independently to cool or heat was designed and simulated, and the respective fabrication process was described. A temperature difference of ±15°C could be achieved in each pixel. Thermoelectric thin-films with high figure of merit were
obtained by co-evaporation, suitable for fabrication of such microcoolers, and lithographic pattern techniques were applied on these films. Bi$_2$Te$_3$ and Sb$_2$Te$_3$ films were patterned with 3:7 HNO$_3$:H$_2$O and 10:6:26 HNO$_3$:HCl:H$_2$O (99.5% HNO$_3$ and 37% HCl), respectively, and selectivity of 50× was measured between these two processes.

A large area pixel of the microcooler was fabricated and its performance analyzed under microscopic infrared imaging. A temperature difference of 5°C was obtained. Differences from expected performance are due to high electrical resistance and low thermal conductance obtained in the pad–thermoelectric material interface. Efforts are being made to reduce contact resistance and fabricate thermoelectric elements with lower dimensions.

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References


Biographies

Lúis Gonçalves graduated in 1993 and received his MSc degree in 1999, both in industrial electronics engineering from the University of Minho, Guimarães, Portugal. From 1993 to 2002 he researched on embedded systems and electronics, on Idite-Minho, an institute to interface between university and industry, Braga, Portugal. Since 2002, he has been a lecturer at Electronics Department, University of Minho. There, he started a new lab on thermoelectric thin-film deposition, characterization and patterning, in collaboration with Physics Department. He is currently working towards his PhD degree and is involved in the research on thermoelectric materials for on-chip cooling and energy harvesting. His professional interests are thermoelectrics, microfabrication technology and microsystems.

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