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Development of a Proposed Single-Phase Series Active Power Filter without External Power Sources

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***Abstract*—The quality of electric power is receiving more and more attention from part of consumers, Distribution System Operators (DSO), Transmission System Operators (TSO) and other competent entities related to the electrical power system. Once the electrical Power Quality (PQ) problems have direct implications for business productivity, causing high economic losses, it is mandatory to develop solutions that mitigate these problems. Active Power Filters (APFs) are power electronic equipment capable of compensating PQ problems that have the ability to dynamically adjust their modes of operation in response to changes in load or in the power system. Among these solutions, the Series Active Power Filter (SeAPF) is specially conceived to deal with problems related to the power system voltage amplitude and waveform. Despite the ability to compensate voltage sags, voltage swells, voltage harmonics, and voltage imbalances in three-phase systems, the SeAPF has not achieved much success neither has not been widely adopted. The lack of interest in this equipment can be largely justified by its high cost and also because of some limitations presented by the SeAPF conventional topology. In this paper is presented a novel topology, as well as the control algorithms of a single-phase SeAPF that is connected directly to the power grid without the use of coupling transformers and that does not require the use of external power sources. The topology and control algorithms of the SeAPF proposed in this paper were firstly evaluated by means of simulation results obtained with PSIM software and, once validated, a laboratory prototype was developed, being presented experimental results that support the correct operation of the proposed system.**

Keywords— Active Power Filters, Harmonics, Power Quality, Single-Phase Series Active Power Filter, Voltage Sags, Voltage Swells.

I. Introduction

Nowadays, we live in a technologically advanced era where electronic equipment is part of the everyday life of any home. Additionally, with the technological development of the industry, as well as more ambitious requirements in terms of quality and quantity, the industry had to be modernized, containing automated equipment based on power electronic converters. However, this sophisticated home and automated industry equipment, when connected into the Power Grid (PG), generate a high harmonic current content, resulting in electrical Power Quality (PQ) problems, that consequently causes to consumers monetary implications [1].

Adjustable speed drives, welding machines and other high-power electronic equipment as well as televisions, computers, printers, lamp electronic ballasts, refrigerators and smartphone charges are some examples with assiduously presence in the industry and at home. Several of this equipment have in similarity a non-controlled diode rectifier followed by a DC-Link, that provokes high current harmonic content [3]. Consequently, these current harmonics, following through the line impedances, cause harmonic distortions in the PG voltage, which makes it a serious problem for electric power producers and, in particular, to the consumers [2].

In addition to the currents harmonics previously mentioned, there are other PQ problems with direct implications in the voltage of the PG, being presented some examples as the follow [3]:

- Inter-harmonics;
- Momentary interruptions;
- Momentary overvoltages (swells);
- Momentary undervoltages (sags);
- Voltage fluctuations;
- Voltage notches;
- Voltage transients;
- Voltage imbalances in three-phase systems.

In addition, the PQ events cause significant monetary losses. Accordingly to [4], around 30% of the most sensitive industry sectors may incur a PQ cost of about 4% of their turnover with about 60% of the cost contribution from the voltage sags and momentary interruptions. Comparing this with the industry European economy, in October 2015 the total PQ cost was estimated to exceed 150 billion euros.

Although the PQ problems have their main origin in consumers, specially industrial consumers, there is a compromise between producers and consumers [2]. The producers undertake to limit voltage harmonics to supply electrical energy within certain stipulated limits (EN 50160 Standard) [5][6]. The same applies to power consumers, who are responsible for limiting the harmonic currents caused by the power electronics equipment in accordance with the permitted electromagnetic compatibility limits standards (CEI / IEC 61000 Standard) [7]. From the perspective of consumers, it becomes important to install equipment capable of providing the harmonics and reactive power required for electrical loads, being the active power supplied by the PG. In this way, it is possible to continuously operate the industry in its full capacity and without compromising the parameters imposed by the energy producers.

Research and development of Active Power Filters (APF) is an area of enormous interest nowadays, presenting solutions capable to, dynamically adapts its operation according to the PQ problems present in the PG. They are classified based in

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three parameters: number of phases, topology and type of inverter.

The APF number of phases is based on three categories: single-phase, three-phase without neutral and three-phase with neutral. Relatively to APF topologies, there are four fundamental topologies: Series APF (SeAPF), Shunt APF (ShAPF), Hybrid APF (HyAPF) and Unified Power Quality Conditioner (UPQC). The first two APFs, SeAPF and ShAPF, represent the primordial topologies, which are strongly used to compensate voltage and current problems, respectively. When these two topologies are combined, is created an UPQC. On the other hand, the HyAPF is based on the integration of SeAPF with tuned harmonic passive power filters [8]–[10]. Finally, the classification of the APF regarding the type of inverter is made according to the storage element used in the DC-Link of the power converter and can be divided into two configurations: Voltage Source Inverter (VSI) and Current Source Inverter (CSI), depending on the storage element [11].

The APFs are composed by an acquisition system and a control system that, with the power converter, provide autonomous mitigation of PQ issues. From the PQ problems presented above, the SeAPF in specific is capable of mitigating majority of the problems related to the voltage of the PG (i.e. momentary interruptions, sags, swells, voltage fluctuation, notches, transients and voltage unbalance).

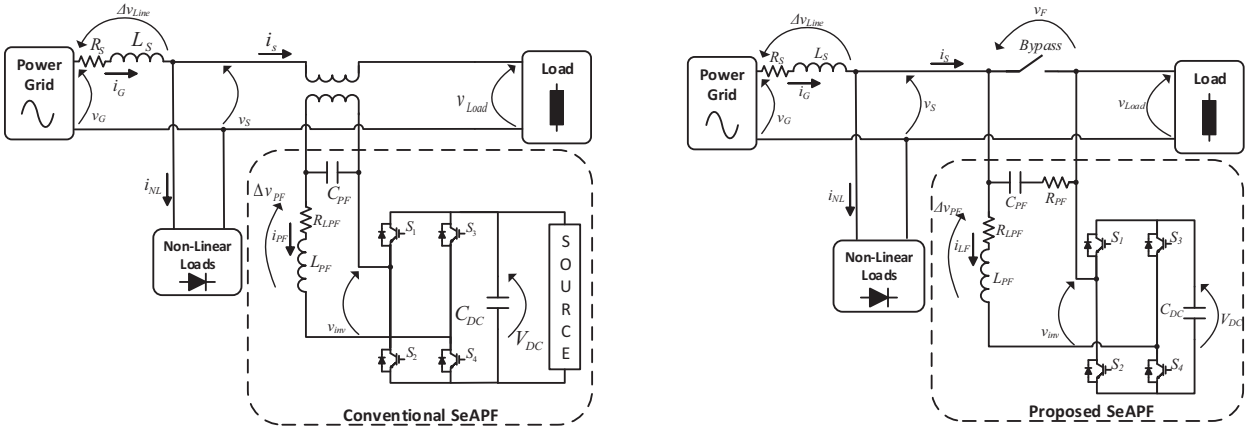
The SeAPF acts identically to an ideal voltage source, providing a voltage that is in phase opposition to the harmonic content of the PG, allowing the voltage waveform of the load to be sinusoidal. With this principle in mind, in 1970, when it was developed the first methods to mitigate PQ problems, it was possible to focus on the development of the first APF. At this time it arises the "conventional" topology of the single-phase SeAPF with coupling transformer between the APF and the PG, as well as, an auxiliary external power source on the DC-Link as shown in Fig. 1 (a) [12]. These aspects provide galvanic isolation between the APF and the PG through the transformer, as well as can compensate for long duration undervoltages and overvoltages due to the external power source. However, due to the fact that the SeAPF injects voltage harmonics through the coupling transformer, it causes high losses and overheating, reducing its life cycle. In addition, the use of transformers and external power sources make this equipment more voluminous and expensive, not presenting an attractive point for the acquisition of this type of equipment [17].

Due to these reasons, a new topology is presented in this paper and is demonstrated in Fig. 1 (b). This novel topology for a SeAPF does not require the extra and expensive components of the conventional topology, being more efficient and more compact. On the other hand, the control system needs to be more sophisticated. However, due to the technological advancement of microcontrollers, having a high processing capacity, more memory and peripherals, the implementation of the control algorithms does not appear as an obstacle. To do so, it would be needed a synchronization method to keep a reference voltage immune to the PG distortions and regulate the SeAPF DC-Link to the reference voltage. Associating this with the information retrieved from the system sensors, it is possible to control the SeAPF to mitigate the PQ problems and provide energy to the loads with sinusoidal voltage waveform.

Finally, this paper is organized in control strategy, followed of the simulation of the SeAPF. Next, is presented the experimental results and the conclusions.

II. Control Strategy

The control strategy of this topology is divided into three main blocks: the Phase Locked Loop (PLL), the DC-Link regulation and the compensation voltage as shown in Fig. 2. The PLL control algorithm composes the first block. This algorithm has the functionality of generating a sinusoidal waveform, v_{PLL}, synchronized with the fundamental component of the PG voltage, v_S [15]. The implemented PLL control algorithm also generate a unitary signal, $v_{PLL\_unitary}$, used in the Compensation Voltage Calculation block. The DC-Link Regulation block is responsible for determining a voltage component, v_{Reg}, responsible for the regulation of the DC-Link. For this, is necessary to determine the difference, V_{DC_Error}, between the reference value, V_{DC}^*, and the actual voltage value on the DC-Link, V_{DC}, as exemplified in (1). The V_{DC_Error} and v_{PLL} are subsequently used in a PI controller to determine the voltage regulation component, v_{Reg}, as can be seen in (2) in order to impose a continuous operation of the SeAPF. Finally, the compensation voltage, v_{Comp}, presented in (3), represents the sum of the three parts: the passive filter voltage, v_{pf}, the harmonic voltage, v_H, presented in the PG voltage and the balance voltage, $v_{Balance}$, to keep the load voltage at 230 V RMS. The passive filter voltage is calculated accordingly with (4), where it is based on the current that passes through the inductor and the equivalent series resistor, R_{LPF}. Then, the (5) related to the harmonic voltage, v_H, is obtained comparing the PLL output signal, v_{PLL}, and the PG voltage, v_S. Lastly, the balance voltage, $v_{Balance}$, is calculated



(a) (b)

Fig. 1. Electrical scheme of a SeAPF: (a) Conventional topology; (b) Proposed topology.

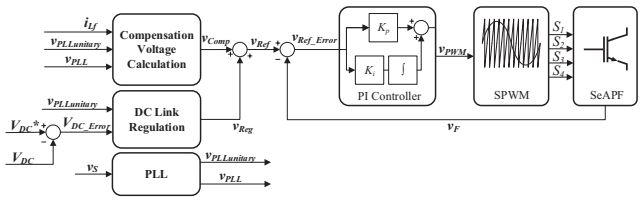


Fig. 2. Block diagram of the SeAPF control strategy.

through the comparison of v_{PLL} and the desired load voltage as presented in (6).

Equation (7) represents the sum of the compensation and regulation voltages, to obtain the reference voltage, v_{Ref}, that SeAPF needs to synthetize. Comparing this value with the SeAPF voltage, v_F, results in an error signal, v_{Ref_Error}, shown in (8). This error is the input of a PI controller that will generate the modulation waveform, as presented in (9), and, the SPWM block, generates the pulses that will be applied to the gate of the IGBTs that constitute the SeAPF.

$$V_{DC\_Error} = V_{DC}{}^{*} - V_{DC} \tag{1}$$

$$v_{Reg} = v_{PLL}\left[k_p V_{DC_{Error}} + k_i \int V_{DC\_Error}\, dt\right] \tag{2}$$

$$v_{Comp} = \Delta v_{pf} + v_H + v_{Balance} \tag{3}$$

$$\Delta v_{pf} = R_{LPF} i_{LF} + L_{PF} \frac{d}{dt} i_{LF} \tag{4}$$

$$v_H = v_{PLL} - v_S \tag{5}$$

$$v_{Balance} = \hat{A} \cdot v_{PLL_{unitary}} - v_{PLL} \tag{6}$$

$$v_{Ref} = v_{Comp} + v_{Reg} \tag{7}$$

$$v_{Ref\_Error} = v_F - v_{Ref} \tag{8}$$

$$v_{PWM} = k_p v_{Ref\_Error} + k_i \int v_{Ref\_Error}\, dt \tag{9}$$

III. Simulation Results

Nowadays computer simulation is an important tool to validate not only the hardware topology but also all the control algorithms that constitute the control system. With the aid of a dedicated simulation software, it is possible to predict the behavior of the SeAPF and tune the control algorithms. With that, it was possible to carry out a more detailed study of the SeAPF to size correctly all the components. In this section are shown the simulation results obtained with the proposed topology. The graphs of the simulations represent the behavior of each control block presented in Fig. 2.

The proposed topology was simulated using PSIM 9.1 software program with the system parameters defined in TABLE I. The proposed topology does not use a transformer neither an external power source, consisting in a two-leg full-bridge inverter with a RLC passive filter in series with the PG and the load (a resistive load in the presented results). The voltage modulation used in the simulation was unipolar sinusoidal pulse width modulation (SPWM).

To validate the reliability of the system, the simulation incorporates five case studies: (1) PLL; (2) pre-charging of the DC-Link capacitor; (3) system in steady state operation; (4) system in transient operation, facing PG voltage sag; (5) system in transient operation, facing PG voltage swell.

TABLE I. System parameters used in the SeAPF simulation model.

System Parameters	Value
PG Voltage/Frequency	230 V/50 Hz
Power System Apparent Power	2.4 kVA
DC-Link Nominal Voltage	200 V
Load impedance	26 Ω
Switching frequency	20 kHz Unipolar SPWM
Passive Filter	L_{PF} = 800 µH, C_{PF} = 40 µF; R_{PF} = 8 Ω

A. Phase-Locked-Loop

In Fig. 3 is represented the PG voltage, v_S, and the resulting plot of the PLL control algorithm, v_{PLL}, during the turn-on transient. To approach the simulation near to the reality, the v_S used in the simulation is similar to the actual voltage waveform in the laboratory, obtained using a power quality analyzer FLUKE 435 *series II*.

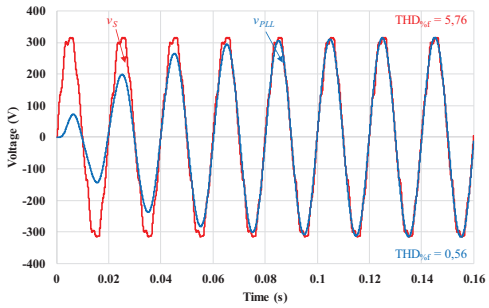


Fig. 3. Simulation result of the PLL signal, v_{PLL}, being synchronized with the PG voltage, v_S.

As it is possible to see, the v_{PLL} gets fully synchronized after four PG cycles, maintaining the synchronization after that moment. In addition, it can be seen that the resulting signal has a residual total harmonic distortion (THD) of 0.56%, even with a THD of 5.76% on the PG voltage.

B. DC-Link Pre-Charging Method

The DC-Link pre-charging method, as explained in the section II, is based in the synthetization by the SeAPF of a low amplitude sinusoidal waveform in phase opposition to the PG voltage. The result obtained with this method is presented in the Fig. 4. Due to the fact the SeAPF connects in series with the load and to maintain its operation in good conditions, this pre-charging is done in a slow way, taking 7.5 s to reach the DC-Link reference voltage. It is important to note that the DC-Link pre-charging occurs only once, when the system is turned on, and during this stage the SeAPF does not compensate the voltage harmonics.

C. Steady-State

Once the DC-Link is charged with the reference voltage, the system starts the operation as SeAPF. The results with the SeAPF operation are presented in the Fig. 5 (b). As it is possible to see, the PG voltage and the load voltage present the same rms values and equal to the nominal value of 230 V. However, as it is visible, the load voltage, v_{Load}, presents a sinusoidal waveform, revealing that the PG voltage

harmonics were compensated by the SeAPF. The $THD_{\%f}$ of the PG voltage is 5.57% while the $THD_{\%f}$ of the load voltage is decreased to 0.89%.

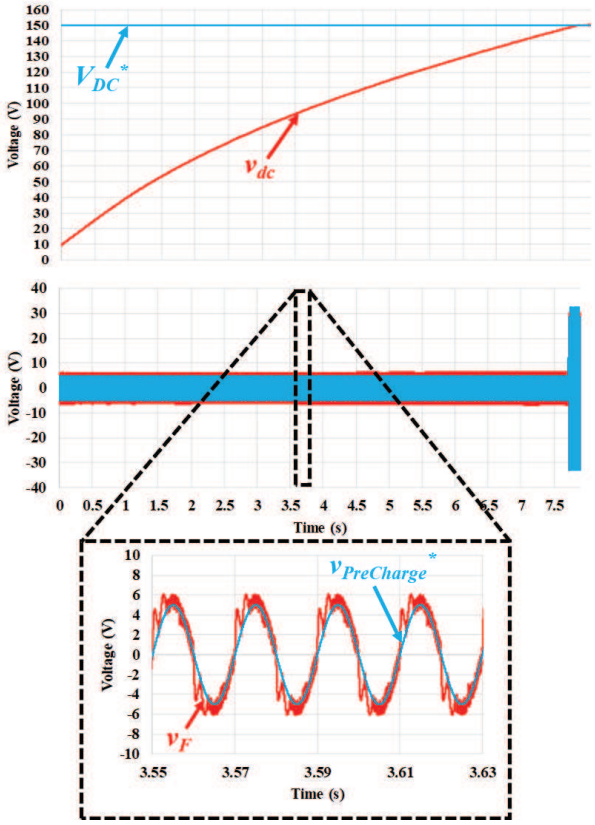
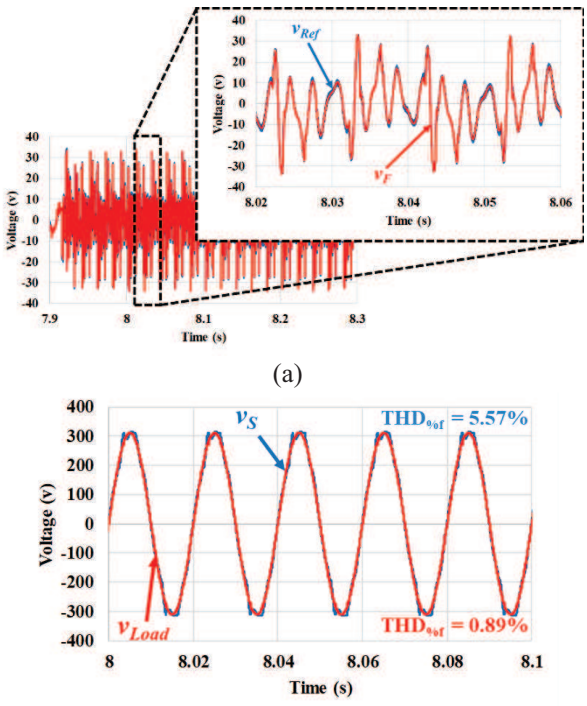


Fig. 4. Simulation result of the pre-charge method through the synthetization of a low voltage signal in opposition of PG voltage.



(a)

(b)

Fig. 5. Simulation result of the SeAPF operation in steady state: (a) Reference, v_{Ref}, and SeAPF, v_F, voltages; (b) PG voltage, v_S and load voltage, v_{Load}.

D. Transient Operation Facing Power Grid Disturbances

One of the requirements of the SeAPF is to compensate voltage sags and voltage swells. To prove this correct operation, were simulated a voltage sag and a voltage swell with 30% and 13% of severity, as shown in Fig. 6. In both cases, the approach to compensate the PG disturbances relies on a constant energy absorption from the SeAPF and limiting the integral error of the PI controller in the DC-Link regulation process. This method allows a fast response when occurs a sag or a swell in the PG.

1) *Sag Event*

The sag event, was programed to happen at 6 s. The control system was able to detect it immediately and impose the user limits in that moment. The SeAPF injects the energy stored in the DC-Link to maintain the load voltage, v_{Load}, stable. This process is demonstrated in Fig. 6 (a). The recovery process is presented in Fig. 6 (b), where can be seen that the DC-Link voltage, V_{DC}, is restored very fast without interfering with stability of the load voltage, v_{Load}.

2) *Swell Event*

In contrast, the swell event was configured to happen at 8.5 s. In similarity, the swell event was also detected by the control system immediately applying the same principle as before. During the swell the DC-Link absorbs energy while the load voltage, v_{Load}, is maintained between the desired parameters as shown in Fig. 6 (d). After the swell event, the DC-Link voltage needs to be restored to its default value. That process is presented in Fig. 6 (e). The DC-Link injects, slowly, the excess of energy in the PG so the load voltage, v_{Load}, is kept stable during that process.

IV. Implementation of the SeAPF Laboratory Prototype

The implementation of the SeAPF prototype with the topology proposed in Fig. 1 (b) is divided in two main parts: the control system and the power circuit, described as follow.

A. Control Scheme

The control system was implemented inside a metal rack box, as presented in Fig. 7, to avoid electromagnetic noise interference from the external noise sources. This prototype part is composed by a signal conditioning and analog to digital converter (ADC) board (2) that converts the analog signals provided by the voltage and current sensors into digital signals, in order to be processed by the Digital Signal Controller (DSC) represented in (4). The DSC uses the information from sensors to execute the control algorithms and to generate the PWM signals. These signals are passed to the IGBTs gate drivers through the command board (1) that converts the signals from 3.3 V TTL logic to 15 V CMOS logic. The command board is also capable of turning off the IGBTs switching if any voltage or current exceed the defined operation limits. For this purpose, an error detection circuit has been implemented in the board (2) whose output signal enable or disable the PWM signals presents in the board (1). Besides that, the control system contains a DC power supply (3) to provide energy to all the electronic boards and a digital to analog converter (DAC) board (5) to allow the real-time visualization, in an oscilloscope, of the DSC internal variables.

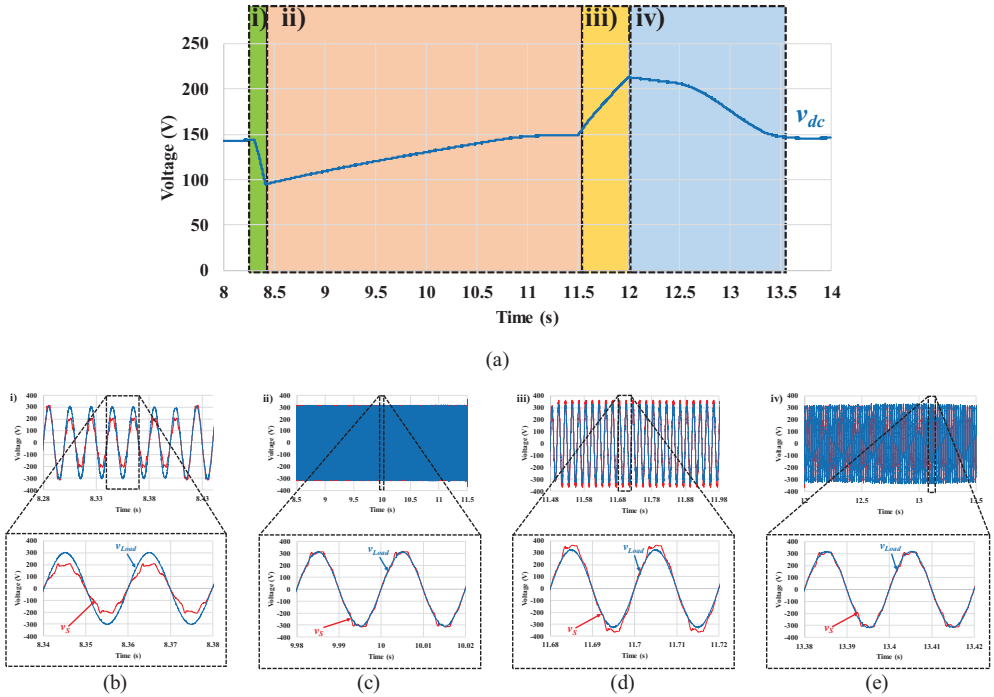


Fig. 6. Simulation results of the SeAPF operating during PG disturbance transients: (a) Variation of the voltage on DC-Link, v_{DC}, during a sag and swell event; (b) PG voltage, v_S, and load voltage, v_{Load}, during a sag event; (c) PG voltage, v_S, and load voltage, v_{Load}, during the recovery time after a sag event; (d) PG voltage, v_S, and load voltage, v_{Load}, during a swell event; (e) PG voltage, v_S, and load voltage, v_{Load}, during the recovery time after a swell event.

B. *Power Circuit*

The SeAPF prototype electric cabinet is constituted by three layers as shown in Fig. 7 (b). The bottom layer (3), in Fig. 7 (b), is related to the interface of the SeAPF with the PG. It is composed by the mechanic contactors to connect and disconnect the SeAPF to the PG, without interrupting the loads voltage. The voltage and current sensors to acquire the variables needed by the control system and the power converter passive filter are also assembled in this layer. In the middle layer (2), represented in Fig. 7 (b), is placed the control system presented in Fig. 7 (a). It is equidistant from both the sensors as the power converter in the top layer (1). In the top layer (1) is located the power electronics converter. Since it is the component that will produce more heat, it was placed in a heatsink with a fan to maintain the operating temperature below the IGBTs limit. Moreover, it was created a simple user interface (4) to enable the PWM signals from the control system to the power converter and to clear the detected errors. Additionally, to allow the user to safely connect and disconnect the SeAPF to the PG, it was also developed a user interface with two push buttons and an emergency stop button (5).

C. *Experimental Results*

A laboratory prototype of the single-phase SeAPF of Fig. 1 (b) was built with the same components value specified in section III. To conduce the experimental validation of the SeAPF with safety, it was used a transformer to reduce the PG voltage from 230V to 50 V. The control algorithms of the SeAPF where implemented in C language and compiled to the TMS320F28335 microcontroller board using the Code Composer Studio IDE. In the following, it will be presented some experimental results related with the PLL as well as the compensation of the voltage applied to a resistive load.

The results presented in Fig. 8 about the PLL control algorithm are very similar to the obtained during the computer simulation. Once the control detects the PLL synchronization, an internal signal is triggered in order to start the dc-link pre-charge method, as presented in Fig. 9. To evaluate the performance of the SeAPF, it was conducted an experimental test with a resistive load of 26 Ω. As can be seen in Fig. 10, the SeAPF voltage, v_F, follows the reference voltage, v_{ref}, however, show small imperfections.

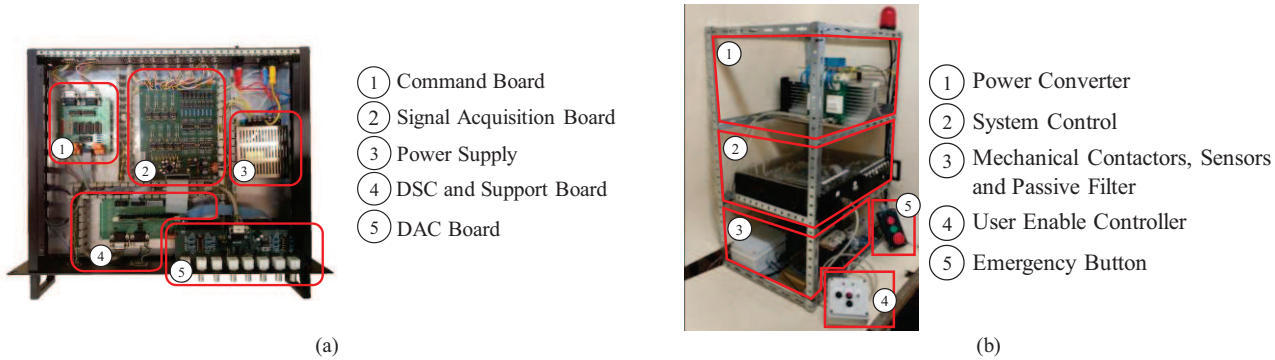
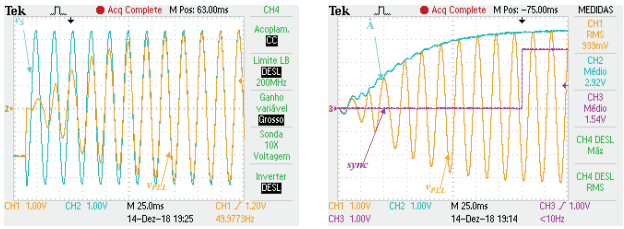


Fig. 7. Hardware implemented for the SeAPF: (a) Control system of the SeAPF prototype; (b) Developed SeAPF laboratory prototype.



(a) (b)

Fig. 8. Experimental results of PLL algorithm: PG voltage, v_S, and PLL voltage, v_{PLL}.

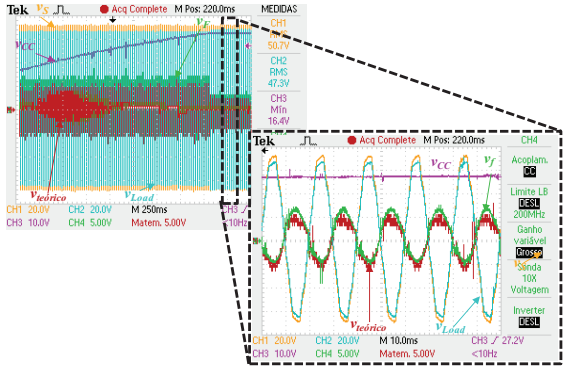
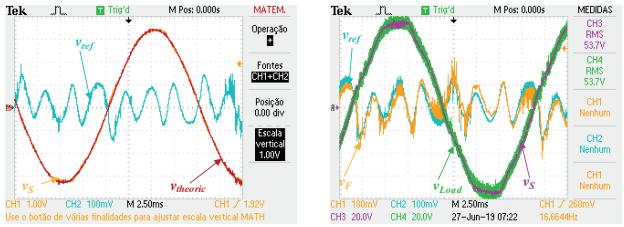


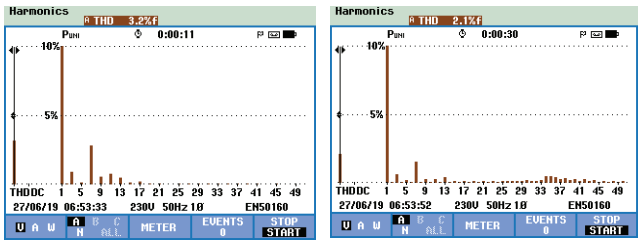
Fig. 9 Experimental results of the dc-link pre-charge process.

Despite that high frequency resonance, it is possible to visualize that the PG voltage, v_S, shows a flattened waveform on the peaks, that is totally compensated by the SeAPF, as can be proved by the load voltage, v_{Load}, reducing the THD of the load terminals from 3.2% to 2.1%, as shown in Fig. 11.



(a) (b)

Fig. 10. Experimental result of the SeAPF in steady state: (a)Theoretical load voltage, $v_{theoric}$; (b) SAPF voltage, v_F, and reference voltage, v_{ref}, and the comparison between the PG voltage, v_S, and load voltage, v_{Load}.



(a) (b)

Fig. 11. Harmonic spectrum of the load voltage, v_{Load}: (a) Load being fed by the PG voltage, v_S. (b) Load voltage during the SeAPF operation.

V. Conclusions

A single-phase Series Active Power Filter (SeAPF) without external power source in the DC-Link and without Power Grid (PG) coupling transformer has been proposed and experimentally validated. The control strategy is based on a PLL circuit to synchronize the control signals with the PG and to calculate the compensation voltage. During the first connection to the PG, the SeAPF executes a pre-charging of the DC-Link capacitor without disturbing the load voltage. During the steady state operation, the SeAPF compensates the PG voltage harmonics making the load voltage sinusoidal. During the PG voltage sag and swell transients, the SeAPF controls the regulation of the DC-Link capacitor voltage and uses this element to provide or absorb energy to compensate the sag or swell, maintaining the load voltage within nominal value. The presented simulation and experimental results validate the functionalities and feasibility of the SeAPF with the proposed topology. As future work, some improvements have to be done in the laboratorial prototype in order to make the hardware more robust to allow experiments at the 230 V rms nominal voltage.

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