INTEGRATED 5.7 GHZ CHIP-SIZE ANTENNA FOR WIRELESS SENSOR NETWORKS

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ABSTRACT

We report on design, fabrication and characterization of chip-size antennas for operation at 5.7 GHz and use in wireless sensor networks. Application of wafer-level chip-scale packaging (WLCSP) techniques like adhesive wafer bonding and through-wafer electrical via formation, combined with the selected antenna types (patch and folded patch) allows on-chip integration and is the main novelty of our work. A short-range wireless link between two systems both equipped with an 8x8 mm^2 patch antenna (measured characteristics: 5.705 GHz central frequency, 90 MHz bandwidth @ -10 dB, 0.3 dB gain, 18 % efficiency) realized on a high-resistivity silicon (HRS) substrate is demonstrated. A folded-patch antenna built on two stacked glass substrates allows size reduction down to 4.5x4x1 mm^3 and has a projected efficiency of 60%.

INTRODUCTION

Application of distributed systems equipped with short-range wireless communication capabilities will highly be facilitated if cheap and easy-to-use 'on-chip' or 'in-package' solutions would be available. The antenna is the key element in order to fully integrate a wireless microsystem into a single chip. The integration requires a small antenna on a low-loss substrate material compatible with integrated circuits (IC) fabrication. As the operating frequencies are increasing (HIPERLAN, IEEE802.11a), on-chip antenna integration having reasonable efficiency becomes feasible [1]. Moreover, due to the frequency increase, the provided bandwidth becomes also acceptable both for data communications and sensor applications. If the frequency is sufficiently high we can even think of the development of a reconfigurable MEMS antenna. Such antenna may have ability of tuning its polarization [2] or to shape its radiating beam into the desired direction [3].

Different solutions have been suggested to achieve antenna integration within a single chip [4, 5, 6]. Since high losses of standard-resistivity silicon are prohibitive for antenna integration, most of the proposed solutions rely on high-resistivity silicon (HRS) or micromachined substrates. The HRS solution uses a bulk substrate having the same electrical permittivity but lower losses. In micromachined substrates, the losses are reduced by selective substrate removal underneath the metal patch.

The drawback is an increase of antenna size due to the effective electrical permittivity reduction resulting from the partial replacement of silicon by air.

MEMS technology and WLCSP techniques when applied to packaging of RF silicon ICs represent truly added value as at a limited cost 3D passive structures can be realized. Application of wafer-level chip-scale packaging (WLCSP) techniques, like adhesive wafer bonding and through-wafer electrical via formation, allows the use of different substrates together with silicon [7]. The use of glass wafers reduces the losses at the expense of a size increase in the integrated antenna. Nevertheless, the use of an advanced antenna design may overcome this drawback providing a small and effective radiator. In this way, the use of glass substrate enables a small on-chip antenna and RF electronics direct coupling. This offers potential of low cost, low profile and simplified assembly. We demonstrate this on patch and folded-patch chip-size antennas.

In this paper, we describe the design, fabrication and measurement of patch antenna built using a HRS substrate. A 3D antenna model was built and the measured antenna parameters were compared with the values obtained by simulation. Next to that, the design of a folded patch antenna realised using stacked glass substrates is presented. Despite its higher fabrication complexity, this antenna has an increased performance and at the same time allows reduction of the used chip area.

ANTENNA DESIGN AND FABRICATION

Patch Antenna

First, a planar antenna operating in the 5-6 GHz ISM band and suitable for on-chip integration was designed. The fabricated prototype is shown in Fig. 1. From the set of available materials used for IC fabrication, standard silicon was not chosen for use as substrate due to its low resistivity. The option was to use HRS together with insulating layers to keep the losses as low as possible.

The used HRS substrate has a dielectric permittivity of 11.7, conductivity in the range 0.02 S/m – 0.05 S/m, and the wafer thickness of 525 ± 25 μm. The use of HRS is enough to provide considerable loss reduction. Nevertheless, the losses can be reduced even further with the use of a dioxide layer between the silicon wafer and
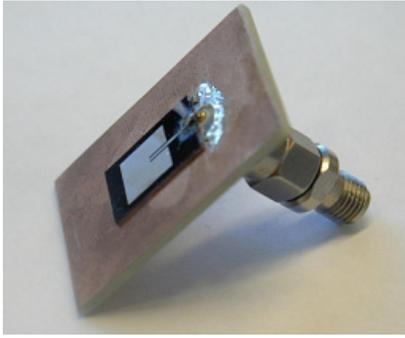
Fig. 1: A 7.7x7.6 mm^2 patch antenna realized on a HRS substrate ready for reflection measurements.

the metal patch. A 300-nm layer of thermal silicon dioxide was used. This layer has a $\varepsilon_r = 3.9$ and it is assumed to be an insulator.

The metal patch and ground plane were obtained using a 2-µm layer of aluminum. Instead, copper could be used to reduce further metal losses. Fig. 2 illustrates the materials and configuration used in the fabrication.

Fig. 2: Cross-sectional view of the realized patch antenna with HRS substrate.

The patch antenna design was supported with a model built using a high frequency structure simulator (HFSS) based on finite elements modeling (FEM) (Fig. 3). A tool with 3D modeling capabilities was necessary due the fact that, for small ground planes, the antenna behavior depends on the ground size.

The two critical steps in designing the patch antenna were the definition of the patch dimensions and the feeding configuration. The patch dimensions have direct influence on the operating frequency and on the antenna gain. The difficulty to predict accurately the patch dimensions is related to the fringing fields together with the small size of the ground plane used. The starting value used for the antenna length, L, was half wavelength in the substrate, which is known to give a close value for the operating frequency. This value was then adjusted by simulation.

The antenna feeding should be designed carefully since it must provide a correct impedance matching. At high-signal frequencies it is necessary to design a feeding line with specific characteristic impedance. Also, that line must be connected in a point of the antenna where the input impedance is the same than the feed-line characteristic impedance. The patch antenna was fed with a microstrip line connected to a point inside the patch where the input impedance is 50 Ω. This connection was achieved with an inset, which had to be properly adjusted with the help of the antenna model.

The model, as well the projected antenna dimensions, are presented in Fig. 3.
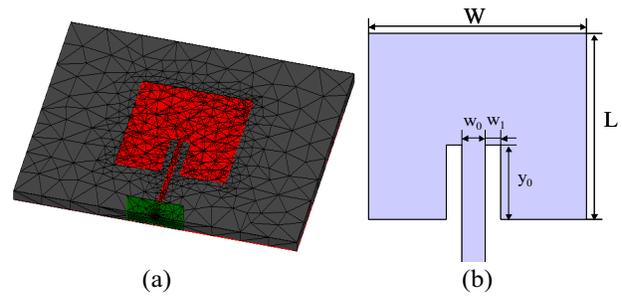

Fig. 3: HFSS meshed model (a), and layout (b) describing the studied square patch antenna (L = 7.7, W = 7.6, y_0 = 3.1, w_0 = 0.36, w_1 = 0.32, in mm).

Folded-Patch Antenna Simulation

The use of a simple patch antenna design on HRS substrate, to achieve antenna integration, suffers from two main drawbacks: large area consumption and low-radiation efficiency. The solution for overcoming this can be the use of different antenna structures combined with different low-loss substrate materials.

In order to meet size restrictions, a folded patch structure is proposed [8]. The folded patch antenna allows the antenna length reduction to one eighth of the wavelength. The main drawback of this antenna is the need of two-stacked wafers and via formation to obtain the desired structure. However, the use of WLCSP techniques brings us the possibility to stack different materials together with silicon. Those materials should be chosen to have low losses and good fabrication processing characteristics [7]. A few suitable available glass substrates are: Corning Pyrex #7740, Schott AF-45 or Hoya SD-2.

The proposed folded antenna, together with the HFSS model is displayed in Fig. 4. This antenna is made up of a middle patch shorted to ground and a ground plane folded around it.
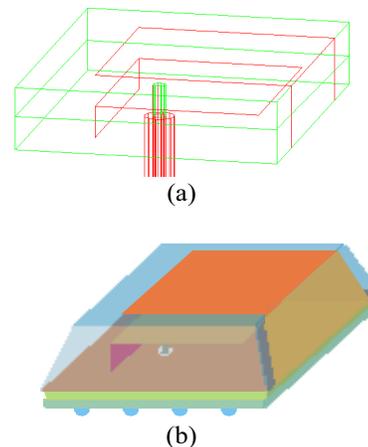

Fig. 4: The integrated folded-patch antenna: a) HFSS model; b) an artistic view of total system.

The folded-patch antenna was designed for fabrication on a stack of Pyrex #7740 glass substrates. Each wafer is 500 µm thick, which gives the antenna overall thickness of 1 mm. The short between the middle patch and ground can be achieved using a slit or several vias side by side

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(via fence). The proposed schematic fabrication sequence is displayed in Fig. 5, and is still under development.
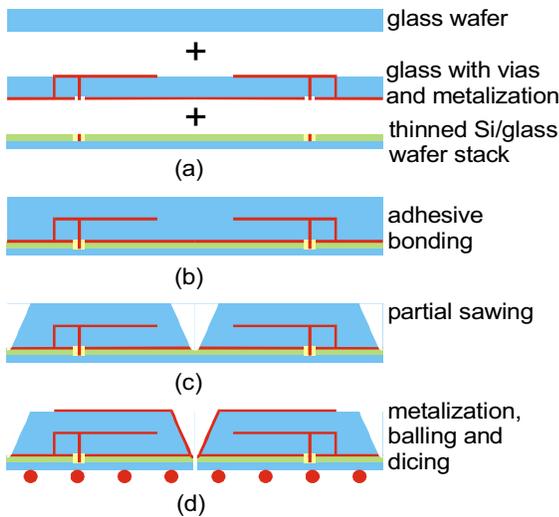

Fig. 5: Schematic fabrication sequence.

The HFSS FEM tool was also used to build a model for the folded patch antenna. The model was then used to design the antenna for operation close to 5.7 GHz.

The obtained antenna return loss is presented in Fig. 6. The designed antenna has central frequency of 5.695 GHz and a –10 dB return loss bandwidth of 50 MHz. The projected efficiency is close to 60 %.
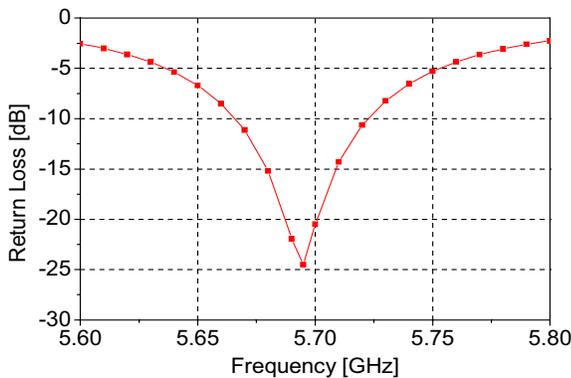

Fig. 6: Simulated return loss of the folded-patch antenna.

The predicted far-field radiation diagrams are plotted in Fig. 7. From this figure we can observe that the power is being mainly radiated from top part of the antenna, as desired.

SIMULATION RESULTS AND MEASUREMENTS OF THE PATCH ANTENNA

The antenna operating frequency, bandwidth and efficiency were obtained from the return loss measurements. The 8510C vector network analyzer was used to measure the return loss. The simulated and measured values for the patch antenna using HRS substrate are plotted in Fig. 8. The simulated data shows good agreement with the measurements. The obtained
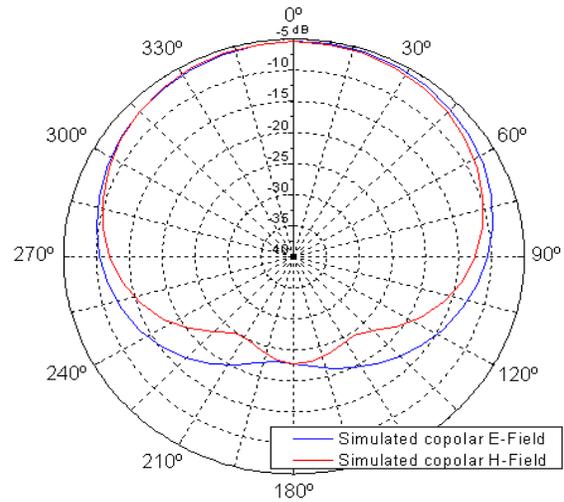

Fig. 7: Simulated co-polar far-field gain patterns for antenna operating at 5.695 GHz.

operating frequency was 5.705 GHz, providing a -10 dB return-loss bandwidth of 90 MHz.

The antenna efficiency was measured using the Wheeler cap method [9]. This method is based in a relation between return loss measurements with the antenna radiating into free space and not radiating. The last condition is usually met with a metallic cover placed around the antenna under test. From those measurements the efficiency can be easily computed. The antenna efficiency was also obtained from simulations and compared with the measured values.

The measured values used for the Wheeler cap method are plotted in Fig. 8. The figure shows the behavior when the antenna is radiating and when it is not, both for simulations and measurements. Using the data from measurements, it was obtained an efficiency of 18.6 %, which is in good agreement with the value computed by HFSS, that was 19.6 %.
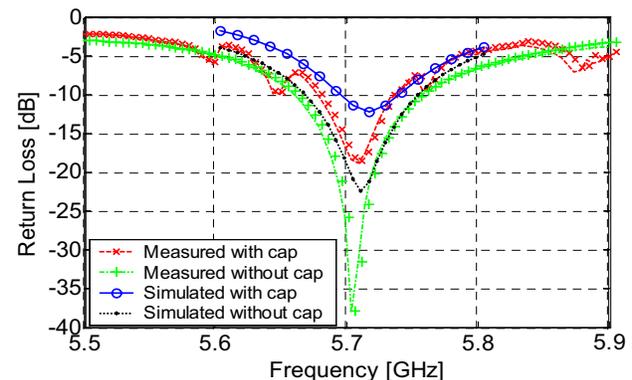

Fig. 8. Measured and simulated return loss versus frequency used to obtain the operating frequency, bandwidth and efficiency of the antenna shown in Fig. 1.

The far-field gain patterns measurements were obtained using the DUCAT anechoic chamber facility at IRCTR-TU Delft. The results are plotted in Fig. 9.

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As it was expected, the antenna exhibits a linear polarization characteristic and the power is mainly radiated from the topside of the antenna. Nevertheless, it would be desirable to further decrease the power level at the back of the antenna to keep the interference with backside components as low as possible. This drawback results from the small size of the ground plane. The maximum gain registered was around 0.3 dB. This small gain is essentially due to low efficiency of the antenna, since the substrate has high losses.
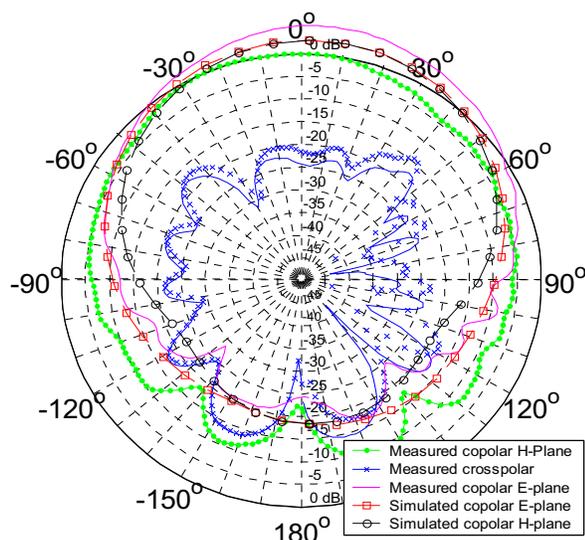

Fig. 9. Measured and simulated co-polar and X-polar far-field gain patterns obtained at 5.705 GHz.

To test the patch antenna effectiveness, a wireless link between two prototypes was established. The radiating antenna was connected to a signal generator and the receiving antenna to the spectrum analyzer. They were placed one meter apart and the output power was set to 0 dBm. A signal power of -50 dBm was received. This result is in good agreement with all the other measured characteristics.

With the model validated by the measured data, the influence of some material tolerances was analyzed by means of simulation. Parameters like substrate thickness, substrate conductivity, and oxide thickness were studied. It was observed that varying the substrate thickness from 500 μm to 550 μm and the oxide thickness from 1 μm to 10 μm, the operating frequency changed from about 5.7 GHz to 5.85 GHz. If the substrate conductivity changes from 0.02 S/m to 0.05 S/m, the efficiency varies from 19.6 % to 30.1 %.

CONCLUSIONS

This work demonstrates that patch and folded-patch antennas on HRS and glass substrates operating at 5-6 GHz are feasible for integration on a RFIC chip for wireless sensor networks. Although high dielectric permittivity of HRS (11.7) is favorable for antenna size reduction, the internal antenna losses are rather high. The analyzed patch antenna has an area of 7.7x7.6 mm^2,

providing a 90 MHz bandwidth at the center frequency of 5.705 GHz, with less than 20% of efficiency.

The glass substrates have better performance when compared to HRS. However, due to their lower dielectric permittivity (~5-6), for the same antenna type and the same operating frequency, significantly larger antenna size is required. To overcome this problem, a folded-patch antenna realized on stacked Pyrex #7740 glass substrates was analyzed. The folded-patch antenna allows size reduction down to 4.5x4x1 mm^3 and has a simulated efficiency of 60%.

A wireless link was established using two patch antenna prototypes. A power of –50 dBm was detected at the receiver when the antennas were placed one meter apart and the transmitter power was set to 0 dBm. The measured values were in good agreement with the values obtained by simulation.

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