End-to-End Synchronization in Packet Switched Networks

N. Almeida*, J. Cabral*, A. Alves* **

** FEUP - Faculdade de Engenharia da Universidade do Porto

* INESC - Instituto de Engenharia de Sistemas e Computadores

Largo de Mompilher, 22, 4007 PORTO Codex, PORTUGAL

Abstract - **The provision of real time services through a Packet Switched Network, requires the adoption of end-to-end synchronization methods. Several of these methods, are compared and a specific hardware solution is discussed. Results obtained through a specially designed Simulation Programme are included, for several network time delay jitter distributions and synchronization methods. These results are used to evaluate systems and design parameters.**

1. INTRODUCTION

The communication services requiring a precise time relation between source and destination (e.g. circuit emulation, CBR and VBR video,...), when supported by a packet switched network (e.g. ATM, DQDB), require end-to-end synchronization methods with variable degrees of quality, according to the service and network performance in terms of delay jitter.

Recent activity in this area has been greatly oriented towards Asynchronous Transfer Mode (ATM) networks, but it will have also impact in other packet switched networks.

For circuit emulation, CBR, and VBR video services, the draft B_ISDN Recommendations (I.321, I.362, I.363) establish the end-to-end synchronization function as an ATM Adaptation Layer (AAL) function. The AAL is mapped between the ATM layer and the User layer (next higher layer). It enhances the services provided by the ATM layer in order to support the functions required by the next higher layer.
In the above recommendations and in the general literature, several end-to-end synchronization methods are being considered but very few and well characterized results are currently available for their evaluation.

A general study of several synchronization methods and their evaluation, is currently in progress, taking in consideration performance and implementation aspects. A simulation programme was developed, HW designed and, in order to make laboratorial tests of main concepts under different conditions, a flexible test system for CBR services is being developed.

The end-to-end synchronization methods most frequently referred to in the literature are:

- Adaptive clock (FIFO level);
- Time Stamping;
- Synchronization Patterns.

A slipping technique (plesiochronous clocks) may also be used, in some cases, where slips can be accommodated, as described in section 3.

This work was started in ESPRIT project 2054 (UCOL-UltraWideband Coherent Optical LAN), in relation to the development of high speed interfaces for CBR services [1]. UCOL is a coherent multichannel optical network of very high performance using a transfer mode based on ATM concepts [2]. These explains why much attention has been given to ATM standards in the current study.

However it must be stated that delay jitter characteristics and cell error rates of UCOL are expected to be substantially different from B-ISDN specification.

In a first phase, the work was oriented towards a better specification of the selected end-to-end synchronization methods. A version of the adaptive clock method, based on buffer (FIFO) level, was the first selected for evaluating, as it showed advantages for CBR services. A preliminary design of all major blocks involved was made. The adaptive method (FIFO level) HW structure is described in section 4.

The simulation programme developed, which allows the analysis and study of the full system behaviour, has been used to optimize the main system parameters.

Simulation results are already available for the adaptive clock recovery (FIFO level) strategy. These results are presented in section 5.

2. GENERAL STRUCTURE OF A END-TO-END SYNCHRONIZATION SYSTEM

2.1. Structure

UCOL high speed interfaces contain two main subsystems: User interfaces (UI) and the ATM Adaptation Layer (AAL).

As mentioned before, the source clock frequency recovery function, is included in the AAL, which will be described in some detail.

The AAL is also the layer responsible for the adaptation of the service specific data format to the cell transport data format. The former is characterized by a continuous and isochronous delivery of information, and the later is of a bursty nature, as the information is being packed in cells for transmission.

2.2. Data formats

Recommendation I.362 (B-ISDN AAL functional description) provides a classification of services (based on the attributes of timing relation between source and destination, bit rate, and connection mode) in order to assist in the development and selection of suitable methods to support the existing (and future) wide range of services. This classification (specific to AAL) has distinguished four classes, from A to D. Typical examples may be: class A-circuit emulation; class B-variable bit rate video and audio; class C-Connection Oriented data transfer and class D-Connectionless data transfer.

Recommendation I.363 (B-ISDN AAL specification) introduces four types of operation (1 to 4) needed to perform all the necessary functions for these service classes.

AAL type 1 and type 2 operation modes are, respectively, indicated for CBR and VBR services requiring end-to-end timing / synchronization.

To obtain a greater flexibility, AAL is also divided into two sublayers: the Segmentation and Reassembly (SAR) sublayer and the Convergence Sublayer (CS).

The SAR, and CS, Protocol Data Unit (PDU) formats for the AAL type 1, are shown respectively in figure 1 and 2.

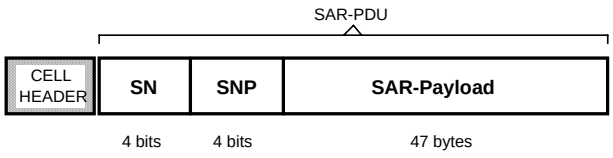
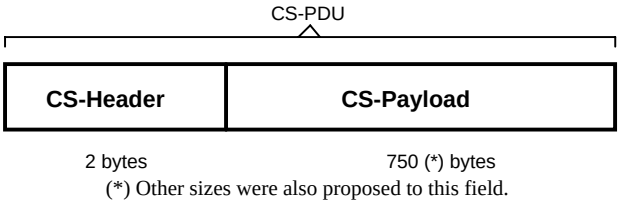


Figure 1. SAR-PDU format for AAL type 1.



(*) Other sizes were also proposed to this field.

Figure 2. CS-PDU format for AAL type 1.

The CS-PDU format is not so well established, but some of the major guideline contributions, indicate the format shown above as a possible solution [3],[4]. The CS header will probably be two byte long, almost exclusively dedicated to synchronization purposes.
The system designed uses PDU formats as shown in figure 3.

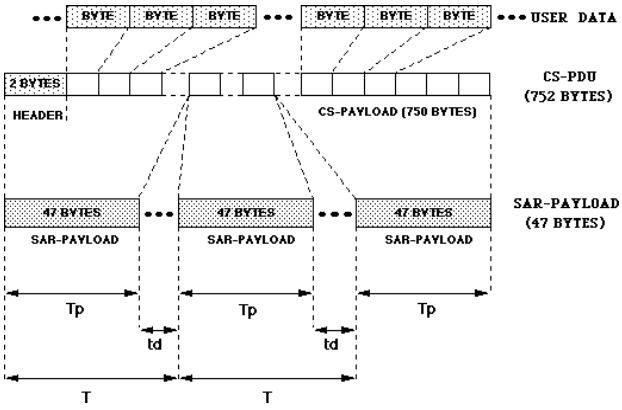


Figure 3. Sync. Test System PDU formats.

The value for **Tp** depends only on the network (line) bit rate. The average value for **T** equals the period service bit rate times 376 (47*8). **td** is the time between two successive cells.

2.3. Test System

In the stage of development of UCOL, there were still a number of uncertainties which recommended a flexible approach to be adopted. It was decided to design the system in such a way that several mechanisms could be easily implemented. On the other side it was decided to implement a test system to allow the evaluation of these subsystems in advance to the network being available.

The general structure of the End-to-End Synchronization Test System is shown in figure 4.

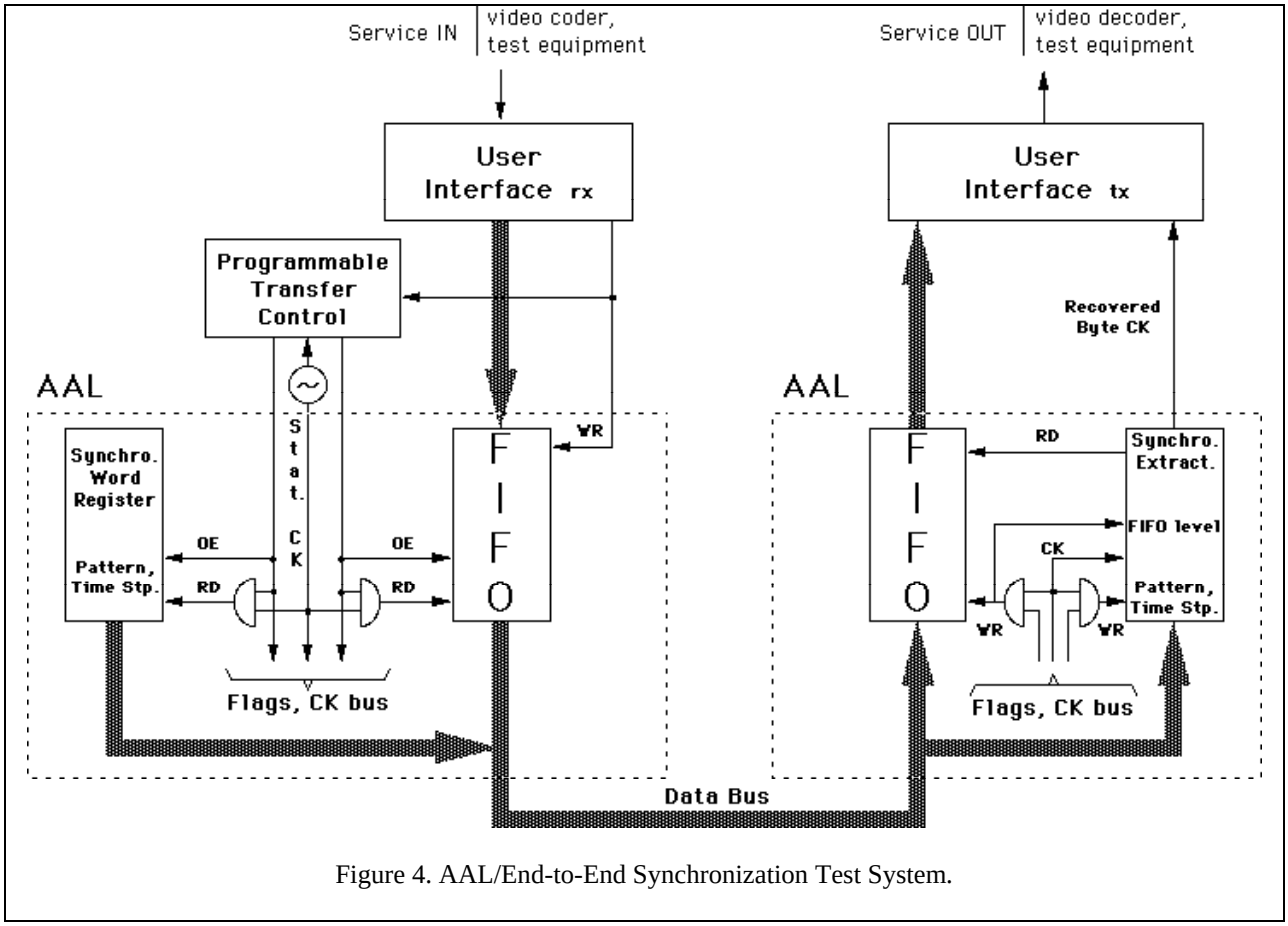


Figure 4. AAL/End-to-End Synchronization Test System.

It consists of user interfaces and AAL subsystems as designed for the real interfaces with the addition of a Programmable Transfer Control (PTC) unit.

The system operation is as follows: data coming out from the "user interface", in parallel, is introduced in a FIFO; a transfer control unit generates clock pulses moving data out of the FIFO in cells (47 bytes long / no header), separated by programmable intervals; a remaining block on the transmitter side is used for the insertion of special words or patterns required by some of the synchronization methods; on the receiver side the reverse operations occur, with the communication between the two parts made via a parallel bus (19.4 Mbyte/s-155 Mbit/s).

The PTC unit acts as a traffic intercell interval generator. The delay jitter, resulting from the several nodes of the network is generated in the PTC, allowing the test and evaluation of the different methods of clock extraction.

The statistical characteristics of the delay jitter can be programmed. Figure 5 shows the functional structure of this unit.

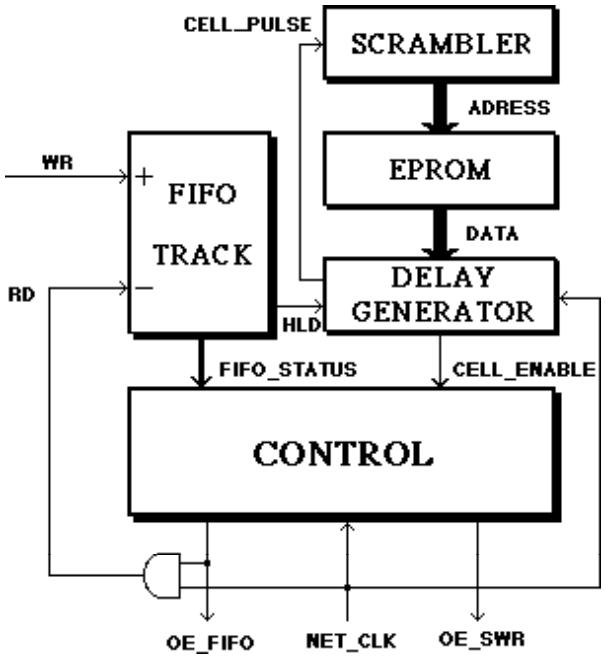


Figure 5. Functional structure of the PTC.

The FIFO_TRACK block saves the difference between the number of Write and Read pulses, in order to determinate the FIFO current level. In some cases it is possible that, as a consequence of the statistical distribution of the delay jitter, FIFO becomes empty. In

this case, a Hold flag is activated, in order to delay the Read pulses.

The statistical distribution is generated in the Scrambler and EPROM blocks. The Scrambler produce a pseudo-random sequence with Uniform distribution and with a period of 2^n (n-number of bits of the shift-register). Each value generated by the Scrambler block addresses the EPROM block which contains the inverse of Distribution Function of the chosen statistic, producing a pseudo-random sequence with a distribution according to the EPROM content. Thus it is possible to change easily the distribution function of the delay jitter just by changing the EPROM content.

The Delay Generator block receives the delay intercell interval information of the Data bus to produce the corresponding delay. This information is supplied to the Control block through the Cell_Enable signal which indicates the start of cell.

The Control block, by means of these signals, will generate the clocks and produce the pulses necessary to build the cell packets in the required format, affected with delay jitter following the selected statistical distribution function.

3. SYNCHRONIZATION METHODS

3.1. Slipping (plesiochronous clocks)

This method does not in fact perform any synchronization between the two-end terminals. The two clocks run independently with a predefined precision and the resulting slip is hidden, using an appropriate mechanism at a different level, so that to the user it looks as if the two systems are synchronized.

Indeed, services as video or audio, may accept periodic bit slips if these were forced at times not relevant to the service (e.g. non-active video lines, audio silence intervals). The faults will be subjectively null. These actions have to be related to the specific service and therefore not completely transparent.

For this reason it does not meet UCOL requirements.

3.2. Adaptive clock (FIFO level)

This method adjusts the local clock with a digital phase-locked loop (DPLL) by observing the occupancy of an input buffer at the receiver end. This is the simpler method since no knowledge about the transmitted signal (e.g. detection of silence intervals or timing information) is required. Figure 6 shows the functional diagram of this DPLL.

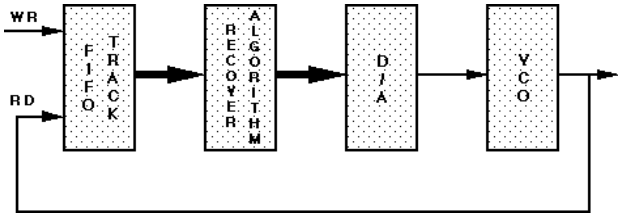


Figure 6. Functional diagram of the DPLL.

Since the write clock to the FIFO is bursty (no pulses when there are no packets arriving) and the read clock is continuous, the phase-detector is different from a conventional one, which compares the phase of a VCO output signal to the phase of a reference (input) signal.

Here the phase-detector is substituted by a FIFO-Level-Tracking (FLT) and a Recover-Algorithm (RA) block. The FLT block saves the current level of the FIFO occupancy, providing that information to the RA block. The RA based on the FIFO occupancy and its history will produce through the D/A, the appropriate control-voltage to VCO. The RA provides that the FIFO occupancy must be about half of its full capacity. This algorithm must avoid buffer over and underflow during the frequency acquisition process. Thus with a sufficiently sized FIFO and with a “good” algorithm the range of input delay jitters that the system may accept can be increased.

Section 4 describes, in more detail, studies made on this matter. The objective is to maximize the capacity of tracking the incoming frequency and to minimize buffer size.

3.3. Time Stamping

In the time stamping method, the transmitter writes an explicit time indication in the CS header. In the receiver, this time indication is compared with a local generated one. The result of the comparison is used to synchronize the local clock.

Figure 7 shows one variant of the time stamping method. This variant does not take into account the possible existence of a common timing reference.

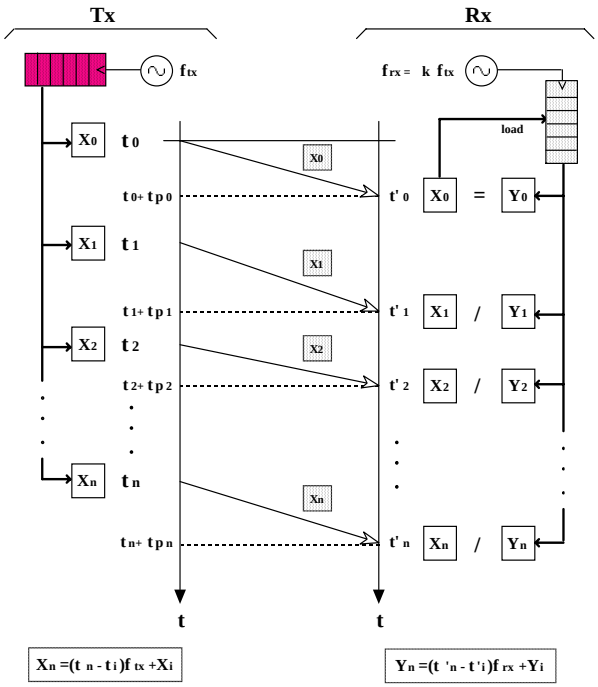


Figure 7. A time stamping operation mode.

The goal is to determine the value of **k,** in order to make the corrections which will equalise the receiver with the transmitter frequency. This may be difficult, taking into account the possible existence of significant network cell delay jitter and the fact that the reference clock used for stamping is not common, and great frequency precision is required.

Indeed, a better exploitation of the time stamp method requires a common timing reference (section 3.4). This represents a considerable drawback when considering networks without a reference clock, as UCOL network was designed.

3.4. Methods based on synchronized transmission links

In some cases a common clock is available distributed by the network. In this case it is possible to take advantage of the common timing reference present at the source and receiver nodes.

The operation of synchronization is achieved as follows: at the emitter the difference between the source and the network clock is coded and then transmitter to the receiver; the receiver, with this information, plus the available node network clock, can recover the source clock [5].

This method cannot obviously be used in most situations and was not considered as it is not applicable to UCOL.

These considerations led us to select the adaptive clock method for our first implementation. This seems to be not very complex to implement and capable to the synchronization requirements.

4. ADAPTIVE METHOD (FIFO LEVEL)

A number of possibilities to implement the recovery algorithm are discussed below.

4.1. Direct approach

This method is based on the current position of the FIFO. The FIFO_LEVEL_TRACKING block keeps track of the FIFO occupancy, in order to provide the convertion block with the current level of the FIFO. The CONVERTION_TABLE converts this information in a correction word that, through the D/A, will give the error voltage to the VCO in order to track the incoming frequency. Figure 8 shows the functional structure of this method.

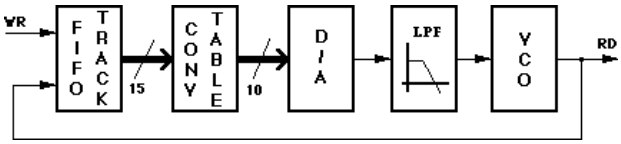


Figure 8. Functional structure of the Direct method.

4.1.1. Parameters and Procedures

The CONVERTION_TABLE is simply a table that converts the current level of the FIFO in a word that, through the D/A, produces the appropriate control voltage. The word generated by the CONVERTION_TABLE must be limited in order to keeps the recovered frequency bound to the nominal range. The number of bits of the D/A must be sufficiently large in order to obtain a good resolution to the output frequency. The Low-Pass-Filter (LPF) main function is to smooth the D/A output voltage steps, between consecutive words.

4.2. Charge Pump approach

This method use a DPLL to recover the frequency of the transmitter clock. Here the Digital Phase Detector keeps track of the FIFO occupancy status and generates UP and Down signals to speed up or slow down the output frequency of the VCO. An error signal is generated by the Charge Pump circuit based on the UP/DOWN signals and then smoothed out by a loop low-pass-filter. Figure 9 shows the functional structure of this method.

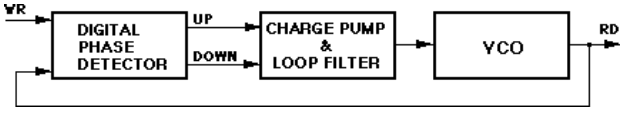


Figure 9. Functional structure of the Charge-Pump method.

4.2.1. Parameters and Procedures

The characteristics of the input delay jitter distribution and the allowed range of frequency variation , that the receiver terminal can accept, determine the size of the FIFO and the cutoff frequency of the LPF. This method

establishes two thresholds, each one being close to the ends of the FIFO.

The FIFO occupancy can be determined by subtracting the WR and the RD pulses. If the subtracted value (FIFO occupancy) is between the two thresholds, both UP and DOWN signals are not asserted and the VCO output frequency is retained. However, if the value is below the lower threshold, Down signal is asserted and the VCO output frequency is decreased. Similarly, if the value is above the higher threshold, the read clock frequency is increased. Consequently, the read clock speed is adjusted dynamically to maintain FIFO occupancy between the two thresholds.

The cutoff frequency of the LPF, should be limited so that high frequency fluctuation of the FIFO occupancy will be filtered out and thus the frequency variation of the receiver clock is bound to the nominal range.

4.3. Hybrid approach

The adaptive method based on the FIFO occupancy, described on the two last preceding sections, shows two ways of extracting the source frequency of the incoming data. A hybrid method has been studied which comprises the techniques of both and incorporates some new procedures in order to improve the performance of the adaptive method. The functional structure of this method is shown on figure 10.

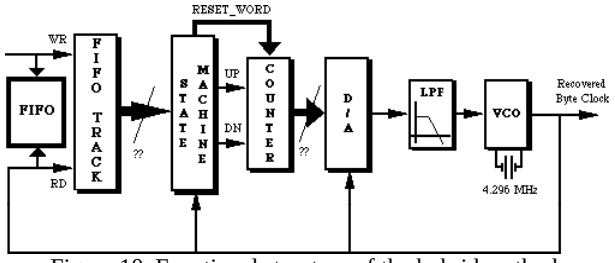


Figure 10. Functional structure of the hybrid method.

Here a FIFO_TRACKING block is also necessary and has the same characteristics of these in the previous sections. The state machine block perform the procedures based on the information which is provided by the FIFO_TRACKING block. The outputs of this block are the UP and DOWN signals to correct the frequency and a reset word to initialize the system to the nominal frequency in case of faults. The counter block is incremented or decremented in order to increase or decrease the read clock. The output of the counter feeds a D/A which converts the output in the corresponding control voltage to the VCO. A Low Pass Filter (LPF) is necessary to smooth the transitions between two successive words.

4.3.1 Parameters and procedures

The algorithm implemented in the state machine performs the corrections in the VCO based in two factors: the variation on the buffer filling level, between two or more time intervals, and the absolute level of the FIFO. The state machine, based on these two factors realize the correction of the read clock, through the UP and DOWN signals.

The correction based on the variation of the buffer level is the only action that is performed while the FIFO_level is between the two near end thresholds. When any of these limits is raised, only corrections based on the absolute level factor are made.

The correction factor based on the variation of the buffer filling level is obtained by calculating the average through a set of values, corresponding to the difference between two consecutive FIFO level readings. The number of values in each average is one of the parameters evaluated under simulation.

5. SYSTEM SIMULATION PROGRAMME

In the previous sections some possible approaches to the adaptive method were discussed. The main idea is to consider a PLL to adjust the receiver clock, based on FIFO level. Although the main concepts behind this technique are simple, determination of the parameters involved (e.g. FIFO size, adjust speed, thresholds limits), is not a trivial task. In order to know how each one of these parameters affects the system performance it was decided to develop a specific simulation programme, described below.

5.1. Generalities

The simulation programme developed may be used to simulate any of the synchronization methods described in section 4.

In all simulations a programmable function is responsible for the generation of the intercell intervals. This will be the main input for the programme. Based on this it generates the write clock pulses.
The processes for generating the various network cell delay jitter patterns include, for the moment, Gaussian and Uniform distributions. Very little information is currently available on the statistics resulting from transmission in real networks. This implies that a considerable amount of work is still required in this area.

Basically, the programme outputs are: the minimum size of the FIFO, the mean frequencies of the read and write clocks, a histogram of FIFO occupancy and a histogram of the output frequency.

These histograms represent, respectively, the percentage of occupation of determinated FIFO zones and the frequency distribution of the recovered clock.

During the total simulation a table is generated, containing the values of some important parameters along the time axis, with programmable resolution.

5.2. Main system parameters

The main system parameters used in current simulations are:

- service bit rate (fo): 34 MHz
- network (line) bit rate (NetCk): 155 MHz
- byte period: Tbyte = (1/ NetCk)*8 = 51 ns
- output frequency range: fo ±20 ppm
- packet (cell) size: 47 byte

With this set of parameters the values in figure 3 are as follows:

Tp = 1 cell = 47 Tbyte
T (avg) = 211.5 Tbyte
td (avg) = 164.5 Tbyte

The standard deviation (STD) is also expressed in Tbyte.

5.3. FIFO size considerations

For each synchronization method the delay jitter distribution determines the minimum size of the receiver buffers necessary to its absorption. Large buffers, however, will have impact on implementation cost and on the total end-to-end delay.
The standardization bodies indicate that the total end-to-end delay (excluding transmission delay) should not exceed 20 ms for real-time interactive services. The provisional time for the transit nodes was established as 1 ms.

The simulations considered here take as standard a FIFO of 32Kbytes. Taking the average filling level as half of FIFO capacity, the average delay on the receiver buffer node is 3.81 ms for a 34 Mbit/s (4.296 Mbytes/s) transmission.

Nevertheless the results of the simulation, indicate that for large delay jitters, greater buffers will be necessary. A relation between the input intercell intervals standard deviation, for the Gaussian and Uniform distributions, and the FIFO size, was established, for the charge pump method. This relation is shown in figure 11.

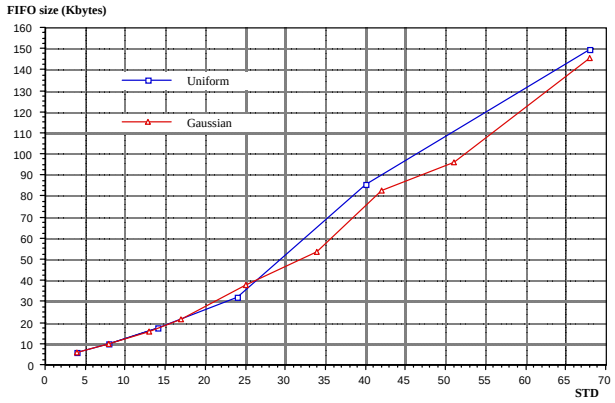


Figure 11. FIFO size versus intercell intervals standard deviation (STD).

5.4. Simulation results

The FIFO level histograms are divided in 34 zones, each one representing 1024 positions of the FIFO, excluding zones 1 and 34, which represent, respectively, the FIFO underflow and FIFO overflow.

The output frequency histograms cover the range of the nominal output frequency (fo) ±20 parts per million (ppm) [6].

Figure 12 shows the histograms for the Charge Pump method. For this method a digital approach was considered since this technique is mainly composed by analog parts.

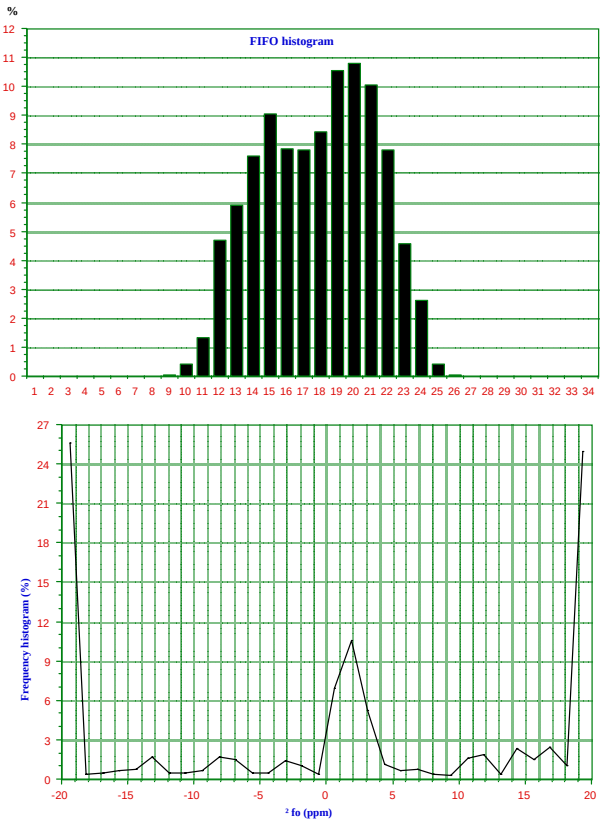


Figure 12. FIFO and frequency histograms for Charge Pump method (STD=15Tbyte).

Figure 12 shows a major disadvantage of this method: the tendency of the RD clock to oscillate between the VCO limits. These produce large oscillations on the RD clock which represent considerable frequency noise in the service provided.

Figure 13 shows a temporal diagram obtained using the Direct method.

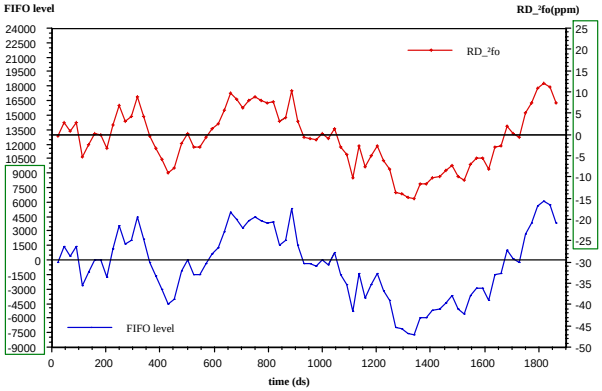


Figure 13. FIFO level and Read frequency temporal diagram, for Direct method (STD=15Tbyte).

This method has the drawback of presenting unnecessary fluctuation on the recovered clock, although FIFO size do not differ very much from the previous method.

Figure 14 shows the histograms for the Hybrid method.

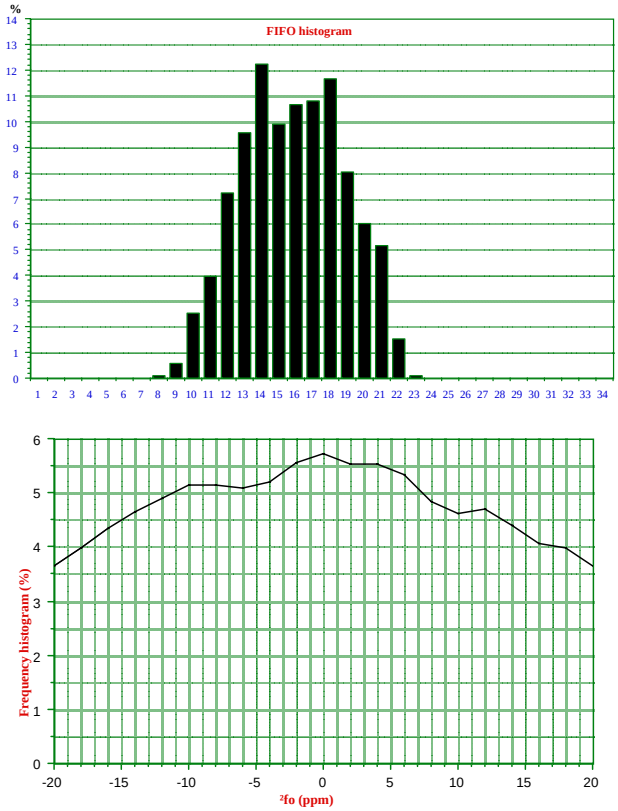


Figure 14. FIFO and frequency histograms for Hybrid method (STD=15Tbyte).

It shows an equilibrated frequency histogram and a reasonable FIFO size. The temporal diagram of figure 15, shows also smooth variations in the recovered clock.

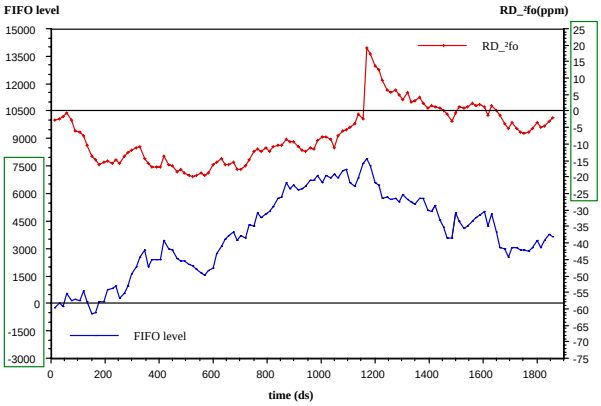


Figure 15. Temporal diagram for FIFO level and RD frequency (STD=15Tbyte).

This seams to be the most appropriated solution for the adaptive clock method. Nevertheless, further study is necessary using the appropriate delay jitter distributions to tune the main parameters and improve the system performance.

6. CONCLUSIONS

The adaptive clock method with an hybrid frequency control algorithm seems to be the best solution for the implementation of synchronization mechanisms for CBR services.

Results are still preliminary, as a better understanding of the system performance, may result from new simulations. This understanding could be achieved using different parameters, and above all, using more realistic delay jitter distributions.

Work will proceed with more simulation studies, with the refinement of the delay jitter distribution routines and the flexible hardware implementation will continue in order to allow the laboratorial testing of the results obtained.

7. REFERENCES

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