energies

MDPI

Article

Balancing the Active Power of a Railway Traction Power Substation with an sp-RPC

Luis A. M. Barros [1,*], António P. Martins [2] and José Gabriel Pinto [1]

[1] ALGORITMI Research Centre/LASI, University of Minho, 4800-058 Guimarães, Portugal
[2] SYSTEC Research Center, University of Porto, 4200-465 Porto, Portugal
* Correspondence: lbarros@dei.uminho.pt

Abstract: The railway system is one of the safest, most efficient, and environmentally friendly means of land transport for people and goods. However, as the demand for mobility has increased, the current railway system has shown some weaknesses, requiring an increase in catenary power in order to be able to supply power to longer trains and faster locomotives, as well as to increase rail traffic. This paper proposes a control algorithm to be implemented in a sectioning post-Rail Power Conditioner (sp-RPC). The sp-RPC is connected to the neutral section between two traction power substations (TPS). With the control algorithm, it is possible to minimize the existing unbalance of the active powers of each TPS. In a regenerative braking condition, this surplus energy can be used to assist the traction of another locomotive on the existing overhead line. In this way, it is possible to increase the capacity of the overhead line. The analysis was performed with computer models using a modular multilevel converter (MMC) topology for the sp-RPC. Quantitative results for different consumption events of the locomotives and the analysis of the response to these variations are presented.

Keywords: electric railway system; neutral section; multilevel converter; regenerative braking; sectioning post-Rail Power Conditioner

Citation: Barros, L.A.M.; Martins, A.P.; Pinto, J.G. Balancing the Active Power of a Railway Traction Power Substation with an sp-RPC. *Energies* **2023**, *16*, 3074. https://doi.org/10.3390/en16073074

Academic Editor: Mario Marchesoni

Received: 1 March 2023
Revised: 21 March 2023
Accepted: 25 March 2023
Published: 28 March 2023

1. Introduction

The constant population increase, forecasting a growth of 38%, reaching a value of 10.88 billion people in 2100 [1], as well as the migration to large urban centers, varying the current ratio from 5/10 people to 7/10 people in 2050 [2], has demonstrated the weakness of the current means of transportation. The railway system is one of the primary means of land transport for transporting people and goods. The electric railway system is energy efficient [3], environmentally friendly [4], safe [5], and capable of responding to the demand for mobility [3]. This leads to the fact that the railway system adds a distinct footprint to the economy of each country, which has encouraged investment in the railway sector.

In order to meet these requirements, different countries aim to increase the speed and size of locomotives. An example is the Portuguese case that intends to increase the number of daily locomotives, speed, and size (up to 750 m). In some cases, this represents a two- to three-times increase in daily energy capacity. Furthermore, with an investment of over EUR 2 billion and over 1000 km of the line under intervention, the aim is to reduce the cost of transport (EURO/km/carriage) and increase catenary capacity (number and length of locomotives) [6]. Another example of an incentive is the European organization Shift2Rail which aims to reduce the life cycle cost of rail transport by up to 50%; double railway capacity; and increase reliability by up to 50% [7,8]. As it turns out, Shift2Rail is committed to making the railway system more efficient, safer, and greener, with a view to "providing, through rail research and innovation, the capabilities needed to achieve a more sustainable, cost-effective mode of transport, high performance, time-oriented, digital and competitive for Europe" [7].

Taking into consideration the ambitions presented as well as the predominance of the 25 kV, 50 Hz railway system, this system is analyzed to identify its weaknesses and possible improvements. In order to avoid power flow between traction power substations (TPS) due to different voltage values or phases, it is necessary to incorporate unpowered railway extensions to create isolation between TPS. These extensions are referred to as neutral sections [9,10]. One of the most used electrification solutions is V/V or *Scott* transformers to feed the overhead lines [11]. This solution allows a better balance in the powers of each phase of the TPS. However, if there is a large unbalance in the consumption values of the locomotives in each catenary, it will accentuate the unbalance between phases of the three-phase system [12]. This problem can be mitigated by incorporating power electronics solutions such as the rail power conditioner (RPC). The RPC allows for minimizing this unbalance [13–15] as well as mitigating other power quality problems [16]. Furthermore, the fact that it is connected close to the TPS allows access to the different voltage and current variables instantaneously, presenting a dynamic response to any type of variation.

These solutions consider each TPS as a microsystem without any interaction with adjacent TPS. In the case of a strong unbalance of the locomotives coupled to the catenaries, it will cause one TPS to operate at its maximum capacity. In contrast, the adjacent TPS operates at a percentage of its capacity. One solution to mitigate this problem is to add a power electronics converter in the neutral section in order to control the power flow between TPS [17]. Hitachi presents in [18] a solution to minimize this problem, called sectioning post-RPC (sp-RPC). The developed sp-RPC was integrated into the neutral section at Ushiku, existing between Fujishiro and Tsuchiura TPS in Japan. The sp-RPC was sized to operate with a nominal voltage of 22 kV and a nominal power of 1.3 MW for each loop. In overload mode, the sp-RPC can operate with a maximum value of 5.3 MW for a maximum period of 1 min, at more than 10 min intervals. The sp-RPC developed by Hitachi also features a static VAr compensator (SVC) functionality up to a maximum value of 1.3 MVAr.

The operating values of the sp-RPC are adjusted according to the hourly forecast and the speed of the locomotives. This solution based on hourly forecast has errors that can reach 6.5% compared to the actual consumption values. This deviation is due, essentially, to delays. Nevertheless, the solution presented is exclusive to regenerative braking events. The authors of [19] present an analysis of an sp-RPC in terms of power losses using the Monte Carlo analysis. The study finds that the railway traffic, as well as the railway extension between the TPS and the neutral section, should be considered. It is intended to determine the best location for the sp-RPC in order to minimize power losses while keeping the two TPS operating at similar active powers.

Regarding the semiconductor market, it is possible to see a breakthrough in the 6500 V blocking voltage barrier. In addition, in this market of high-voltage and power semiconductors, it is possible to see an increase in switching frequencies, enabling the development of more compact solutions. As an example, it can highlight the technology 4H-SiC [20,21] or double implanted MOSFET (DMOSFET) [22] emerging to break the 10 kV barrier. Cree presented a new SiC MOSFET for 10 kV and 240 A, featuring 116 kV/µs transitions during turn-on and 70 kV/µs during turn-off [23]. Another example is a 10 kV and 120 A MOSFET module with a half-bridge configuration for a solid-state power substation. These modules allowed configuring a switching frequency of 20 kHz, contributing to 70% less weight and 50% less volume than a 60 Hz low-frequency transformer [24].

This paper intends to contribute to the study and development of a dynamic control algorithm capable of incorporating an sp-RPC. The control algorithm is based on the average operating power of each TPS. This information is periodically sent to the sp-RPC. This paper is structured as follows: in Section 1, an introduction of the railway power systems is performed, highlighting the state-of-the-art of the RPC connected in neutral sections; in Section 2, the sp-RPC concept is realized, analyzing the possible operation modes; in Section 3, the proposed dynamic control algorithm to be integrated into sp-RPC is presented, taking into account a modular multilevel converter topology of sp-RPC to

interface with a 25 kV/50 Hz electric rail system; in Section 4, the performance of sp-RPC with the proposed algorithm for different locomotive power conditions is analyzed; Section 5 is used for the quantitative analysis of the obtained results; Section 6 is a discussion of the obtained results, presenting the conclusions.

2. sp-RPC Concept

The sp-RPC is a power electronics device connected in the neutral section between two TPS. Knowing the average operating powers of each TPS, the sp-RPC can control the flow of energy between TPS in order to balance the operating powers of each TPS. In this way, overloading at a single TPS is avoided by increasing the capacity of the overhead line. Nevertheless, in the event of regenerative braking, the sp-RPC can use surplus energy to minimize the existing power consumption in the TPS. In the event of zero consumption, this surplus energy is distributed equally between the two TPS. Figure 1 shows the integration of an sp-RPC in a 25 kV railway system.

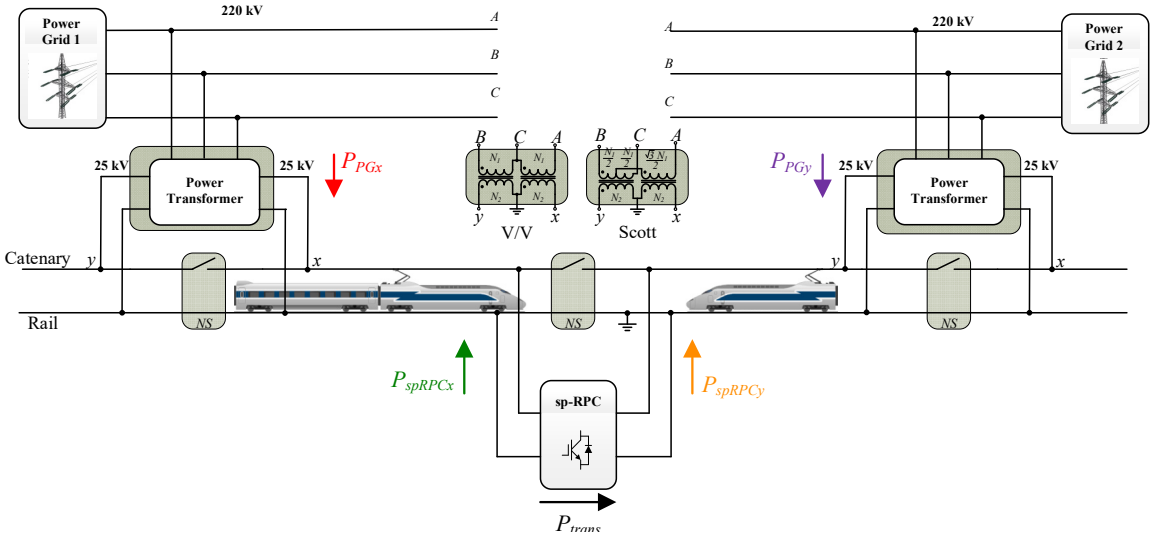

Figure 1. Electric railway system with the integration of the sp-RPC.

The further the locomotive is from the TPS, the greater the voltage drop caused by the impedance of the overhead contact line. In turn, in the event of regenerative braking, the effective value of the overhead contact line voltage rises. These variations caused by the above phenomena can be minimized with the sp-RPC since it is located in the neutral section, at the furthest point from the TPS. This control is accomplished by the reactive energy produced by the sp-RPC, capacitive or inductive, in case of under-voltage or over-voltage. Furthermore, by imposing a more constant root mean square (rms) value of the overhead contact line voltage, it is possible to maintain an equally constant current value for a given power consumption. This ensures a more stable power system.

3. sp-RPC Proposed and Operation Principle

This section presents the entire structure of the sp-RPC for a real application and the proposed control algorithm for balancing the active powers of each TPS. In addition, the other control algorithms responsible for the synchronism with the voltage in the catenary, the output current control, the regulation of the different dc-links as well as the techniques for the sp-RPC are also presented.

3.1. sp-RPC Topology

Considering the 25 kV on the catenary, modularity, and multilevel concepts were used. The proposed topology is shown in Figure 2. As can be seen, different submodules connected in series were used for the high-voltage ac catenary side. The low-voltage dc

side of these submodules is common, which facilitates energy exchange and minimizes the complexity of the control algorithms. In order to provide isolation, the dual-active bridge (DAB) topology was integrated into each submodule. The DAB integrated in each submodule is responsible for the exchange of energy between the common dc-link and the submodule high-voltage dc-link. Nevertheless, the transformation ratio used in the high-frequency transformer of the DAB allows the creation of a common low-voltage dc-link and a dedicated high-voltage dc-link for each submodule. In this way, the number of submodules used can be adjusted as a function of the transformation ratio. This topology features a structure similar to a solid-state transformer (SST), thus incorporating the advantages of an SST. That is, it features a low-voltage dc side and a high-voltage dc and ac side. To better understand the explanation, the power converter connected to the x-side was called *spRPCx*. In turn, the power electronics converter connected to the y-side was called *spRPCy*. Due to the modular structure, it is possible to implement redundant operating mechanisms, increasing the robustness of the system. Although it is outside the scope of this article, some protection and fault tolerance mechanisms are presented in [25].

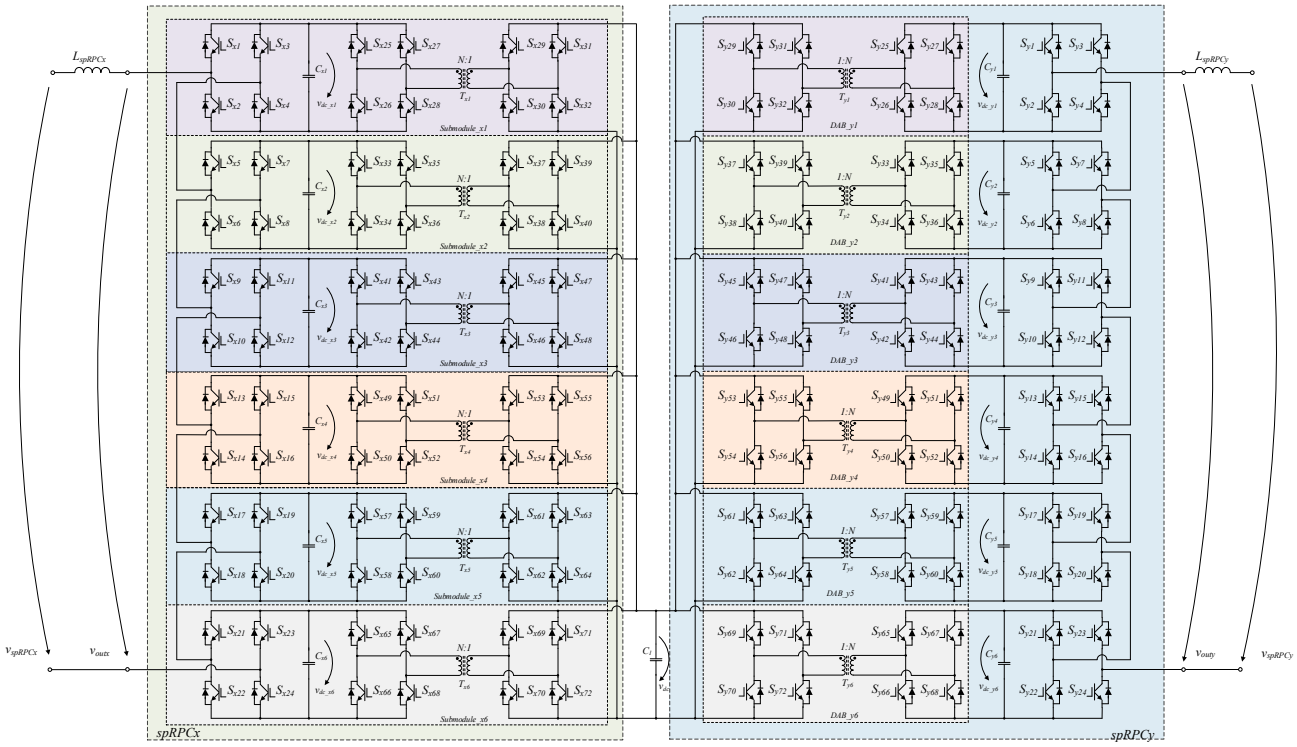

Figure 2. Electrical schematic of the proposed topology for the sp-RPC.

The main parameters of the operating conditions of the sp-RPC and the rest of the railway system are presented in Table 1. The average nominal power for the spRPCx, PspRPCx, and the spRPCy, PspRPCy of 2.5 MW, was considered for the developed simulation model. Regarding the dc-link, a nominal voltage of 1 kV was considered on the common dc-link, v_{dc}, and a voltage of 7 kV on the dedicated dc-link of each submodule, v_{dc_xk}, and v_{dc_yk}, k being the number of the submodule of the x-side or y-side. The value of 1 kV was defined in order to obtain a voltage value on the low-voltage common dc-link. In this way, it would be easier to integrate a solar photovoltaic system and an energy storage system with a lower voltage interface.

Table 1. Main parameters of the topology.

	Variable	Nominal	Unit
Nominal active power for the sp-RPC	P_{sp_RPCx}, P_{sp_RPCy}	2.5	MW
Common dc-Link nominal voltage	V_{dc}	1	kV
Nominal voltage on the dedicated dc-links of the sp-RPC	V_{dc_x1}, V_{dc_x2}, V_{dc_x3}, V_{dc_x4}, V_{dc_x5}, V_{dc_x6}, V_{dc_y1}, V_{dc_y2}, V_{dc_y3}, V_{dc_y4}, V_{dc_y5}, V_{dc_y6}	7	kV
Catenary nominal voltage	v_{PGx}, v_{PGy}	25	kV
sp-RPC output nominal current	i_{spRPCx}, i_{spRPCy}	100	A
Communication frequency between TPS and the sp-RPC	f_{s_PG}	5	Hz
Sampling frequency for the sp-RPC	f_s	50	kHz
Switching frequency for the ac side	f_{sw_spRPC}	1	kHz
Switching frequency for the DAB	$f_{sw\_spRPC\_DAB}$	1	kHz

Moreover, as it is a common dc-link with different power converters connected, it needs high-capacity capacitors, being in the market solutions with a nominal voltage value close to 1 kV. In addition, the sp-RPC was also designed to allow a simple interface of a solar photovoltaic (PV) system as well as a battery energy storage system (BESS). Considering the legislation regarding the maximum limits of a solar photovoltaic system, the 1 kV dc-link was considered a reference value for the realization of the interface with the solar PV and the BESS by using simple non-isolated dc-dc converters topologies. In this way, it is possible to implement power converters, without isolation maintaining a low difference between the voltage levels of the solar PV system or BESS and the common dc-link voltage. Regarding the high-voltage dc-link in each submodule, the 7 kV value was defined considering the number of submodules and the peak value of the catenary voltage. A modulation index of around 80% was also considered.

The communication between the two TPS and the sp-RPC is performed at 5 Hz. For the local variables, the sp-RPC is performed at a sampling frequency of 50 kHz. In turn, a switching frequency of 1 kHz was implemented for each submodule of *spRPCx* and *spRPCy*, considering the DAB and the cascaded full-bridge on the ac side. Table 2 shows some of the values considered for the different components that compose the simulation model of the sp-RPC topology based on SST. The simulation model was developed with the PSIM v9.1 software. The simulations were run on a computer with an i7-8700, 3.2 GHz processor, and 24 GB of RAM, featuring a simulation time of 154 min. The integration time was 1 µs, generating data files with 3.9 GB.

Table 2. Main parameters of the electric components used on the sp-RPC topology based on SST.

	Variable	Value	Unit
Line impedance inductors	L_{PGzx}, L_{PGzy}, $L_{spRPCzx}$, $L_{spRPCzx}$,	2.5 (250 [#1])	mH (mΩ)
Coupling inductor	L_{spRPCx}, L_{spRPCy}	50 (10 [#1])	mH (mΩ)
Capacitance on the dc-link	C_1	200 (10 [#1])	mF (mΩ)
Capacitance on the dc-link	C_{x1}, C_{x2}, C_{x3}, C_{x4}, C_{x5}, C_{x6}, C_{y1}, C_{y2}, C_{y3}, C_{y4}, C_{y5}, C_{y6}	10 (10 [#1])	mF (mΩ)

[#1] Considered as internal series resistance for each component.

Equation (1) was used to determine the coupling inductors, L_{spRPCx} and L_{spRPCy}, of the sp-RPC with the catenary [26]. Determining L_{spRPCk}, with k being equal to x or y depending on the x or y side, requires taking into account the voltage on the dc-link of each submodule.

Being a cascaded converter with 13 levels, the inductor current ripple comes from the transition between adjacent levels with 7000 V (V_{dc_k}) on the V_{dc}. Additionally, considering six submodules with a switching frequency of 1 kHz with a unipolar modulation at the output of each full-bridge, the resulting output frequency of the sp-RPC is 12 kHz (f_{sw}). Finally, a 3% ripple in the inductor (Δi_{spRPCk}) was considered, obtaining a minimum value in the coil of 48.6 mH. This value was rounded off to 50 mH

$$L_{spRPCk} = \frac{V_{dc\_k}}{\left(4\Delta i_{spRPCk} f_{sw}\right)}, \text{ [being } k \text{ equal to } x \text{ or } y\text{]}, \quad (1)$$

Equation (2) was used to size the capacitors in each submodule [27]. The value of α (=0) represents the operating power factor, v_{spRPCk} (25,000 V) the rated voltage of the sp-RPC at the point of connection to the catenary, and i_{spRPCk} (100 A) the maximum rated current of the sp-RPC. In turn, ω (2 π 50 rad/s) relates the frequency of the catenary voltage, N (6) is the number of submodules, V_{dc} (7000 V) is the voltage at the dc-link of each submodule, and the desired voltage ripple is defined by Δv_{dc} (20 V peak to peak). The value obtained was 9.5 mF and was adjusted to 10 mF. The capacitor C_1 was adjusted with the aid of the simulation results until the best response was obtained.

$$C_k = \frac{(1-\alpha) v_{spRPCk} i_{spRPCk}}{\omega N V_{dc} \Delta v_{dc}}, \text{ [being } k \text{ equal to } x \text{ or } y\text{]}, \quad (2)$$

3.2. Sp-RPC Control Algorithm

For the correct functioning of the sp-RPC, it is necessary to constantly monitor the different variables of the system. The sp-RPC controller has real-time access to the local variables and the active power in each TPS in intervals of 0.2 s (f_{S_PG} = 5 Hz). Due to the inherent concept, the sp-RPC will have to conciliate the instantaneous monitoring of the operating variables of the power electronic converters, with periodic monitoring, caused by the time delay of sending information, of the active powers of each TPS. In this way, throughout this topic, all the implemented algorithms are presented in order to provide a continuous operation of the sp-RPC. This topic starts by analyzing the different variables to be controlled, the interaction between different control algorithms, the determination of the reference values for each power electronics converter, and the control signals for the power semiconductors.

Figure 3 shows a simplified electrical schematic of the proposed topology for integrating a full scale sp-RPC. In the represented electrical diagram, it is possible to verify not only the constitution of each power electronics converter but also the measurement points of the different variables, currents, and voltages.

For the correct operation of sp-RPC, the entire algorithm must present a given sequence of data processing, as well as identify the interaction of variables between different blocks of data processing. Figure 4 shows the main implemented control algorithms, highlighting the input and output variables. Nevertheless, it is possible to verify a sequence of data processing, starting with the acquisition of instantaneous voltage and current values from different points of the sp-RPC, going through to determine the average values of both voltage and power required. Then, based on the combination of average and instantaneous values with specific control functions, it is possible to determine the reference operating powers for each sp-RPC side, the *spRPCx* and *spRPCy*. These values are later used to adjust the control signals in order to minimize operating errors compared to the reference values.

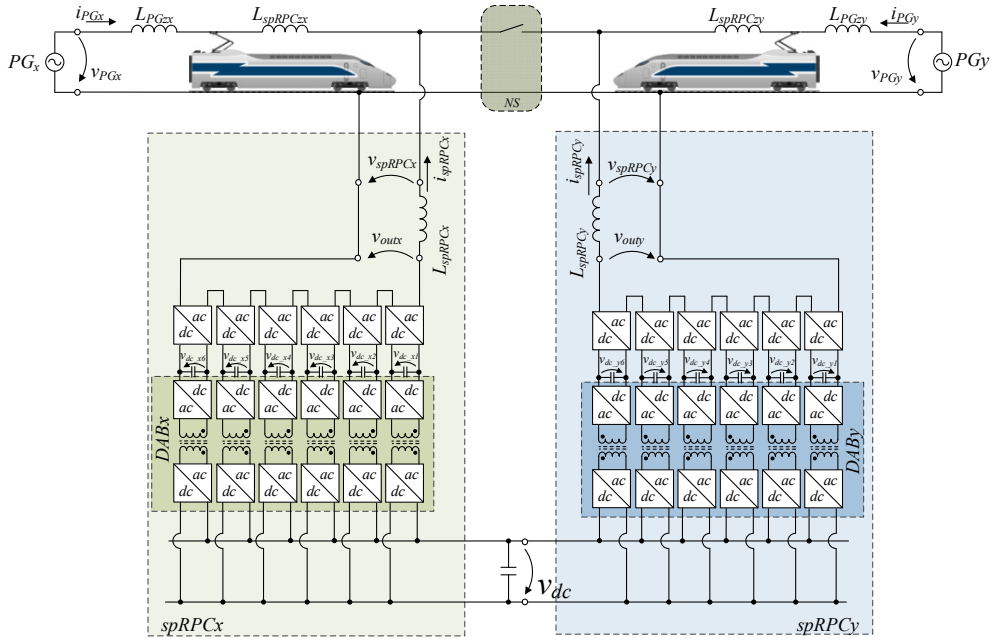

Figure 3. Simplified schematic of the proposed topology for the sp-RPC, highlighting the measurement points for the variables involved in the control algorithms.

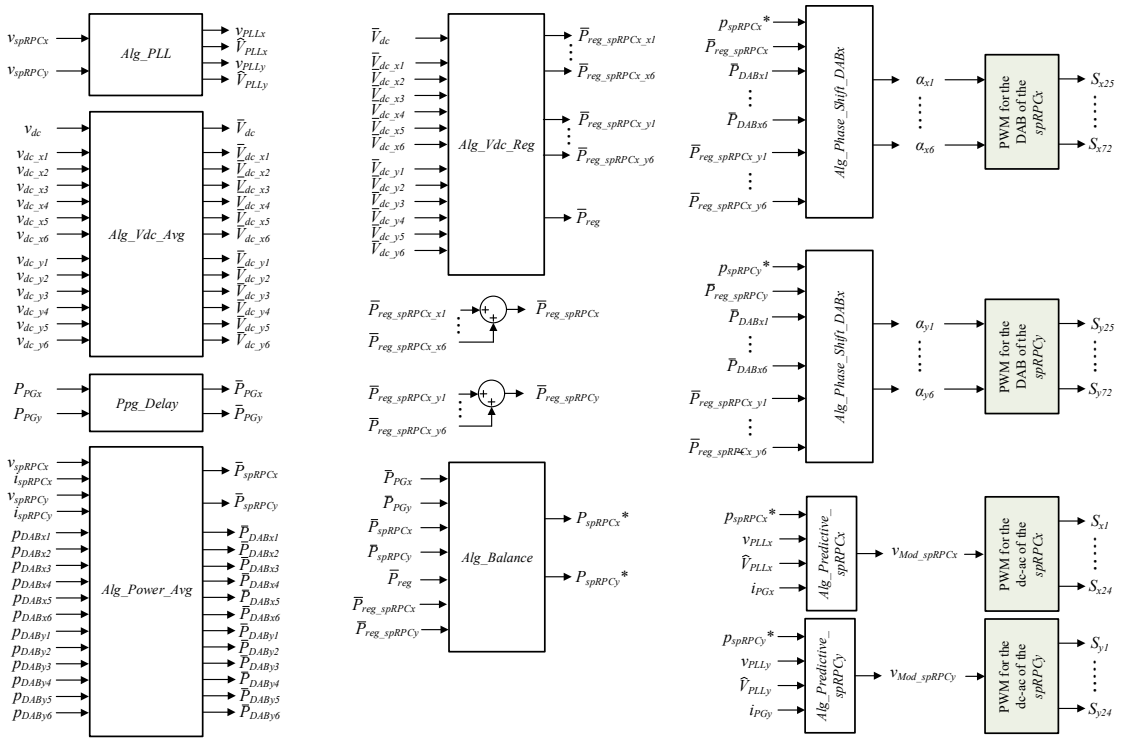

Figure 4. Block diagram of all the control algorithms implemented for the proposed sp-RPC.

For the correct functioning of the implemented algorithm, it is necessary to initially determine the average voltage and power values. This way, the control algorithm *Alg_Vdc_Avg* determines the average values of the voltages in the dc-links that compose the sp-RPC. In turn, the control algorithm *Alg_Power_Avg* is responsible for performing the communication between the TPS and providing the average operating power of each one. Finally, as the last control block for the input variables, the phase-locked loop (PLL) control algorithm, *Alg_PLL*, is responsible for synchronizing the sp-RPC with the fundamental component of each voltage catenary.

Once all the instantaneous input variables have been processed, it is necessary to define the operating reference values for each power electronics converter. In this way, based on the *Alg_Vdc_Reg* function, one starts by determining the regulating power in order to keep the voltages of the dc-links regulated. The sum of the regulating powers *Preg_spRPCx* for the *spRPCx* and *Preg_spRPCy* for the *spRPCy*, are later used in the control algorithm *Alg_Balance*. This block, *Alg_Balance*, is responsible for managing and determining the reference active power values for the different power electronics converters.

Once all the operating reference values have been determined, it is necessary to activate the different power semiconductors that compose the power electronics converters based on the modulation technique used. For the SST, the control is done by the phase-shift technique, with the control algorithm *Alg_Phase_Shift_DABx* responsible for generating the phase angles for each SST that constitutes the *spRPCx*. At the same time, the *Alg_Phase_Shift_DABy* is responsible for generating the phase angles for each SST that constitutes the *spRPCy*. These values are later used for the direct drive of semiconductors *Sx25* to *Sx72* of *spRPCx* and *Sy25* to *Sy72* of *spRPCy*. For the power converters connected to the catenary, a predictive control algorithm is used in order to determine a modulation wave for the pulse width modulation (PWM) signals. In this way, the *Alg_Predictive_spRPCx* function is responsible for generating a modulating wave *vMod_spRPCx*, while *Alg_Preditice_spRPCy* is responsible for generating a modulating wave *vMod_spRPCy*. These modulating waves are later compared with carrier waves for the activation of semiconductors *Sx1* to *Sx24* of *spRPCx* and semiconductors *Sy1* to *Sy24* of *spRPCy*. It should be mentioned that in order to impose a better power balance between submodules, the phase-shift carrier PWM technique was implemented.

Figure 5 shows the simplified flow diagram of the implemented algorithm. After the start of the operation, the operating conditions of the two TPS must be checked. After acquiring P_{PGx} and P_{PGy}, the next step involves determining the reference active power P_{spRPCx}* and P_{spRPCy}*. This determination is based on Equations (6) and (7), explained in the next topic. Next, these values are used to determine the i_{spRPCx}* and i_{spRPCy}* operating currents (based on Equations (8) and (9), also explained in the following topic). Once this sequence is complete, it is checked if an updated value has been received in the TPS operating power. If so, the average values of the TPS are updated, repeating the entire process. Otherwise, the values of P_{PGx} and P_{PGy} are maintained, updating P_{spRPCx}* and P_{sRPCy}* only based on the instantaneous operation values of sp-RPC.

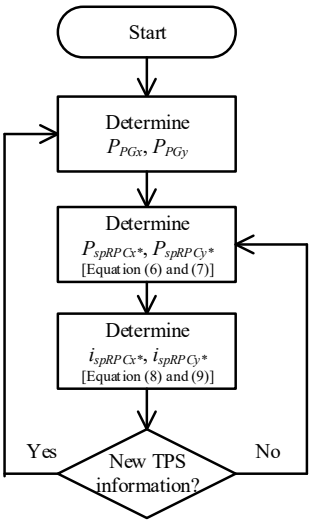

Figure 5. Simplified flowchart of the sp-RPC control algorithm.

3.2.1. Dynamic sp-RPC Control

In this topic, the constitution of the *Alg_Balance* control block is presented below. For the correct functioning of the system dynamically, it is necessary to continuously acquire the active power values on each side of the TPS. That is the average value of the TPS on the x-side, P_{PGx}, and the y-side, P_{PGy}. Due to the distance from the TPS to the sp-RPC, these parameters are updated periodically. In this way, the determination of the average value of the operating power between the two TPS, P_{avg}, represented in Equation (3), is affected by the time of sending this information (200 ms).

$$P_{avg} = \left(P_{PGx} + P_{PGy}\right)/2, \tag{3}$$

Once the P_{avg} value has been determined, it is necessary to determine the desired energy transfer between TPS and P_{trans}. That is, if it is intended to absorb energy from the TPS on the x-side and inject it into the y-side or vice versa. For this, Equation (4) is necessary to determine the active power of the *spRPC* on the y-side, P_{spRPCy}. By adding P_{PGy} to P_{spRPCy} and subtracting the value of P_{avg}, it is possible to verify the intended energy flow. If a positive result is obtained, the power flow is carried out from the x-side TPS to the y-side TPS. Otherwise, the energy flow is carried out in the opposite way.

$$P_{trans} = -P_{Avg} + P_{PGy} + P_{spRPCy}, \tag{4}$$

Once the P_{trans} value is determined, it remains to define the average operating powers for *spRPCx* and *spRPCy*, P_{spRPCx}* and P_{spRPCy}*, respectively. Equation (5) determines the value of P_{spRPCx}*, while Equation (6) is used for the P_{spRPCy}*.

$$P_{spRPCx}{}^{*} = -P_{trans}, \tag{5}$$

$$P_{spRPCy}{}^{*} = P_{trans}, \tag{6}$$

These values presented are limited to the maximum and minimum values desired for the operating powers of each power converter, *spRPCx,* and *spRPCy*. However, it is still necessary to consider the regulating powers determined in order to keep the voltages at all dc-links regulated. P_{reg} represents the regulating power to keep the common dc-link regulated. In turn, P_{reg_spRPCx} represents the regulating power to keep all the dedicated dc-links of the *spRPCx*, while P_{reg_spRPCy} represents the regulating power to keep all the dedicated dc-links of the *spRPCy*. The determination of these regulating powers is analyzed in the following topic. Once limited, the portion of the regulating powers used to regulate the dc-links that constitute the full sp-RPC system, as represented in Equation (7), is subsequently added.

$$P_{spRPCx}{}^{*} = P_{spRPCx}{}^{*} - \left(P_{reg} + P_{reg_{spRPCx}} - P_{reg_{spRPCy}}\right), \tag{7}$$

Once the reference values for the active power of P_{spRPCx}* and P_{spRPCy}* are set, it is necessary to determine the reference current values i_{spRPCx}* and i_{spRPCy}*. Equation (8) is used to determine i_{spRPCx}*, using the values determined by the PLL control algorithm (*Alg_PLL*): $\hat{V}_{PLLx}$ (the peak value) and v_{PLL} (sinusoidal waveform with amplitude equal to 1). The factor of 2 arises from the ratio of the peak and rms value of the voltage and current values. An analogous approach is taken in Equation (9) to determine i_{spRPCy}*.

$$i_{spRPCx}{}^{*} = \frac{2 \times P_{spRPCx}{}^{*} \times v_{PLLx}}{\hat{V}_{PLLx}}, \tag{8}$$

$$i_{spRPCy}{}^{*} = \frac{2 \times P_{spRPCy}{}^{*} \times v_{PLLy}}{\hat{V}_{PLLy}}, \tag{9}$$

3.2.2. DC-Link Regulation

For the sp-RPC to synthesize the desired output current, the voltages on the dc-links must present a minimum value. This value depends not only on the peak voltage of the catenary but also on the topology of the power electronics converter. In this specific case, it is necessary to consider the combination of the different voltage values of each submodule that constitutes the sp-RPC, and the total value must exceed the peak voltage of the catenary. Thus, the control algorithm *Alg_Vdc_Reg* is responsible for determining the necessary regulating power value for voltage regulation of each capacitor of the different dc-links. Considering this premise, it is necessary to regulate all the dc-links that compose the sp-RPC.

Initially considering the common dc-link, it is necessary to determine the average voltage value before proceeding with implementing a sliding window average. Then, the voltage error is obtained by making the difference between the desired voltage reference value, V_{dc}*, and the average value obtained, V_{dc}. Finally, the *V_dc_error* portion is used with a PI controller in order to determine the final regulating power *Preg*. The representative block diagram of the algorithm implemented for regulating the dc-link voltage is shown in Figure 6.

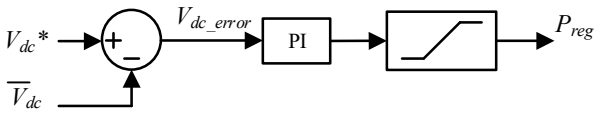

Figure 6. Block diagram of the control algorithm responsible for regulating the voltage on the common dc-link.

Regarding the capacitors that compose each SST submodule, it is necessary to apply the same methodology for regulating their voltage. Figure 7 shows a block diagram illustrating the algorithm performed for regulating the dc-link of each SST that makes up the *spRPCx*. The sum of each plot represents the total regulated power, P_{reg_spRPCx}, that the *spRPCx* needs to keep all the voltage on all the dc-link regulated. The same methodology is replicated for *spRPCy*.

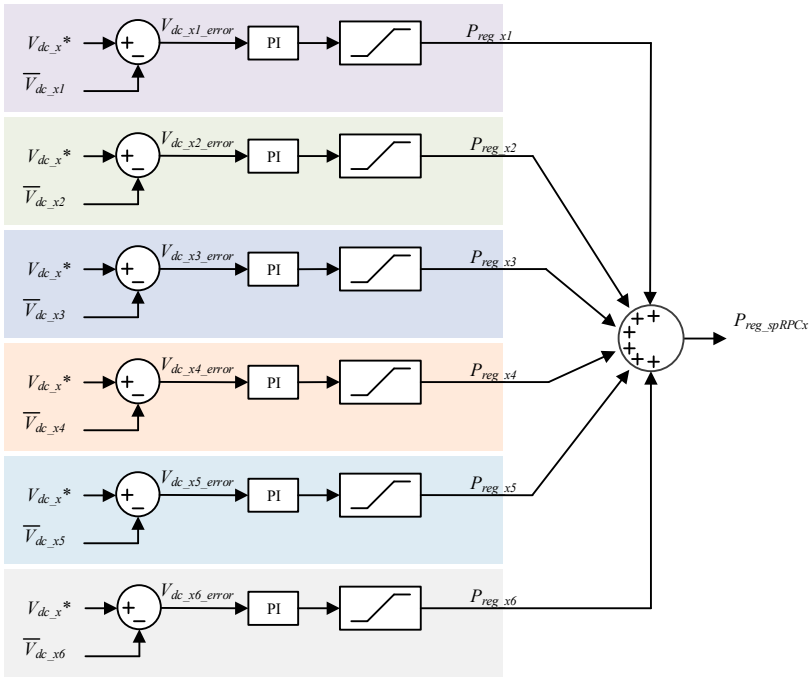

Figure 7. Block diagram of the control algorithm responsible for regulating the different dc-link voltages on the *spRPCx*.

The next step is determining P_{spRPCx}* and P_{spRPCy}* based on the previous Equations (7) and (6). Once P_{spRPCx}* has been determined, it is necessary to determine the average operating power for each submodule in order to maintain not only the regulation of the dc-link but essentially impose an equal power distribution between submodules. In this way, the power value is defined as a function of the number of existing submodules, dividing P_{spRPCx} by N. The resulting portion is then added to the representative regulating power of each submodule, thus creating a reference power. The average operating power of each submodule is then compared with the respective average power, resulting in an error value. Finally, this value is used in a proportional-integral (PI) controller in order to generate a phase angle capable of minimizing the error obtained, as illustrated in Figure 8.

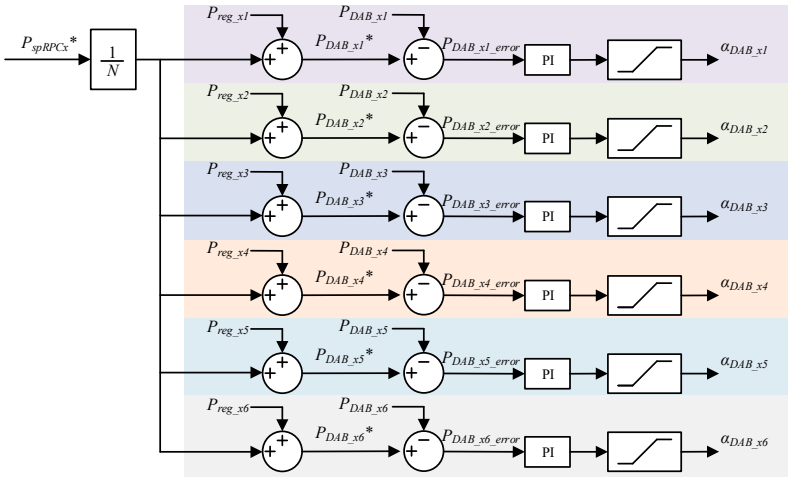

Figure 8. Block diagram of the control algorithm responsible for balancing the power between the different submodules of the *spRPCx*.

3.2.3. PLL Control Algorithm

In order to allow a continuous operation of the sp-RPC when connected to the catenary, the control system must be synchronized with the fundamental component of the voltage in each catenary. With this synchronism, it is possible to control the power factor of the sp-RPC. Analyzing the literature, it is possible to identify several synchronization techniques [28–30]. This study was focused on the synchronization technique called PLL. More specifically, the technique presented by Karimi et al. [28]. This PLL technique has been used in previous projects, showing good performance.

Briefly, the PLL technique allows the detection of the phase and amplitude of the fundamental component of the measured signal, resulting in a sinusoidal and in-phase signal. Figure 9 shows the representative block diagram of the constitution of the PLL technique, consisting of a phase detector, a filter, and a voltage-controlled oscillator.

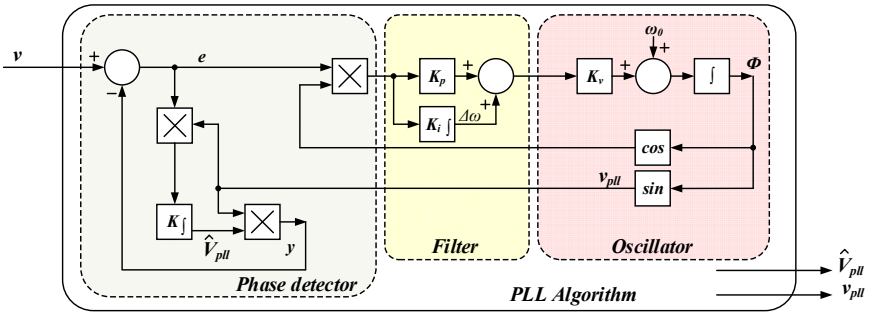

Figure 9. Block diagram of the PLL control algorithm (based on [28]).

The phase detector is responsible for measuring the error between the input and output signals. The resulting signal is used in a low-pass filter that forms the filter block. Finally, the oscillator is responsible for originating an output signal synchronized to the fundamental component of the input signal.

This structure provides access to two signals: v_{pll} and V_{pll}. The v_{pll} signal corresponds to a unitary signal and is synchronized with the fundamental component of the catenary. In turn, V_{pll} represents the amplitude of the input signal. The v_{pll} signal can be used as a reference sinusoidal signal for current control. V_{pll} will allow the amplitude of the reference current to be determined, knowing the desired operating power.

3.2.4. Predictive Current Control Algorithm

The predictive current control technique is based on the electrical model of the system in order to predict the behavior of the variables to be controlled. This prediction allows a dynamic and fast response in the current control. Furthermore, this concept does not require gain adjustment at the control level, presenting a better system performance regardless of the desired output current waveform. However, it requires correct analysis of the existing electrical model. A simplified structure of the predictive algorithm and its interaction with the electrical system is shown in Figure 10.

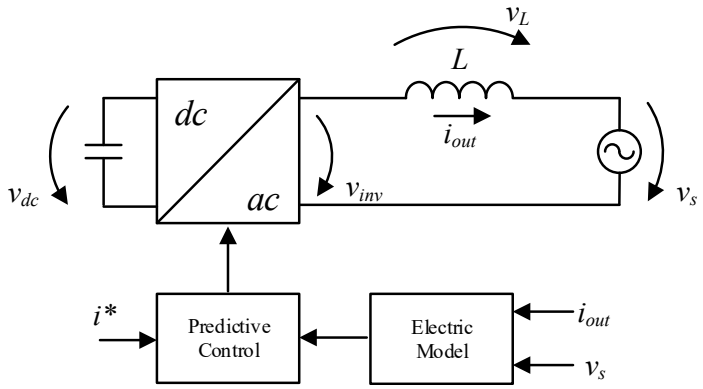

Figure 10. Simplified diagram of the electrical system for the predictive control algorithm.

In the literature, there are several analyses of the electrical model considering different passive filters between the power electronics converter and the ac-link system. The more complex the filter used between the power electronics converter and the ac system, the more complex the electrical model. Consequently, the greater the complexity of the calculations performed. However, with microcontrollers, process accelerators can be used to increase the processing speed.

Considering the multilevel system and the operating voltages of the catenary, the analysis of the control algorithm was performed considering only the coupling inductor. Considering the model in Figure 10, the system equation can be deduced according to Equation (10).

$$v_{inv} = v_L + v_s, \tag{10}$$

Knowing that the difference between the reference current, i^*, and the output current, i_{out}, is the error current, i_{error}, Equation (11) was deduced by introducing the characteristic equation of the inductor v_L.

$$v_{inv} = L\frac{d(i^* - i_{error})}{dt} + v_s, \tag{11}$$

In order to cancel the error current portion, it is multiplied by -1, thus obtaining Equation (12).

$$v_{inv} = L\frac{di^*}{dt} + L\frac{di_{error}}{dt} + v_s, \tag{12}$$

In order for the digital microcontroller to process the equation, it is necessary to convert it to the discrete domain. Then, applying the forward Euler method [31,32] with a sampling frequency given by $f_a = 1/T_a$, it is possible to obtain the equation:

$$v_{inv}[k+1] = v_s[k] + \frac{L}{T_a}(i^*[k] - i^*[k-1] + i_{error}[k] - i_{error}[k-1]), \quad (13)$$

Considering that $i_{error}[k]$ defines the difference between $i^*[k]$ and $i_{out}[k]$, Equation (13) can be simplified to Equation (14).

$$v_{inv}[k+1] = v_s[k] + \frac{L}{T_a}(2i^*[k] - i^*[k-1] - i_{out}[k] - i_{error}[k-1]). \quad (14)$$

3.2.5. PWM Techniques for Multilevel Converter

In order to control the output current of a multilevel converter (MLC), it is necessary to correctly drive the power semiconductors. These PWM signals originated from the comparison between modulator and carrier waves. The greater the number of voltage levels that the MLC can synthesize, the more complex the implementation of the PWM signals becomes. The number of carrier waves increases with the number of voltage levels generated by the MLC. The arrangement of the carrier waves as well as the sequence of the generated signals will affect the performance of the MLC.

Barros et al. present in [25] a study and analysis of different PWM techniques applied to MLC. The analysis is done for (i) level-shift PWM technique; (ii) phase-shift carrier; (iii) hybrid carrier. For each group, the different variants are also analyzed in order to minimize the circulating currents between submodules, lower the harmonic content and increase the balance of operating powers between submodules. The preferred techniques for each MLC topology are also identified. Considering the results presented, as well as the concept of using ac-side cascaded full-bridge converters, the phase-shift carrier technique is the most suitable.

The phase-shift carrier technique shifts the carrier waveforms horizontally. All carrier waves have the same amplitude, frequency, and mean value. They, in turn, present a phase-shift between them of $2\pi/n$, as represented in Figure 11. The value of n is adjusted by considering the number of arms the MLC topology presents.

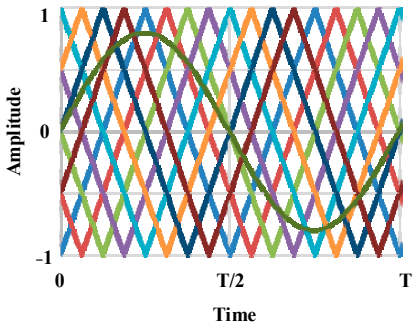

Figure 11. Illustration of the carrier and modulation waveforms for the phase-shift carrier technique.

Considering several cascaded full-bridges, this control technique can impose a similar operating power between each full-bridge. In this way, the concept of modularity is maintained. Analyzing its implementation in a microcontroller, there are solutions on the market, as is the case of Texas Instruments, whose microcontrollers present dedicated peripherals to perform the desired horizontal displacement [25].

4. sp-RPC Simulation Results

In this topic, the different simulation results obtained are presented, considering the real-scale simulation model of sp-RPC. This analysis considered the different operating

modes, as well as the different operating conditions caused by the loads. In turn, the system robustness was also analyzed considering different operating conditions of the loads, different operating inputs and outputs, load transients, and regenerative braking.

4.1. Case Analysis Scenarios

For a comparative analysis of the performance of the sp-RPC, the different loads considered are presented in Figure 12, highlighting the imposed operating conditions. The analysis of each figure is presented in the following topics:

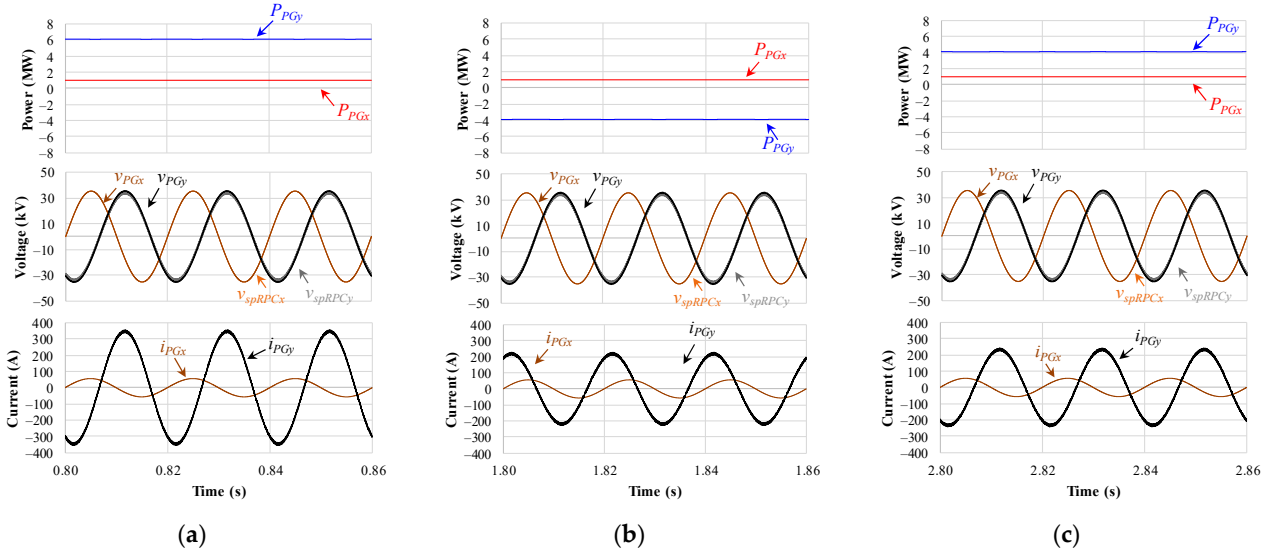

Figure 12. Simulation results of the power in each TPS, P_{PGx} and P_{PGy}, the voltages, v_{PGx}, v_{PGy}, v_{spRPCx} and v_{spRPCy}, and currents, i_{PGx} and i_{PGy}, for different load conditions: (**a**) P_{Loadx} = 0.998 MW and P_{Loady} = 6.12 MW; (**b**) P_{Loadx} = 0.998 MW and P_{Loady} = −3.88 MW; (**c**) P_{Loadx} = 0.998 MW and P_{Loady} = 4.12 MW.

- In Figure 12a, the load on the x-side presents an average active power P_{Loadx} = 0.998 MW, while the load on the y-side presents P_{Loady} = 6.12 MW. Regarding the currents, it is possible to verify that i_{PGx} presents an amplitude of 56.54 A, while i_{PGy} presents an amplitude of 357.2 A. This case represents the event (i);
- In Figure 12b, the load on the x-side presents an average active power P_{Loadx} = 0.998 MW, while the load on the y-side presents P_{Loady} = −3.88 MW. Regarding the currents, it is possible to verify that i_{PGx} presents an amplitude of 56.54 A, while i_{PGy} presents an amplitude of 228.4 A. This case represents the event (ii);
- In Figure 12c, the load on the x-side presents an average active power P_{Loadx} = 0.998 MW, while the load on the y-side presents P_{Loady} = 4.12 MW. Regarding the currents, it is possible to verify that i_{PGx} presents an amplitude of 56.54 A, while i_{PGy} presents an amplitude of 243 A. This case represents the event (iii).

4.2. Traction Power Substation Active Power Analyses

In Figure 13a, it is possible to verify that P_{PGx} and P_{PGy} initially present different values, and at 0.4 s, the proposed control algorithm is activated, being able to verify that P_{PGx} and P_{PGy} converge to an average value of 3.6 MW. At instant 1 s, the locomotive on the y-side starts braking ($P_{Loady} < 0$), generating a new unbalance between P_{PGx} and P_{PGy}. When the control algorithm updates the reference values for the sp-RPC, it is possible to verify that P_{PGx} and P_{PGy} converge to similar values, presenting an average value of −1.4 MW. Finally, at the instant 2 s, the locomotive on the y-side starts to accelerate, P_{Loady} varies again, and as soon as the reference values are updated, it is possible to verify that the average values of P_{PGx} and P_{PGy} converge again, presenting an average value of 2.6 MW. In Figure 13b, it is possible to see that the powers P_{spRPCx} and P_{spRPCy} always follow the

reference values P_{spRPCx}* and P_{spRPCy}*. Figure 13c shows the variation of the dc voltage on the different dc-links over time. Regarding the common dc-link, it is possible to verify that the v_{dc} remains regulated to an average value of 1 kV. In turn, the remaining dc voltages that compose each submodule, from v_{dc_x1} to v_{dc_x6} and from v_{dc_y1} to v_{dc_y6}, are also regulated to an average value of 7 kV.

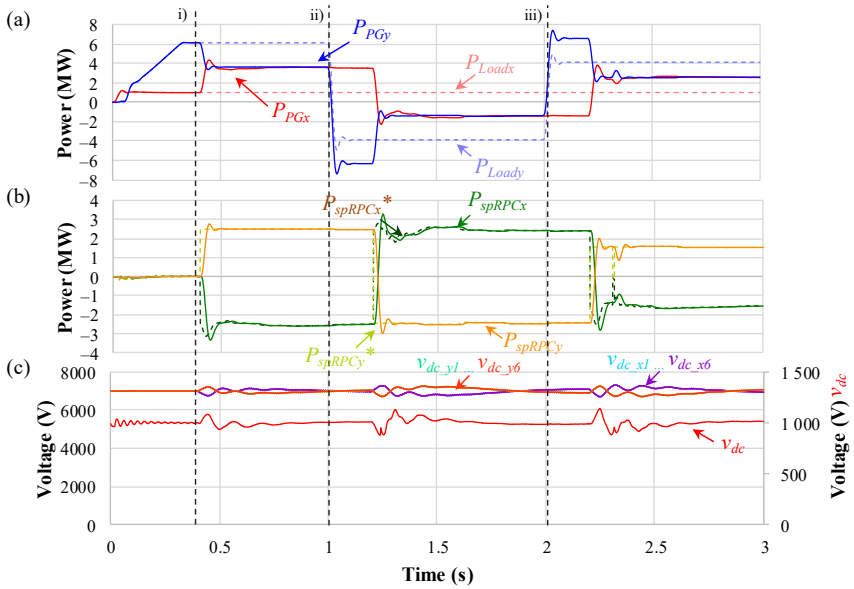

Figure 13. Evolution of active powers and voltages: (**a**) variation of the load power, P_{Loadx} and P_{Loady}, and the active power on each TPS, P_{PGx} and P_{PGy}; (**b**) variation of sp-RPC active power, P_{spRPCx} and P_{spRPCy}, as well as the reference values, P_{spRPCx}* and P_{spRPCy}*; (**c**) variation of the common dc-link voltage, v_{dc}, variation of the voltage of the dc-link on each submodule, v_{dc_x1} to v_{dc_x6}, and v_{dc_y1} to v_{dc_y6}.

4.3. Detailed Analysis of the sp-RPC

Figure 14 presents a more detailed view of the system operation between the time interval from 0.3 s to 0.6 s in Figure 13. In Figure 14a, it is possible to verify the voltages of each TPS, v_{PGx}, and v_{PGy}, as well as the voltages on each side of the sp-RPC, v_{spRPCx}, and v_{spRPCy}. Moreover, it is possible to check the dc-link voltages from v_{dc_x1} to v_{dc_x6} and from v_{dc_y1} to v_{dc_y6}, showing an initial disturbance caused by the start of the operation but maintaining a constant desired average value of 7 kV. In Figure 14b, the multilevel voltages v_{outx} and v_{outy} are presented, being able to verify the 13 voltage levels generated by the modular power converter based on SST. Nevertheless, it is also possible to see that despite the initial perturbation, v_{dc} remains regulated at a value of 1 kV. Finally, by analyzing Figure 14c, it is possible to verify that as soon as the sp-RPC starts operating, synthesizing i_{spRPCx} and i_{spRPCy}, it was possible to equalize the amplitudes of the i_{PGx} and i_{PGy}.

Continuing with the analysis, it is possible to verify in more detail in Figure 15 the operation of the system between the time interval from 0.95 s to 1.25 s, representative of event (ii) in Figure 13. In Figure 15a, it is possible to verify the voltages of each TPS, v_{PGx} and v_{PGy}, as well as the voltages on each side of the sp-RPC, v_{spRPCx} and v_{spRPCy}. Moreover, it is possible to see that v_{dc_x6} has an average value of 7.02 kV, while v_{dc_y6} has an average value of 6.99 kV during this interval. The remaining voltages have similar values of the dc-link on the same side. In Figure 15b, the multilevel voltages v_{outx} and v_{outy} are displayed, as well as it is also possible to see that v_{dc} shows an average value of 1.0 kV during this interval. Finally, by analyzing Figure 15c, it is possible to verify that until the instant 1 s, the amplitudes of i_{PGx} and i_{PGy} were almost similar, obtaining a maximum amplitude value of 205.5 A and 213.0 A. At this time, i_{spRPCx} has a maximum value of 148.4 A, while i_{spRPCy} has a maximum value of 142.6 A. However, with the locomotive on the y-side starting regenerative braking ($P_{Loady} < 0$), the amplitude of i_{PGy} increases to a

maximum value of 364.8 A, and a new unbalance appears. At instant 1.2 s, the proposed control algorithm updates the operation reference values, as can be seen with the amplitude change of the i_{spRPCx} and i_{spRPCy}, being able to verify that i_{PGx} and i_{PGy} converge again to similar amplitude values.

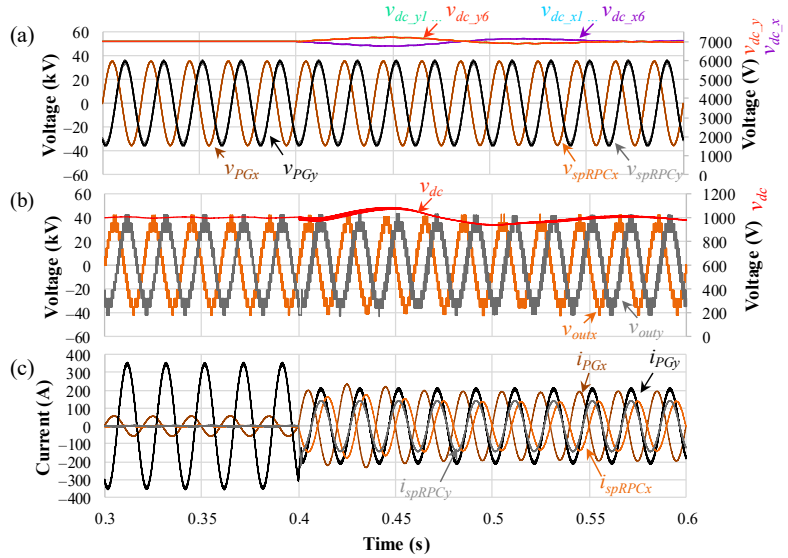

Figure 14. Detailed real-scale simulation results during the time interval from 0.3 s to 0.6 s: (**a**) the voltages on each TPS, v_{PGx} and v_{PGy}, the output voltages of the sp_{RPCx} and sp_{RPCy}, v_{spRPCx} and v_{spRPCy}, and voltages on the dc-link of each submodule, v_{dc_x1} to v_{dc_x6}, and v_{dc_y1} to v_{dc_y6}; (**b**) the multilevel voltage of the *spRPCx* and *spRPCy*, v_{outx} and v_{outy}, and the voltage of the common dc-link voltage, v_{dc}; (**c**) the currents on each TPS, i_{PGx} and i_{PGy}, and the output currents of the sp-RPC, i_{spRPCx} and i_{spRPCy}.

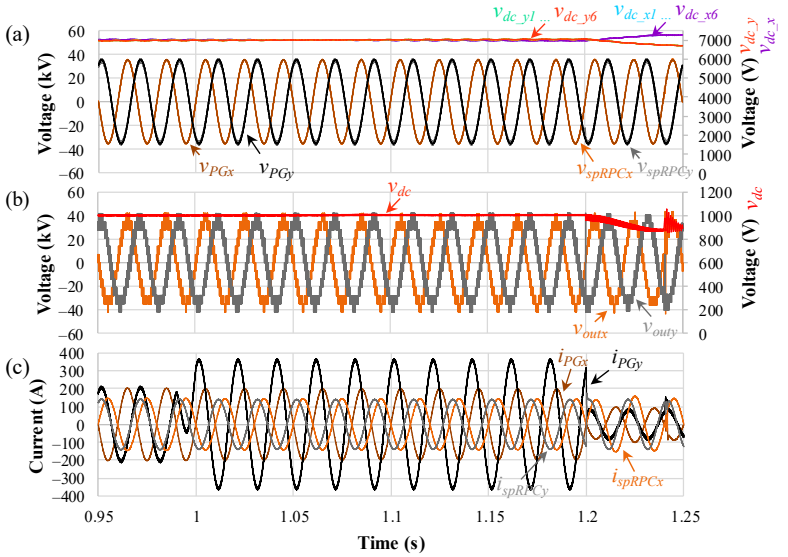

Figure 15. Detailed real-scale simulation results during the time interval from 0.95 s to 1.25 s: (**a**) the voltages on each TPS, v_{PGx} and v_{PGy}, the output voltages of the sp_{RPCx} and sp_{RPCy}, v_{spRPCx} and v_{spRPCy}, and voltages on the dc-link of each submodule, v_{dc_x1} to v_{dc_x6}, and v_{dc_y1} to v_{dc_y6}; (**b**) the multilevel voltage of the *spRPCx* and *spRPCy*, v_{outx} and v_{outy}, and the voltage of the common dc-link voltage, v_{dc}; (**c**) the currents on each TPS, i_{PGx} and i_{PGy}, and the output currents of the sp-RPC, i_{spRPCx} and i_{spRPCy}.

Figure 16 shows the result during the time interval from 1.95 s to 2.25 s, representative of event (iii) in Figure 13. Figure 16a shows it is possible to verify the voltages of each

TPS, v_{PGx} and v_{PGy}, as well as the voltages on each side of the sp-RPC, v_{spRPCx} and v_{spRPCy}. Moreover, it is possible to see that v_{dc_x6} has an average value of 7.06 kV, while v_{dc_y6} has an average value of 6.94 kV during this interval. The remaining voltages have similar values of the dc-link on the same side. In Figure 16b, the multilevel voltages v_{outx} and v_{outy} are displayed, and it is also possible to see that v_{dc} shows an average value of 0.99 kV during this interval. Finally, by analyzing Figure 16c, it is possible to verify that until the instant 2 s, the amplitudes of i_{PGx} and i_{PGy} were similar, obtaining a maximum value of 81.15 A and 85.51 A, respectively. At this time, i_{spRPCx} has a maximum value of 137 A, while i_{spRPCy} has a maximum value of 68.61 A. However, with the locomotive on the y-side starting to accelerate, varying the $P_{Loadx} > 0$, i_{PGx} increases to a maximum amplitude value of 381 A, and a new unbalance appears. At the time instant 2.1 s, the proposed control algorithm updates the operation reference values, as can be seen with the amplitude change of the i_{spRPCx} and i_{spRPCy}, being able to verify that i_{PGx} and i_{PGy} converge again to similar amplitude values.

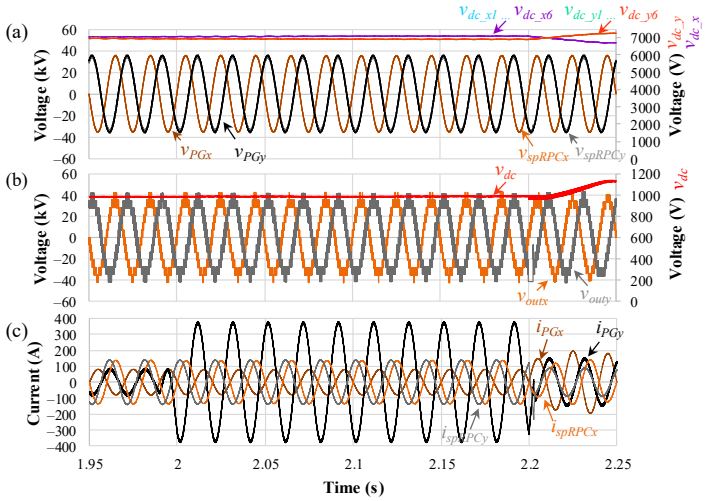

Figure 16. Detailed real-scale simulation results during the time interval from 1.95 s to 2.25 s: (**a**) the voltages on each TPS, v_{PGx} and v_{PGy}, the output voltages of the sp_{RPCx} and sp_{RPCy}, v_{spRPCx} and v_{spRPCy}, and voltages on the dc-link of each submodule, v_{dc_x1} to v_{dc_x6}, and v_{dc_y1} to v_{dc_y6}; (**b**) the multilevel voltage of the *spRPCx* and *spRPCy*, v_{outx} and v_{outy}, and the voltage of the common dc-link voltage, v_{dc}; (**c**) the currents on each TPS, i_{PGx} and i_{PGy}, and the output currents of the sp-RPC, i_{spRPCx} and i_{spRPCy}.

Finally, the last result is presented in Figure 17 during the time interval from 2.9 s to 3 s in Figure 13, when the system is in steady-state operation. Figure 17a shows it is possible to verify the voltages of each TPS, v_{PGx} and v_{PGy}, as well as the voltages on each side of the sp-RPC, v_{spRPCx} and v_{spRPCy}. Moreover, it is possible to see that v_{dc_x6} has an average value of 6.95 kV, while v_{dc_y6} has an average value of 7.07 kV during this interval. The remaining voltages have similar values of the dc-link on the same side. In Figure 17b the voltages v_{outx} and v_{outy} are displayed, and it is also possible to see that v_{dc} shows an average value of 1.02 kV during this interval. Finally, by analyzing Figure 17c, it is possible to verify that i_{PGx} and i_{PGy} have a similar amplitude value, obtaining a maximum amplitude of 146.3 A and 155 A, respectively. At this time, i_{spRPCx} has a maximum value of 89.74 A, while i_{spRPCy} has a maximum value of 87.46 A.

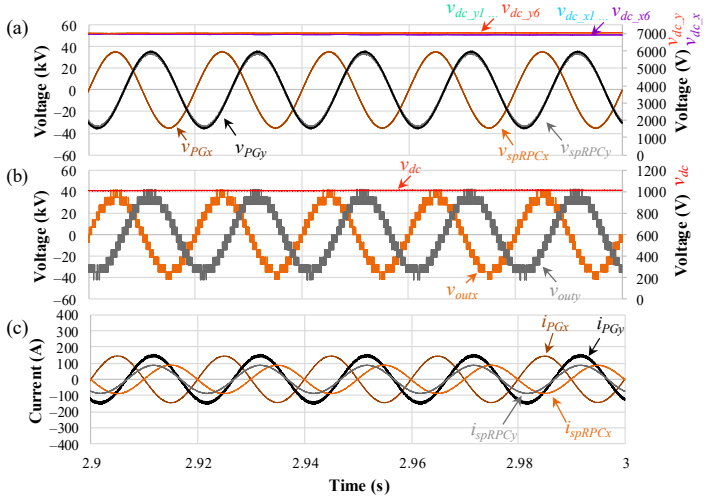

Figure 17. Detailed real-scale simulation results during the time interval from 2.9 s to 3 s: (**a**) the voltages on each TPS, v_{PGx} and v_{PGy}, the output voltages of the sp_{RPCx} and sp_{RPCy}, v_{spRPCx} and v_{spRPCy}, and voltages on the dc-link of each submodule, v_{dc_x1} to v_{dc_x6}, and v_{dc_y1} to v_{dc_y6}; (**b**) the multilevel voltage of the *spRPCx* and *spRPCy*, v_{outx} and v_{outy}, and the voltage of the common dc-link voltage, v_{dc}; (**c**) the currents on each TPS, i_{PGx} and i_{PGy}, and the output currents of the sp-RPC, i_{spRPCx} and i_{spRPCy}.

5. Performance Analyses of the sp-RPC

This topic serves as a critical analysis and discussion of the results obtained, presenting quantitative data on the performance of the real-scale model developed. These data essentially portray the ability to balance the active power in each TPS.

For the quantitative analysis, it is necessary to implement a methodology quantifying the percentage value of active power unbalance in operation in each TPS. Once the values before and after the activation of the implemented control algorithms were measured, with the aid of the methodology implemented in [25], it was possible to quantify the performance of the sp-RPC. The equation used is represented in Equation (15). Initially, the maximum absolute value of the difference between P_{PG} and P_{avg} is determined, where P_{PG} represents the operating power of one side of the TPS, either side x-side or y-side, and P_{avg} represents the average value of the operating power of the two TPS. The maximum value determined is then divided by P_{avg} in order to determine the unbalance. Finally, by multiplying the result by 100, it is possible to obtain the percentage value of the unbalance.

$$Unbalance_{\%} = \frac{\left|P_{PG} - P_{avg}\right|_{Max}}{P_{avg}} \times 100[\text{in}\%], \tag{15}$$

Table 3 shows the current and voltage rms values, the active power of each TPS as well as from each side of the sp-RPC, and the unbalance value. This analysis is performed taking into account the moments before and after the sp-RPC is activated. Thus, the P_{PG_off} variable represents the average active power between the two TPS when the sp-RPC is off, and P_{PG_on} is used for the same measurement when the sp-RPC is on.

Analyzing the performance firstly, when the sp-RPC is off (the left side of Table 3), it is possible to verify that the side with the highest load causes a voltage drop—concluding that the greater the load, the greater the voltage drop at the connection point of sp-RPC, v_{spRPCx} and v_{spRPCy}. Additionally, to highlight the existing unbalance in the current values of the i_{PGx} and i_{PGy}. On the bottom side of Table 3, the average values of the operating powers of each TPS for different initial operating load conditions (with the sp-RPC disconnected) can be seen. Analyzing the data, it is possible to verify that the greater the difference in the value of the connected load, the greater the unbalance caused by each TPS, as expected. Nevertheless, to mention that the system unbalance varies from values of 33.3% to 169.3%.

Table 3. Currents and voltages rms values, and active power and unbalance value for different locomotive consumption before and after the sp-RPC being enabled.

	sp-RPC Disabled			sp-RPC Enabled			
Event / **Parameters**	**(i)**	**(ii)**	**(iii)**	**(i)**	**(ii)**	**(iii)**	
i_{PGx}	39.97	39.97	39.97	144	56.9	102	A
i_{PGy}	245.8	155	165.4	143	63.5	104	A
i_{spRPCx}	-	-	-	105	97	62.4	A
i_{spRPCy}	-	-	-	100	100	61.4	A
v_{PGx}	24,992	24,992	24,994	24,983	25,004	24,987	V
v_{PGy}	24,982	25,018	24,985	24,990	25,005	24,992	V
v_{spRPCx}	24,982	24,982	24,984	24,923	25,043	24,950	V
v_{spRPCy}	24,940	25,081	24,968	25,013	25,014	25,000	V
P_{Loadx}	999	999	999	999	999	999	kW
P_{Loady}	6119	−3884	4122	6119	−3884	4122	kW
P_{PGx}	999	999	999	3612	−1419	2565	kW
P_{PGy}	6119	−3884	4122	3626	−1367	2565	kW
P_{spRPCx}	-	-	-	−2608	2424	−1564	kW
P_{spRPCy}	-	-	-	2507	2507	1534	kW
P_{PG_off}	3559	−1442	2560	-	-	-	kW
P_{PG_on}	-	-	-	3619	−1393	2565	kW
$P_{PG\_\%inc}$	-	-	-	1.7	−3.4	0.2	%
Unbalance	71.9	169.3	61.0	0.19	1.86	0	%

Regarding the analysis when the sp-RPC is on, this can be evaluated with the data presented on the right side of Table 3. Thus, it was possible to verify that on the side where the sp-RPC injects energy, the voltage at the coupling point increases slightly. On the other hand, on the side with the highest load coupled, the voltage drop is minimized. Nevertheless, to highlight the balancing capability of the sp-RPC, imposing similar i_{PGx} and i_{PGy} rms values. Analyzing the active power values, it is possible to conclude that the proposed algorithm mitigates the existing unbalance, decreasing to values below 1.86% in the existing operating conditions.

Nevertheless, it was possible to verify that with the start of the operation of the sp-RPC, the average value of the power between the two TPS increased. That is, and for the case P_{Loadx} = 999 kW and P_{Loady} = 6119 kW, initially, the average value of the two TPS with the sp-RPC disabled, P_{PG_off}, was 3559 kW, changing to 3619 kW when the sp-RPC was enabled, P_{PG_on}. The start-up of the sp-RPC reflected an increase of 1.7%, $P_{PG\_\%inc}$, in the average operating power of the two TPS. The same phenomenon occurs in the remaining operating conditions.

6. Discussion

In this topic, a critical analysis of the results obtained is performed. For this, it is necessary to verify the initial operating conditions of the active powers of the TPS presented in the table. It verified the existence of operation unbalances, the largest unbalance identified by the regenerative braking event. These unbalances are reflected in different operating currents, as shown in the table. Nevertheless, the higher the current, the higher the voltage drop at the end of the overhead contact line, which is identified by the connection point of sp-RPC, v_{spRPCx} and v_{spRPCy}. In turn, with regenerative braking, one encounters an

increase in the rms value of the overhead contact line voltages, being most evident, once again, at the end of the overhead contact line, v_{spRPCy}. With the sp-RPC on, it is possible to impose a similar average operating power in each power TPS. This characteristic was quantified by presenting the results obtained in the table. Analyzing the first case presented, with P_{Loadx} = 999 kW and P_{Loady} = 6119 kW, it is possible to verify that with the sp-RPC, it was possible to decrease an unbalance from 71.9% to 0.19%. Analyzing the initial data with sp-RPC disabled, it is possible to verify an active power between the two TPS of P_{pg_off} = 3559 kW. When the sp-RPC starts operating, this value rises to P_{PG_on} = 3619 kW. This increase, $P_{PG\_inc\%}$, is due essentially to the energy losses presented by the sp-RPC.

Regarding the regenerative braking event, it was also possible to minimize system unbalances by distributing the energy from regenerative braking to the two energy TPS. With this, it was also possible to impose a greater balance of voltages on the overhead contact lines. The negative value in P_{PG_on} is due to the decrease in the average absolute value of the active powers of the two TPS due to the sp-RPC losses.

In general, the overhead supply circuit can have different parameters (resistance and inductance per km, namely), and they have an impact on the voltage drop. The higher the traction load, the longer the distance from the TPS, and the lower the power factor, the higher the voltage drop. The sp-RPC has the capability of compensating this voltage drop through reactive power control (i.e., an SVC function); this will be addressed in future work together with the interface of a PV and BESS system. In the same way, when redirecting active power, the sp-RPC can increase (in some operating scenarios) the system's overall losses, which can be an issue for infrastructure managers.

7. Conclusions

This paper proposes a control algorithm integrated into a sectioning post-Rail Power Conditioner (sp-RPC) connected to a neutral section between two TPS. The proposed control algorithm presents a good dynamic response to any disturbance originated by the electric locomotives, either in a moment of acceleration or regenerative braking, maintaining a similar operating active power in the two TPS. The developed analysis was based on real-scale computational models, presenting a modular and multilevel architecture for the power electronic converters. As such, the proposed control algorithm also allows the correct balancing of the voltages at the different dc-links that compose the sp-RPC. For the sp-RPC analysis, different scenarios were considered, showing in a detailed way how the sp-RPC works in the instant of disturbance as well in steady-state. Quantitative data are also presented and analyzed. In general, it is possible to conclude that the sp-RPC manages to reduce power imbalances between neighboring TPS, contributing to the better operation of electrified railway systems.

Author Contributions: Conceptualization, L.A.M.B.; formal analysis, L.A.M.B.; investigation, L.A.M.B., A.P.M. and J.G.P.; methodology, L.A.M.B. and J.G.P.; software, L.A.M.B.; supervision, A.P.M. and J.G.P.; validation, L.A.M.B. and A.P.M.; writing—original draft, L.A.M.B.; writing—review & editing, L.A.M.B., A.P.M. and J.G.P. All authors have read and agreed to the published version of the manuscript.

Funding: This work has been supported by FCT—Fundação para a Ciência e Tecnologia, within the R&D Units Project Scope UIDB/00319/2020. Luis A. M. Barros is supported by the doctoral scholarship PD/BD/143006/2018, granted by the Portuguese FCT foundation.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Future Population Growth. Available online: https://ourworldindata.org/future-population-growth (accessed on 24 March 2023).
2. Goulding, L.; Morrell, M. *Future of Rail 2050*; Arup Rail: London, UK, 2019; p. 60.
3. IEA—International Energy Agency. *The Future of Rail: Opportunities for Energy and the Environment*; IEA—International Energy Agency: Paris, France, 2019.

4. UIC-ETF (Railway Technical Publications) & CER. *Rail Transport and Environment: Facts & Figures*; CER: Paris, France, 2015.
5. CER. *The Voice of European Railways: Activity Report 2019*; CER: Paris, France, 2019.
6. Infraestruturas de Portugal. Available online: https://www.infraestruturasdeportugal.pt/ (accessed on 30 December 2022).
7. Shift2Rail Joint Undertaking. *Multi-Annual Action Plan (Executive View Part A)*; Horizon 2020 European Union Funding for Research & Innovation: Brussels, Belgium, 2015. Available online: https://rail-research.europa.eu/wp-content/uploads/2017/11/Shift2Rail-MAAP-Part-A_Executive-View_web.pdf (accessed on 24 March 2023).
8. Shift2Rail Joint Undertaking. *Multi-Annual Action Plan*; European Union: Brussels, Belgium, 2019. Available online: https://rail-research.europa.eu/wp-content/uploads/2020/09/MAAP-Part-A-and-B.pdf (accessed on 24 March 2023).
9. Gazafrudi, S.M.M.; Langerudy, A.T.; Fuchs, E.F.; Al-Haddad, K. Power quality issues in railway electrification: A comprehensive perspective. *IEEE Trans. Ind. Electron.* **2015**, *62*, 3081–3090. [CrossRef]
10. Canales, J.M.; Aizpuru, I.; Iraola, U.; Barrena, J.A.; Barrenetxea, M. Medium-Voltage AC Static Switch Solution to Feed Neutral Section in a High-Speed Railway System. *Energies* **2018**, *11*, 2740. [CrossRef]
11. Serrano-Jiménez, D.; Abrahamsson, L.; Castaño-Solís, S.; Sanz-Feito, J. Electrical railway power supply systems: Current situation and future trends. *Int. J. Electr. Power Energy Syst.* **2017**, *92*, 181–192. [CrossRef]
12. Barros, L.A.M.; Tanta, M.; Martins, A.P.; Afonso, J.L.; Pinto, J.G. STATCOM Evaluation in Electrified Railway Using V/V and Scott Power Transformers. In Proceedings of the International Conference on Sustainable Energy for Smart Cities, Braga, Portugal, 4–6 December 2019; pp. 18–32. [CrossRef]
13. Li, T.; Shi, Y. Application of MMC-RPC in High-Speed Railway Traction Power Supply System Based on Energy Storage. *Appl. Sci.* **2022**, *12*, 10009. [CrossRef]
14. Song, S.; Liu, J.; Ouyang, S.; Chen, X. A modular Multilevel Converter Based Railway Power Conditioner for Power Balance and Harmonic Compensation in Scott Railway Traction System. In Proceedings of the 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), Hefei, China, 22–26 May 2016; pp. 2412–2416. [CrossRef]
15. Li, T.; Shi, Y. Power Quality Management Strategy for High-Speed Railway Traction Power Supply System Based on MMC-RPC. *Energies* **2022**, *15*, 5205. [CrossRef]
16. Tanta, M.; Cunha, J.; Barros, L.A.; Monteiro, V.; Pinto, J.; Martins, A.P.; Afonso, J.L. Experimental Validation of a Reduced-Scale Rail Power Conditioner Based on Modular Multilevel Converter for AC Railway Power Grids. *Energies* **2021**, *14*, 484. [CrossRef]
17. Barros, L.A.M.; Tanta, M.; Martins, A.P.; Afonso, J.L.; Pinto, J.G. Opportunities and Challenges of Power Electronics Systems in Future Railway Electrification. In Proceedings of the 2020 IEEE 14th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Setubal, Portugal, 8–10 July 2020. [CrossRef]
18. Aoki, K.; Kikuchi, K.; Seya, M.; Kato, T. Power Interchange System for Reuse of Regenerative Electric Power. *Hitachi Rev.* **2015**, *67*, 834–835.
19. Morais, V.A.; Martins, A.P. Traction power substation balance and losses estimation in AC railways using a power transfer device through Monte Carlo analysis. *Railw. Eng. Sci.* **2022**, *30*, 71–95. [CrossRef]
20. Kosugi, R.; Ji, S.; Mochizuki, K.; Adachi, K.; Segawa, S.; Kawada, Y.; Yonezawa, Y.; Okumura, H. Breaking the Theoretical Limit of 6.5 kV-Class 4H-SiC Super-Junction (SJ) MOSFETs by Trench-Filling Epitaxial Growth. In Proceedings of the 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 19–23 May 2019; pp. 39–42. [CrossRef]
21. Kadavelugu, A.; Bhattacharya, S.; Ryu, S.-H.; Van Brunt, E.; Grider, D.; Agarwal, A.; Leslie, S. Characterization of 15 kV SiC n-IGBT and its application considerations for high power converters. In Proceedings of the 2013 IEEE energy conversion congress and exposition, Denver, CO, USA, 15–19 September 2013; pp. 2528–2535. [CrossRef]
22. Howell, R.S.; Buchoff, S.; Van Campen, S.; McNutt, T.R.; Ezis, A.; Nechay, B.; Kirby, C.F.; Sherwin, M.E.; Clarke, R.C.; Singh, R. A 10-kV Large-Area 4H-SiC Power DMOSFET with Stable Subthreshold Behavior Independent of Temperature. *IEEE Trans. Electron Devices* **2008**, *55*, 1807–1815. [CrossRef]
23. Passmore, B.; Cole, Z.; McGee, B.; Wells, M.; Stabach, J.; Bradshaw, J.; Shaw, R.; Martin, D.; McNutt, T.; VanBrunt, E.; et al. The next generation of high-voltage (10 kV) silicon carbide power modules. In Proceedings of the 2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Fayetteville, AR, USA, 7–9 November 2016; pp. 1–4. [CrossRef]
24. Das, M.K.; Capell, C.; Grider, D.E.; Leslie, S.; Ostop, J.; Raju, R.; Schutten, M.; Nasadoski, J.; Hefner, A. 10 kV, 120 A SiC half H-bridge power MOSFET modules suitable for high frequency, medium voltage applications. In Proceedings of the 2011 IEEE Energy Conversion Congress and Exposition, Phoenix, AZ, USA, 17–22 September 2011; pp. 2689–2692. [CrossRef]
25. Barros, L.A.M.; Martins, A.P.; Pinto, J.G. A Comprehensive Review on Modular Multilevel Converters, Submodule Topologies, and Modulation Techniques. *Energies* **2022**, *15*, 1078. [CrossRef]
26. Pinto, J.G.; Monteiro, V.; Goncalves, H.; Afonso, J.L. Onboard reconfigurable battery charger for electric vehicles with traction-to-auxiliary mode. *IEEE Trans. Veh. Technol.* **2013**, *63*, 1104–1116. [CrossRef]
27. Gohil, G.; Wang, H.; Liserre, M.; Kerekes, T.; Teodorescu, R.; Blaabjerg, F. Reduction of DC-link capacitor in case of cascade multilevel converters by means of reactive power control. In Proceedings of the 2014 IEEE Applied Power Electronics Conference and Exposition-APEC, Fort Worth, TX, USA, 16–20 March 2014; pp. 231–238. [CrossRef]
28. Karimi-Ghartemani, M.; Iravani, M.R. A Method for synchronization of power electronic converters in polluted and variable-frequency environments. *IEEE Trans. Power Syst.* **2004**, *19*, 1263–1270. [CrossRef]

29. Karimi-Ghartemani, M. *Enhanced Phase-Locked Loop Structures for Power and Energy Applications*; John Wiley & Sons: Hoboken, NJ, USA, 2014. [CrossRef]
30. Blaabjerg, F.; Teodorescu, R.; Liserre, M.; Timbus, A.V. Overview of control and grid synchronization for distributed power generation systems. *IEEE Trans. Ind. Electron.* **2006**, *53*, 1398–1409. [CrossRef]
31. Monteiro, V.; Oliveira, C.F.; Afonso, J.L. Experimental Validation of a Bidirectional Multilevel dc-dc Power Converter for Electric Vehicle Battery Charging Operating under Normal and Fault Conditions. *Electronics* **2023**, *12*, 851. [CrossRef]
32. Basri, H.M.; Lias, K. Predictive Current Control of Three Level Neutral Point Clamped Based Indirect Matrix Converter. In Proceedings of the 2019 International UNIMAS STEM 12th Engineering Conference (EnCon), Kuching, Malaysia, 28–29 August 2019; pp. 16–21. [CrossRef]