Universidade do Minho
Escola de Engenharia

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Performance of Radiofrequency Circuits Based on 2D Technology

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Work developed under the supervision of:
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STATEMENT OF INTEGRITY

I hereby declare having conducted this academic work with integrity. I confirm that I have not used plagiarism or any form of undue use of information or falsification of results along the process leading to its elaboration.

I further declare that I have fully acknowledged the Code of Ethical Conduct of the Universidade do Minho.

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Abstract

Performance of Radiofrequency Circuits Based on 2D Technology

As the IoT become more prevalent and require a massive number of devices with a small footprint to be integrated without much notice, the ability to miniaturise the electronic components while maintaining or improving their performance becomes a challenge. This challenge is associated with short-channel effects and interconnect's heating.

In recent years, 2D materials became the focus of many investigations as a possible solution to the above-mentioned problems. One of the most promising materials is graphene due to its remarkable properties, such as high carrier mobility compared to silicon. In this regard, many studies focus on the fabrication of graphene-based transistors but lack the ability to predict the device's behaviour since there are no well-defined models.

This dissertation's main objective is to understand how to perform circuit-level simulations of graphene-based transistors. In this regard, three models chosen from the literature were implemented in an EDA tool to understand which would be more reliable for DC and RF applications. Since some of the models rely on parameters extracted from real devices, an insight into how to perform measurements and extract the desired parameters is presented.

The models were simulated against real data to understand the importance of simulation for more complex designs. It was possible to conclude that a semi-empirical model allows for obtaining closer results and can be used in both the DC and RF domains. The semi-empirical model allowed simulation and refinement at the circuit level of inverters, ring oscillators and frequency doublers. Moreover, the devices simulated using graphene transistors show the need for this kind of simulation to understand the operation points needed for the device's functioning.

Keywords: Graphene transistors, 2D materials, Radio frequency, Modelling

Resumo

Circuitos de Radiofrequência Baseados em Tecnologia 2D

À medida que as IoT se tornam mais prevalentes e requerem um número massivo de dispositivos que ocupem pouco espaço, a habilidade de reduzir os componentes eletrónicos mantendo ou aumentando a sua performance torna-se um desafio. Este desafio está associado com efeitos de canal pequeno e o aquecimento dos *interconnects*.

Nos últimos anos os materiais 2D tornaram-se o foco de muitas investigações como possível solução para os problemas mencionados. O material mais promissor é o grafeno devido às suas propriedades extraordinárias, tais como a sua elevada mobilidade de portadores de carga em relação ao silício. Neste sentido muitas estudos focam-se na fabricação de transístores de grafeno, mas não têm a capacidade de prever o comportamento do dispositivo uma vez que não existem modelos bem definidos.

O principal objetivo desta dissertação é entender como efetuar simulações de circuitos com transístores de grafeno. Neste sentido três modelos escolhidos da literatura foram implementados numa EDA para entender qual seria mais fidedigno para aplicações DC e RF. Como alguns modelos dependem de parâmetros extraídos de dispositivos reais, é dada uma breve explicação em como fazer medições e extrair os parâmetros desejados.

Os modelos foram simulados e comparados com dados reais para perceber a importância da simulação em circuitos mais complexos. Destas simulações foi possível concluir que um modelo semi-empirico gera resultados mais próximos dos reais, e que pode ser utilizado no domínio DC e RF. O modelo semi-empírico permitiu simulação e refinamento ao nível do circuito de inversores, ring oscillators e duplicadores de frequência. Para além disso, das simulações com dispositivos usando os transistores de grafeno é possível aferir a necessidade deste tipo de simulações de modo a perceber os pontos de operação necessários para o funcionamento destes dispositivos.

Palavras-chave: Transistor de Grafeno, Materiais 2D, Radio frequência, Modelo

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Acronyms

I_{DS}	Extrinsic drain-source current 11, 14, 15, 18, 22, 37, 42, 45
MoS_2	Molybdenum disulfide 4, 5, 11, 14, 17
V_{DS}	Extrinsic drain-source voltage 35, 37, 38, 40, 41, 43
V_{GS}	Extrinsic gate-source voltage 21, 35, 37, 39, 40, 45
V_{ds}	Intrinsic drain-source voltage 26, 30
V_{gd}	Intrinsic gate-drain voltage 28, 29
V_{gs}	Intrinsic gate-source voltage 21, 28, 29
f_T	Cut-off frequency 14, 15, 16, 18, 19, 23, 33, 34, 38, 39
f_{max}	Maximum oscillation frequency 14, 15, 16, 18, 33, 34, 38, 39
g_m	transconductance 15, 22, 31, 37, 39, 40
1D	One dimensional 18
2D	Two dimensional 1, 2, 3, 4, 7, 10, 11, 16, 18, 20, 46
AC	Alternating current 12, 23, 45
ALD	Atomic layer deposition 12
AM	Analytical Model 21, 25, 37, 38, 40, 45
CVD	Chemical Vapour Deposition 4, 5
DC	Direct Current 2, 3, 6, 8, 12, 15, 18, 20, 21, 22, 23, 25, 26, 28, 30, 31, 35, 37, 38, 40, 41, 45, 46
DOS	Densisty of states 14
DUT	Device Under Test 25, 33, 34, 39
EDA	Electronic Design Automation 2, 3, 21, 25, 28, 35, 36, 37, 54
EDL	Electrical double layer 8, 12
EM	Empirical Model 21, 31, 37, 38, 39, 40
FET	Field Effect Transistor 11, 22
FETs	Field Effect Transistors 5, 14, 26
FOMs	Figures Of Merit 7, 10, 15, 21, 31, 34, 35, 39, 40, 45

GFET	Graphene Field-Effect Transistor 2, 3, 12, 15, 19, 20, 22, 25, 26, 28, 31, 37, 41, 42, 44, 45, 46
GFETs	Graphene Field-Effect Transistors 10, 11, 12, 14, 15, 18, 19, 20, 21, 26, 41, 42, 45, 46
GUI	Graphic User Interface 2, 3, 32, 34, 46
H-params	Hybrid parameters 23
hBN	Hexagonal boron nitride 9, 10, 12
ICs	Integrated Circuits 8
IIP3	Third-order Intercept Point 19
IoT	Internet of Things 1
MAG	Maximum Available Gain 16
MLG	Multilayer graphene 6
MSG	Maximum Stable Gain 16
Q-factor	Quality factor 6, 7, 8, 9, 10, 20
RF	Radio Frequency 1, 2, 3, 5, 7, 8, 11, 12, 14, 15, 18, 19, 20, 21, 22, 23, 24, 28, 32, 35, 38, 39, 40, 41, 46
SEM	Semi-Empirical Model 21, 28, 32, 37, 38, 39, 40, 41, 45, 46
S-params	Scattering parameters 15, 23, 24, 31, 33, 35, 39, 41, 54
SLG	Single layer graphene 6
TMDS	Transition-metal dichalcogenides 4, 5
U/MAG/MSG	Maximum Gain 15, 16
VNA	Vector Analysis Network 23
Y-params	Admitance parameters 23, 24, 25, 32
Z-params	Impedance parameters 23, 24, 25

1

Introduction

Technology has always been around, be it the most straightforward wooden wheel or a more complex system like a modern car. Technology's and science's evolution pave the way for society's evolution. One of the most relevant breakthroughs in the past years was the transistor's discovery in 1947. This discovery allowed for replacing the vacuum tube, also known as the valve, with a device with a smaller footprint and better efficiency. This discovery led to a massive bump in industrial society's evolution. Technology fully integrates people's lives directly in the devices they use (e.g., smartphones) or indirectly by those who provide them with a service (e.g., mobile operators' signal coverage).

This revolution was possible due to the miniaturization of the electronic components that integrate transistors while maintaining or improving their performance. According to Moore's Law, the number of transistors in the same chip area doubles every two years. This law has been confirmed for over 50 years, but it is getting to a point where reducing component size is reaching its physical limitations due to short-channel effects and interconnect's heating [1, 2]. Further research on new materials is required to replace silicon before a new paradigm in nanoelectronics – more than Moore – can be reached.

In recent years, Two dimensional (2D) materials have become the focus of many investigations to replace silicon to continue downscaling electronic devices [3–6]. Many of these materials show excellent electronic, photoelectronic, and mechanical properties. Therefore, investigating the implementation of a technology based on such materials is imperative as the Internet of Things (IoT) becomes ever more prevalent and requires a massive number of devices with a small footprint to be integrated without much notice. Although these are promising materials, their integration with standard manufacturing processes and replicability outside the laboratories is yet to be achieved [7]. Furthermore, other problems associated with interfacing 2D and other materials continues to be challenging since these interfaces usually degrade their electronic properties, especially carrier mobility, reducing their overall performance [8, 9].

Despite all the challenges associated with 2D materials, these materials are investigated in an extensive range of applications. Among these applications are electronics, sensing, photonic, optoelectronic, power and energy [10]. In the electronics field, investigations are done towards low-power and flexible electronics, and components like transistors, capacitors and inductors are developed for their implementation in the Radio Frequency (RF) domain [11]. As for the sensing applications, gas sensors [12] and biosensors [13] are being studied by taking advantage of the large surface-to-volume ratio of 2D materials and the ability to functionalize the surface to detect the desired molecule. In photonic and optoelectronic applications, photodetectors are being studied for photo imaging and photovoltaic applications [14]. In power and energy applications, graphene is being studied as a substitute for the electrodes of batteries [15] and supercapacitors [16] due to its high surface area and flexible behaviour. As the investigations progress, the ability to simultate the devices' behaviour to optimize them and understand their implementation in more complex systems becomes imperative.

1.1 Work Motivation

This Master's Dissertation comes from the urgent need to find new ways of developing even smaller devices/systems to increase device performance per area and the ability to integrate these tiny systems where modern electronics cannot be used (e.g. flexible systems). This project's work will rely on electronic components already fabricated using 2D materials. After identifying the main characteristics of the available electronic sub-systems, a model to simulate each element, which allows for predicting the performance of a 2D system, will be proposed. The main goal is to build a simulation framework that enables an understanding of the potential of graphene electronic RF systems to be used as a replacement/complement to the already available systems. This work will rely on the expertise from ongoing research on 2D Technology.

1.2 Contribution

The main contribution of this master's dissertation was to choose among the already available models that describe the behaviour of Graphene Field-Effect Transistor (GFET) the one that was most suitable for both Direct Current (DC) and RF simulations and implement it in Verilog-A to be used on an Electronic Design Automation (EDA) tool. In this study, three models were tested using parameters extracted from a real device to choose the one that best fits the measurements.

Since some models rely on parameter extraction from measured data, a brief explanation of performing such measurements and extracting the parameters is presented. This explanation includes the de-embedding process for RF performance assessment.

The final contribution is the development of a Python Graphic User Interface (GUI) to extract both DC and RF parameters based on the model found to be the most reliable during this dissertation.

1.3 Dissertation organization

This dissertation is organized into five chapters.

Chapter 1 is a brief introduction to the 2D material technologies alongside the motivation and contributions of this study.

Chapter 2 is a literature review of the state-of-the-art in 2D materials-based RF electronics. The chapter briefly introduces 2D materials, followed by both passive and active components based on 2D materials, particularly graphene-based devices.

Chapter 3 presents how to measure and extract parameters from both DC and RF analysis, followed by the presentation of the three models that try to predict the GFET behaviour. This chapter also presents a Python GUI that allows for a user-friendly environment for both DC and RF parameters extraction of the GFET according to the model found to be the most reliable.

Chapter 4 compares three models in different types of simulations. This chapter starts with a quick tutorial on how to implement the models in EDA tools by using Verilog-A language, followed by the test of the three models in DC and RF analysis. The best model is then used to simulate an inverter, a ring oscillator and a frequency doubler.

The final chapter provides a general conclusion of the work developed in this master's and presents a perspective of future work.

2

2D material-based RF components and devices

2.1 2D Materials

The first 2D material discovered was graphene by Andre Geim and Konstantin Novoselov in 2004, which led them to win The Novel Prize in Physics in 2010 [17]. The graphene was obtained using tape to exfoliate graphite until it reached a single atomic layer. The discovery of graphene launched curiosity and investigations into graphene and other 2D materials. These days, the research of 2D materials has progressed immensely to a point where we can already separate 2D materials into families according to their element's chemical composition, unit cell, electronic, optical, or structural properties [18]. The most known families are X-enes and Transition-metal dichalcogenides (TMDS). X-enes are single-element materials with atoms organized in a hexagonal lattice, which is the case of graphene, silicene, germanene and others. TMDS group 2D materials of the form MX_2, where M is a transition metal from the 4th, 5th or 6th group, and X is a chalcogen from group 16th. The most known TMDS are Molybdenum disulfide (MoS_2), tungsten disulfide, and molybdenum diselenide. Since some 2D materials were discovered recently, their science and technology are not mature enough to place them as next-generation electronic materials. Therefore, we limit the discussion to graphene and MoS_2 since, as of today, they are by far the most studied materials.

Graphene consists of a single graphite layer of carbon atoms arranged in a hexagonal lattice. Graphene can be grown at a large scale by Chemical Vapour Deposition (CVD) [19, 20] or Liquid Phase Exfoliation (LPE). One of the problems with graphene fabrication is that it cannot be grown directly on most substrates. Graphene is usually deposited on a transition metal catalyst foil – often copper or nickel - and then transferred using a wet or dry transfer process to the desired substrate [21]. Because of the need to transfer to the final substrate, graphene's performance is affected by the degradation of its carrier mobility during this transfer process [22]. Graphene has remarkable properties, such as extremely high carrier mobility ($\mu > 2000\ cm^2V^{-1}s^{-1}$ for any CVD mechanically transferred graphene [23] and $\mu \approx 200000\ cm^2V^{-1}s^{-1}$ for exfoliated suspended graphene [24]) when compared to silicon ($1400\ cm^2V^{-1}s^{-1}$ for electrons and $450\ cm^2V^{-1}s^{-1}$ for holes), good electrical conductivity ($\approx 10^4\ \Omega^{-1}cm^{-1}$ [24]), high thermal conductivity ($5300\ Wm^{-1}K^{-1}$ [25]), and high Young's modulus ($0.5 - 1.0\ TPa$ [23]). This material is a gapless semiconductor ($0\ eV$ energy gap). Because of this intrinsic property, graphene cannot be used in devices where the off state is needed since the material always conducts electricity by holes or electrons since the valence and conduction band communicate at the Dirac point. These properties make graphene a possible solution to overcome silicon limitations in certain applications and can be implemented in devices with a broad range of uses, from high-speed electronics to sensing applications.

MoS_2 belongs to the TMDS family and consists of a molybdenum layer sandwiched between two sulphur layers. This material appears in nature as molybdenite and like graphene, can be fabricated using CVD or exfoliation techniques. Unlike graphene, MoS_2 properties are not all well-defined, but its carrier mobility has been shown to have values up to $200\ cm^2V^{-1}s^{-1}$ at room temperature and Young's modulus of $0.33\ TPa$ [26]. In addition, unlike graphene, MoS_2 has a direct bandgap with $1.8\ eV$ [20], which means it can be used in devices that need an off state.

Due to the remarkable properties of these materials, their implementation on capacitors, inductors, and Field Effect Transistors (FETs) is already reported in numerous papers. In the following sections, the literature on these components will be explored regarding their physical implementation and the models that try to predict these components' behaviour.

2.2 2D Passive Component

Passive components are defined as electronic components that cannot introduce energy into a circuit. They also cannot have a source of power. This definition of components includes inductors and capacitors since they cannot amplify the input signal. Both the inductors and capacitors are usually used as signal filters but can also be used as sensors. In this section, graphene-based inductors and capacitors will be explored.

2.2.1 Graphene Inductors

On-chip inductors revolutionized RF electronics in the 90s, but not everything is excellent. These inductors are planar and must have a large area dictated by electromagnetic laws, which means they cannot be downsized alongside standard transistors while maintaining high inductance density. In some cases, it is reported that planar inductors occupy up to 50% of an integrated circuit area. Thus, they hinder further miniaturization and integration. Finding new approaches to making these devices is imperative.

It is well known that the inductance is shape and size-dependent, but in graphene, a third factor can be explored, known as kinetic inductance. This material property arises from the inertia of charge carriers moving in alternating electric fields. Like all mass particles, charge carriers preserve their momentum, so when in an alternating electric field, it takes a finite time to change their speed according to the field, which manifests as kinetic inductance. It is not very important in conventional metals because their conductance is associated with higher carrier concentration and macroscopic thickness. The kinetic inductance manifests as an equivalent series inductance, adding to the geometric inductance related to the shape/size. Therefore, materials with high kinetic inductance must be used to reduce inductor size while maintaining high inductance density. Graphene is being exploited as a possible solution to the inductance components miniaturization issue due to its atomic thickness, and relatively high conductivity, based on high carrier mobility and low carrier concentration. Consequently, graphene has high kinetic inductance and a small footprint.

A Multilayer graphene (MLG) inductor is proposed in [27]. The authors' choice of using MLG is to ensure a lower quantum contact resistance (resistance associated with the interface between graphene and metal contact). This approach raises two problems: when compared with metals, graphene has a much lower conductivity, compared to Single layer graphene (SLG), the MLG exhibits reduced charge carrier inertia due to interlayer coupling. Bromine intercalation is used to overcome these issues by increasing the conductivity and reducing interlayer coupling. Using this approach, Quality factor (Q-factor) up to 12 are achievable and 1.5-times higher inductance in a two-turn inductor when compared to copper ones. The authors also claim that it is possible to achieve better results by improving the intercalation technology and increasing contact quality.

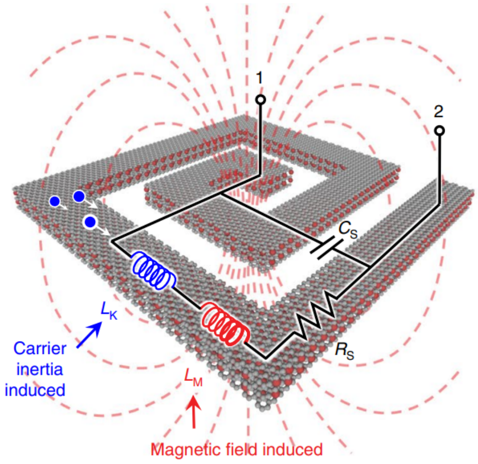


Figure 1: Schematic of a spiral inductor and its simplified equivalent circuit. L_M and L_K are the magnetic and kinetic inductance, respectively. R_S and C_S are the series resistance and the inter-turn capacitance, respectively [27].

2.2.1.1 Modelling Of Graphene Inductors

The modelling of graphene inductors is not perfectly established, and most works are based on extracting parameters or simulating typical metallic structures, adding some parameters to better match graphene characteristics.

In [27], the authors affirm that current simulation tools cannot capture the physics of graphene in modelling impedance/inductance. To try and predict the inductor behaviour, the authors start by analysing the performance of the inductors through finite element method (FEM) simulations in ANSYS HFSS and then modelled bulk coils with electrical conductivities considering grain-boundary and surface-scattering effects at the micro and nanoscale for metals, and graphene conductivities extracted from DC analysis.

Although modelling graphene inductors remains a challenge, a simple model of a graphene spiral inductor can be seen in Figure 2. In this model, it can be corroborated that L_k appears in series with L_M, the substrate and dielectric need to be considered, and an inter-turn coupling capacitance appears, resulting from the inductor design. This model predicts that the substrate and the inter-turn coupling degrade the inductor's behaviour at higher frequencies.

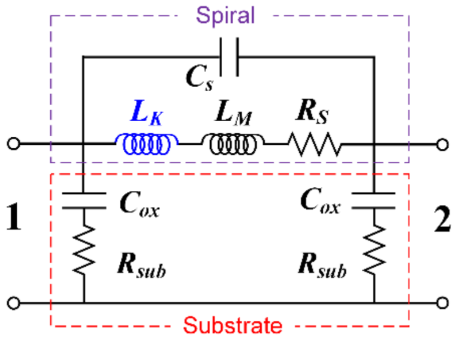


Figure 2: Simplified circuit model for a two-turn inductor. L_K, L_M and R_S are the kinetic inductance, magnetic inductance, and series resistance of the graphene inductor, respectively. C_s is the inter-turn coupling capacitance. C_{ox} and R_{sub} substrate dielectric capacitance and substrate resistance, respectively [27].

By using Launder's approach, the kinetic inductance per unit length is given by:

$$L_k = \frac{2\pi\hbar}{e^2 v_F M} \approx \frac{81\ nH}{M}/\mu m \tag{2.1}$$

where M is the number of quantum modes $\left(M = \frac{\Delta E_F}{\pi\hbar v_F}\right)$, ΔE_F is the difference between Dirac point energies and Fermi level, W is the width of graphene, e is the electron charge, $\hbar$ is the reduced Planck's constant, and v_F is the Fermi velocity. The Figures Of Merit (FOMs) of an inductor is the Q-factor and is expressed as:

$$Q_{factor} = -\frac{\text{Imag}[Y_{12}]}{\text{Real}[Y_{12}]} = \frac{Z_L/j}{R} = \frac{wL}{R} \tag{2.2}$$

where Y_{12} is an admittance parameter, Z_L is the inductor impedance, L and R are the inductance and resistance of the inductor, and w is the angular frequency.

2.2.2 Graphene capacitors

A capacitor is a passive device that stores electrical energy and adds capacitance to a circuit. The main usages of this device are to serve as a signal filter, for example, in a ladder design or a temporary battery. The simplest capacitor consists of two parallel metal plates separated by a dielectric material and the energy stored depends on the area of the plates, the distance between plates, the permittivity, and the dielectric function. Capacitors based on 2D materials have been explored, and the most common material used is graphene. Most of the work is done towards biosensing, but research in the RF branch is emerging.

Graphene is used in the biosensing scene due to the possibility of functionalizing the graphene's surface. By immobilizing molecular probes on graphene using a linker, it is possible to change the graphene's surface charge density whenever there is a biorecognition event. This change accumulation or depletion happens due to the charged or polar target molecules' local gating, which modulates the graphene channel conductance. The effect is capacitive, where the capacitance is that of the Electrical double layer (EDL) forming at the graphene-solution interface. Consequently, different target molecule concentrations induce different amounts of charge in the EDL capacitor, which will be mirrored on the opposite plate of the capacitor, i.e., the graphene surface.

There are no well-defined characteristics of graphene capacitors on the RF branch, but due to the high quantum capacitance and tuning possibility, some works claim that graphene is an excellent candidate. Moreover, the small footprint and low control voltage allow the development of compact systems like voltage-controlled oscillators, tunable filters and phase shifters.

In [28], a variable capacitor based on graphene was implemented as a glucose sensor. This device takes advantage of the carrier density change in functionalized graphene when the adsorbed molecules' concentration changes, leading to the modulation of the channel conductance. As shown in Figure 3, aside from the capacitance dependence in adsorbed molecules concentration, it also depends on the gate voltage and ranges from 90 to 140 pF.

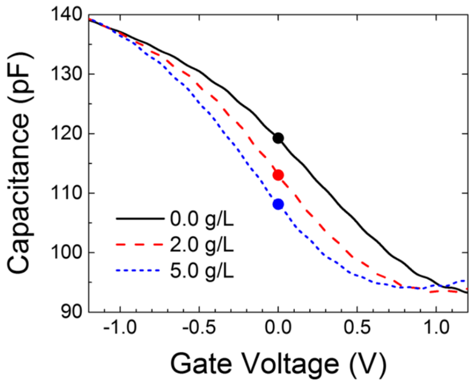


Figure 3: Capacitance-Voltage curves [28].

Another capacitor with tunable control based on graphene was studied for RF applications, and capacitance was between $3.8 - 2.9$ pF, with a gate voltage of 1.25 V and frequencies ranging from 1 to 10 GHz [29]. The best device performance was achieved with 1.25 V gate voltage and 0.4 GHz frequency, obtaining a Q-factor up to 14.5. The device consists of two symmetrically placed capacitors in a parallel configuration so that they can be characterised at microwave frequencies. This design also uses a multi-finger approach to increase the capacitance while reducing graphene's parasitic resistance. From Figure 4, it is possible to see that by changing the DC bias, the capacitance also changes, allowing for low-power Integrated Circuits (ICs). With this design, the maximum Q-factor obtained is 15 at 0.4 GHz, but the authors say it is possible to increase it with simple design changes.

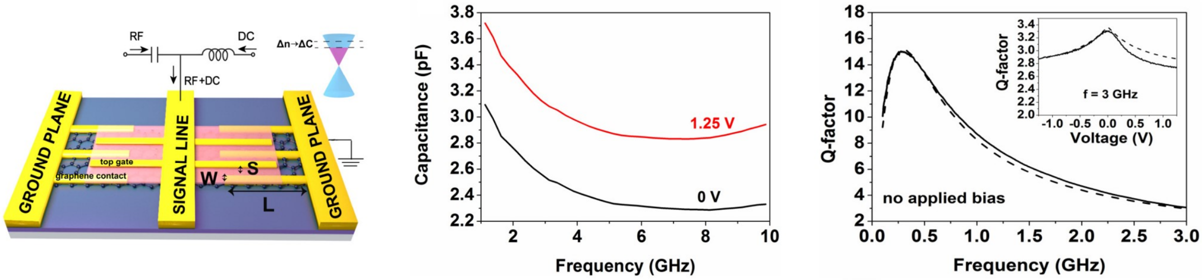


Figure 4: Schematic of the graphene quantum capacitor (left), capacitance dependence on frequency and DC bias (centre) and Q-factor dependence on frequency (right) [29].

In [30], the same authors explored the design described above. By changing the fingers' number and size, the authors concluded that the Q-factor increases when reducing the finger length and that the number of fingers does not have much impact on the Q-factor. It was also concluded that changing the number of fingers makes it possible to scale the capacitors to any capacitance while maintaining similar Q-factor. The best device achieved has a Q-factor of 12 at $1\ GHz$, an improvement from the first study, where at $1\ GHz$ the Q-factor was about 9.

Another tunable graphene capacitor is explored in [31]. This design, Figure 5, is more straightforward than the previous one discussed and consists of a parallel capacitor where the bottom plate is graphene, the dielectric is Hexagonal boron nitride (hBN), and the top plate is chromium (Cr) and gold (Au). From the graph below, it can be proved that the capacitor is tunable and that it has a minimum capacitance of around $3.5\ pF$.

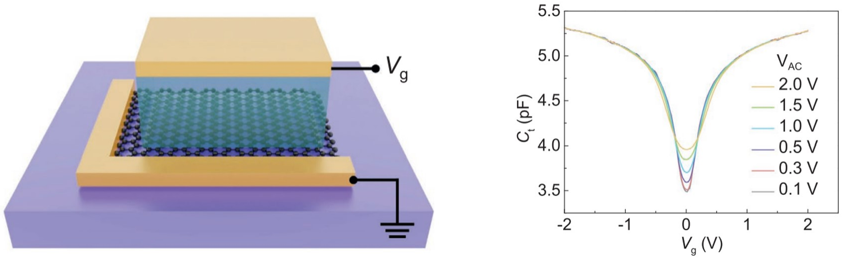


Figure 5: Schematic of graphene tunable capacitor (left) and capacitance dependence on bias voltage and Ac signal voltage (right) [31].

2.2.2.1 Modelling graphene capacitors

As for graphene inductors, the state-of-the-art in graphene capacitor modelling is not well established, and due to the differences between designs, the available models may not suit all layouts.

In [30], the authors used the circuit model in Figure 6 to extract the device parameters for the proposed design. In this model a series resistance $(R_C + R_M + R_{GS})$ is observed, and an oxide capacitance (C_{ox}) that arises from the material's intrinsic properties. The graphene layer raises variable resistance (R_G) and quantum capacitance C_q. The quantum capacitance of graphene is reported as follows:

$$C_q = \frac{2q^2 k_B T}{\pi\left(\hbar v_F\right)^2} \ln\left[2\left(1+\cosh\left(\frac{q\varphi_s}{k_B T}\right)\right)\right] LWN \tag{2.3}$$

where q is the electron charge, k_B is the Boltzmann's constant, T is the temperature, $\hbar$ is the reduced Plank's constant, v_F is the Fermi velocity, φ_s is the electrostatic graphene potential, N is the number of fingers, and L and W are the length and width of the fingers.

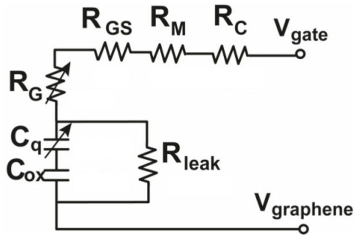


Figure 6: Circuit model used to extract the device parameters. R_C is the contact resistance. R_M is the metal fingers' resistance. R_{GS} is the graphene resistance in the interspace. R_G is the graphene resistance. C_q is the graphene quantum capacitance. C_{ox} is the fixed oxide capacitance [30].

For the more straightforward design [31], the authors propose an equivalent circuit composed of two capacitors in series. One is the geometrical capacitance which depends on the hBN thickness and dielectric constant and is defined as $C_{ox} = \frac{\epsilon}{t_{hBN}}$. The other is the quantum capacitance of the graphene and is defined as $C_q = \frac{dQ}{d\varphi_s}$, where Q is the charge induced on the graphene and φ_s the graphene potential. Far from the Dirac point, C_q increases while C_{ox} does not change. So, in that region, the quantum capacitance may be neglected if its value becomes much larger than the geometrical capacitance.

Similar to the inductors, the FOMs of a capacitor is the Q-factor and is expressed as:

$$Q_{factor} = -\frac{\text{Imag}[Y_{12}]}{\text{Real}[Y_{12}]} = \frac{jZ_C}{R} = \frac{1}{wCR} \tag{2.4}$$

where Y_{21} is an admittance parameter, Z_C is the capacitor's impedance, C and R are the capacitance and resistance of the inductor, and w is the angular frequency.

2.3 2D Active Component

Active components are defined as electronic components that can introduce energy into a circuit. They also may have a source of power. This definition of components includes transistors and diodes. Transistors are usually used as amplifiers. As for the diodes they are usually used as signal rectifiers since they only allow current to flow in one direction. This section will explore Graphene Field-Effect Transistors (GFETs) and 2D-based diodes.

2.3.1 Graphene-based transistors

Transistors are one of the essential components of modern electronics and can be found in almost every electronic system to amplify or switch electrical signals. There are several types of transistors, the most relevant for micro and nanoelectronics being the Field Effect Transistor (FET). These devices are based on channel conductance modulation by applying a voltage to the gate. It means the current that flows between the drain and source terminals, Extrinsic drain-source current (I_{DS}), can be controlled using a gate voltage applied to a third contact, which is electrically insulated from the other two. The gate contact and the FET channel coupling are capacitive and have been discussed to some extent in the previous section.

The most important part of the transistor is the channel, which forms in the semiconductor material at the interface with the gate dielectric. Most common chips use transistors with silicon channels and rely on reducing the channel's size to improve its overall performance. In simple terms, reducing transistors size allows for more integration in the same chip area, increasing the chip performance and speed. However, due to short-channel effects and transistor Cu interconnects heating due to increased speed, their downscaling is becoming a considerable challenge. To overcome this issue and ensure technological advancement, further research on new materials to replace silicon must be undertaken. As a result of the effort to find new materials to replace silicon, 2D materials appeared as a possible solution because of their high saturation velocity and high carrier mobility, being the most promising graphene and MoS_2. These materials can be used in transistors for RF applications, such as oscillators, frequency multipliers, transceivers, or mixers.

2.3.1.1 Most Common Topologies for Transistors

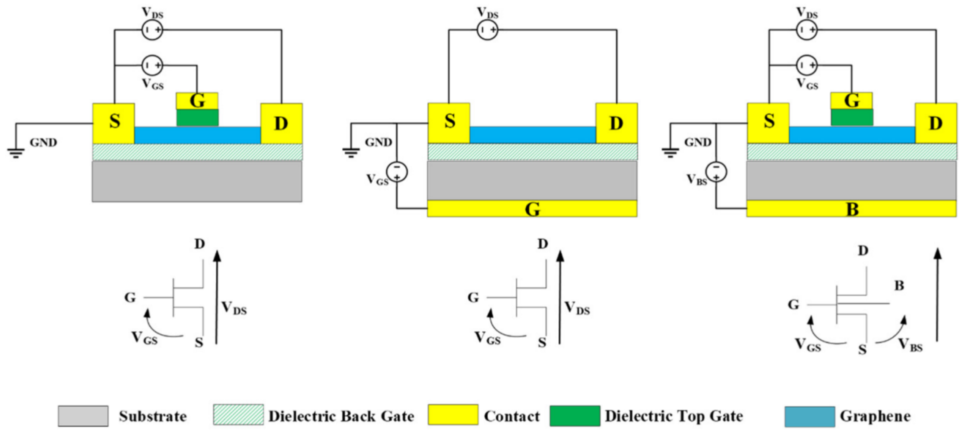


Figure 7: Top-gated (left), back-gated (centre) and top/back-gated (right) graphene transistors [32].

The common topologies of GFETs are those found in other technologies, namely top-gated, back-gated, and top/back-gated GFETs, Figure 7. What gives the name to these topologies is the position of the gate relative to the channel. Although the difference between these topologies may look simple, changing the position of the gate has implications on the fabrication methodology, expected performance, modelling considerations, and applications.

Top-gated GFETs are reported in the literature with their implementation on RF applications, biosensors, and liquid-gate GFETs. This approach is excellent when having greater control over the channel modulation while using a lower gate bias by using a thin gate oxide layer is necessary. However, the major problem with this topology is the need to grow an oxide layer on top of the graphene without damaging its structure and consequently degrading its carrier mobility. To overcome this issue, researchers are trying new approaches, such as the physical transfer of a nanowire to function as a gate electrode or the use of hBN, or the refinement of standard fabrication techniques like Atomic layer deposition (ALD) or thermal growth.

Back-gated structures expose the channel, allowing the graphene's surface to interact with light or molecules. Both interactions produce changes in graphene's properties and therefore changes in the transfer characteristic, allowing the evaluation of the element that caused the change. This behaviour makes back-gated GFETs suitable for biosensors and photodetectors. The major problem with this approach is often the necessity of high voltage to control the device, which is a drawback for most common applications.

Top/back-gated structures are used when it is advantageous to split the DC and Alternating current (AC) parts of the gate voltage and apply them to different contacts. In this way, a constant quiescent bias can be applied to the back gate – setting the transistor functioning point – while a signal is applied to the top gate in this case, modulating the transfer characteristics around the GFET quiescent point. Since GFET technology is still early, researchers use this topology to tune all their devices equally. Another architecture reported in [33] uses a receded gate geometry. It is adequate for liquid-gate transistors working as chemical sensors since, like in the bottom gate case, it leaves the channel accessible for the molecules in the solution. Moreover, it uses the EDL formed at the solid-liquid interfaces as the gate dielectric, providing a supercapacitor that allows operation at very low voltage, which is critical when dealing with biomolecules, cells, and microorganisms.

Table 1: GFETs found in the literature. Adapted from [32].

	Purpose	**Graphene Type**	**Differentiating Approach**	**Performance**	**Ref**
Top gated	Achieve high transconductance and drain-current saturation	CVD	Self-aligned source/drain electrodes	Maximum $g_m = 250\ \mu S/\mu m$	[34]
	RF applications	Mechanical exfoliation	Nanowire as the gate and self-aligned source/drain	Maximum $g_m = 1.27\ \mu S/\mu m$ and intrinsic $f_T = 300\ GHz$	[35]

Top gated	Improve the drain-current saturation	CVD	Thin Al_2O_3 gate oxide dielectric ($\approx 4\ nm$)	$\frac{f_{max}}{f_T} > 3$ $A_v > 30\ dB$	[36]
	RF applications	Mechanical exfoliation	Dual top gate	Maximum $g_m = 550\ \mu S/\mu m$ and intrinsic $f_T = 14.7\ GHz$	[37]
	RF applications	CVD	T-shaped gate and drain/source	Intrinsic $f_{max} = 200\ GHz$ and extrinsic $f_{max} = 106\ GHz$	[38]
	DNA biosensor	CVD	Liquid gate and PDMS well to isolate source/drain electrodes	Detection of full hybridization of the complementary strand down to $15\ aM$	[39]
Back gated	Study of velocity saturation: design and performance	Pulsed CVD	Use the h-BN as a gate oxide. Dual-gate device	$\frac{f_{max}}{f_T} > 5$	[40]
	Achieve high f_{max}	CVD	Buried gates to reduce gate resistance	Intrinsic $f_T = 35\ GHz$ and $f_{max} = 50\ GHz$	[41]
	Achieve high f_{max}	CVD	T-gate structure to reduce the gate resistance	Extrinsic $f_T = 11.4\ GHz$ and $f_{max} = 15\ GHz$	[42]
	Improvement of the process-induced mobility degradation of graphene	CVD	Development of buried gates	$I_{on}/I_{off} = 5.31$ Maximum $g_m = 6.85\ \mu S/\mu m$ Intrinsic $f_T = 2\ GHz$ and $f_{max} = 13\ GHz$	[43]
	High-sensitivity label-free DNA biosensor	CVD	Electrolysis bubbling method for graphene transfer	The detection limit depends on the length of the DNA	[44]
	Graphene FET biosensor for the label-free sensing of exosome	CVD	Back gate contact made with silver paint	Exosome detection of at least $0.1\ \mu g/ml$	[45]
Top/back gated	GFET	Mechanical exfoliation	Gate oxide (Al_2O_3) deposited by ALD	Preservation of graphene mobility after gate dielectric deposition ($8000\ cm^2V^{-1}s^{-1}$)	[46]

Top/back gated	Frequency doubler	Mechanical exfoliation	Yttrium oxide as gate dielectric	Able to work with 200 kHz input frequencies	[47]
	RF applications	Mechanical exfoliation	h-BN used as top and back gate dielectric	Current density of 1.2 A/mm Extrinsic $f_T = 33\ GHz$	[48]

GFETs have some unique characteristics, which are a consequence of graphene Densisty of states (DOS) and its conduction electrons. The first is that they cannot be turned off. Conventional transistors have a threshold gate voltage below which no current flows between the drain and source and are turned off. This property allows conventional transistors to be used in digital systems. On the contrary, GFETs do not have a minimum gate voltage to turn on. They have a specific voltage where they exhibit the minimum I_{DS}, which is called the Dirac voltage. The second unique property of GFETs is their ambipolar character. Whereas, for example, silicon FETs are either n- or p-type, but not both simultaneously, because their doping is achieved by impurity doping, which acts as donors (n-doping) or acceptors (p-doping), but not both, GFETs can be seen as p- and n-type transistors in the same device, whereby adjusting the gate voltage to the left or right of the Dirac voltage switches from p- to n-type. Although this is an obstacle for digital applications, it is possible to implement them in analogue systems. These analogue systems can be biosensors, flexible electronics, or RF circuits. The third unique property of GFETs stems from graphene's very high carrier mobility, which is essential for developing transistors with high Cut-off frequency (f_T) or biosensors with exceedingly high sensitivity. GFETs with $f_T = 100\ GHz$ were reported in [49], and many others and the purpose of their investigation can be seen in Table 1. GFETs found in the literature are not easy to replicate, so further research is still needed to integrate these devices into a system.

Unlike GFETs, MoS_2 FETs can be turned off like conventional FETs. Therefore, MoS_2 FETs can be used in digital systems, which makes them a possible replacement for silicon-based transistors. MoS_2 Single layer FETs with f_T of $6.7\ GHz$ and Maximum oscillation frequency (f_{max}) of $5.3\ GHz$ were reported in [50]. Although the design frequencies and the carrier mobility in MoS_2 are lower than the graphene, the presence of a bandgap enables more significant voltage gain compared to GFETs. In another publication, by using a few-layer MoS_2 it was achieved a f_T of $42\ GHz$ and f_{max} of $50\ GHz$ [51]. Although MoS_2 FETs may look great, the low mobility of MoS_2 can be a limitation for their application in the higher frequency domain. The lack of models makes it difficult to predict the behaviour of these devices, and the state-of-the-art of such devices is still too poor compared to GFETs. Further research is needed to understand the true potential of these devices.

2.3.1.2 Modelling of 2D materials-based transistors

Simulating a device's performance is a crucial success factor of modern electronics. Because of that, modelling GFETs plays a vital role in helping researchers achieve GFETs' best performance and understanding if their implementation in more complex devices is reliable, allowing for the substitution of silicon transistors.

Many papers try to achieve the closest and more reliable GFET model possible. In [52], the authors take a different approach. Instead of relying only on measured data, they try to predict the transistor behaviour using analytical expressions and some tabulated values of the materials' properties. With their work, the authors implemented a compact equivalent circuit that evaluates the value of I_{DS} in the three working regions and verified the model against experimental DC data. The significant difference between the models presented here is that one relies on measured data to analyse the RF performance, and the other using only theoretical data, can predict the DC behaviour of the transistor.

Like all transistors, GFETs can be modelled using the small-signal model, which is done in [53]. In this paper, the authors use a fixed transconductance (g_m) to simulate the Scattering parameters (S-params), and because of that, the generalization of this model becomes difficult since operating the GFET around the Dirac point is especially important to some applications like the ring oscillator, and close to this point g_m changes a lot. Another paper shows a similar approach to the previous one mentioned, but instead of using a fixed g_m, they use a set of equations to model the current source, allowing for both DC and large-signal simulations. Reported in the literature are several models that try to predict the behaviour of the GFET, and by taking different approaches, they can predict its behaviour in a closed operation zone. To replace silicon, the GFET model needs to be standardized in all operation zones, allowing researchers and chip manufacturers to design and predict the device performance accurately.

The FOMs of GFET are the f_T and f_{max}. The f_T is defined as the frequency at which the magnitude of the small-signal current gain is unitary ($H_{21} = 0\ dB$). This FOM is usually extracted from the H_{21} parameter, which is obtained by the measurement and conversion of the S-params of the device, using the following expression:

$$H_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \tag{2.5}$$

Also, to predict the f_T, it is generally used the following expression:

$$f_T = \frac{g_m}{2\pi \left[(C_{gs} + C_{gd})(1 + (R_d + R_s)g_{ds}) + C_{gd}g_m(R_d + R_s) + C_{pg} \right]} \tag{2.6}$$

The f_{max} is described as the frequency when the Maximum Gain (U/MAG/MSG) becomes unitary ($U/MAG/MSG = 0\ dB$). This gain is not directly calculated, it must satisfy some conditions [54]. By using the S-params, the first thing to evaluate is the stability factor for all frequencies using the following expression:

$$k = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2\,|S_{12}|\,|S_{21}|} \quad \equiv \quad \text{Stability Factor} \tag{2.7}$$

Afterwards comes the evaluation of all k's. If all k's are less than one ($k < 1$ for all frequencies), the U/MAG/MSG corresponds to the Mason's Gain (U), and it can be calculated using the following expression:

$$U = \frac{\left|\frac{S_{12}}{S_{12}} - 1\right|^2}{2k\left|\frac{S_{21}}{S_{12}}\right| - 2\,\text{Real}\left[\frac{S_{21}}{S_{12}}\right]} \quad \equiv \quad \text{Mason's Gain} \tag{2.8}$$

If all k's are not less than one, for each frequency must be evaluated if k is less or greater than one. If k is less than one $(k < 1)$, the U/MAG/MSG corresponds to the Maximum Stable Gain (MSG) and can be calculated using the following expression:

$$MSG = \frac{|S_{21}|}{|S_{12}|} \quad \equiv \quad \text{Maximum Stable Gain} \tag{2.9}$$

If k is greater than one $(k > 1)$, the U/MAG/MSG corresponds to the Maximum Available Gain (MAG) and can be calculated using the following expression:

$$MAG = MSG \cdot (k - \sqrt{k^2 - 1}) \quad \equiv \quad \text{Maximum Available Gain} \tag{2.10}$$

Finally, the U/MAG/MSG can be converted to dB by the evaluation of ten times the logarithmic of each value of U/MAG/MSG $(U/MAG/MSG(dB) = 10\log_{10}(U/MAG/MSG))$.

Like for f_T, there is a general expression used to try to predict f_{max}, and it is the following:

$$f_{max} = \frac{f_T}{2\sqrt{g_{ds}(R_g + R_s) + 2\pi f_T R_g C_{gd}}} \tag{2.11}$$

2.3.2 2D material diodes

A diode is an electronic component that allows current to flow in one direction while it blocks transport in the reverse direction, thus rectifying the electric signal. The most common semiconductor diode type is a p-n junction. The p-n junction induces an electric field in a space-charge carrier-depleted volume, enabling current rectification. There are homo- and hetero-junctions, depending on if both sides of the junction are made of the same or different materials. 2D materials junctions can be made 2-dimensional or 1-dimensional. Some authors add a gate to the junction diode to tune the chemical potential on one or both sides of the junction, thus controlling the barrier height and improving the device's performance.

2.3.2.1 Most common topologies

P-n junctions based on 2D materials can be made of only one material (2D homostructures), two different materials (2D heterostructures), or different dimensions materials (mixed-dimensional) [55]. 2D homostructures can be obtained using various methods, which are:

- **Thickness-based:** p and n regions are formed by regions with different thicknesses.
- **Electrostatically doped:** p and n regions are obtained using local gates.
- **Chemical doping:** p and n regions obtained by the surface adsorption of molecules, nanoparticles or quantum dots.
- **Elemental doping:** 2 flakes with different doping are stacked.

2D heterostructures can be:

- **Vertical:** stacking two different 2D materials on top of each other.
- **Lateral:** combining two different 2D materials on the same plane.

Mixed-dimensional can be:

- **2D-0D and 2D-1D:** 2D-0D and 2D-1D material junctions.
- **2D and 3D:** stacking of 2D and 3D material on top of each other.

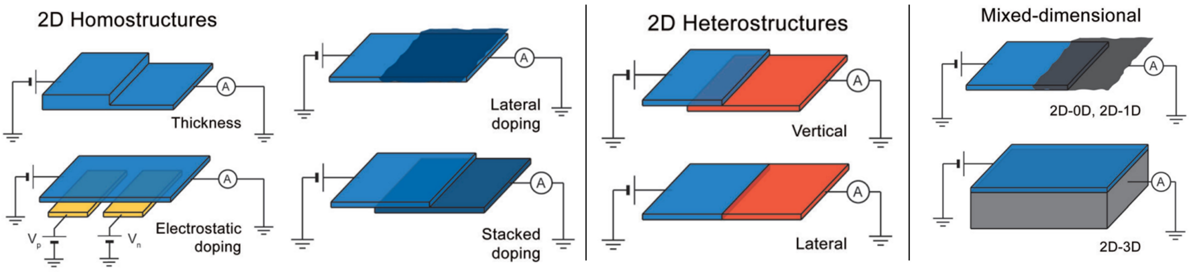


Figure 8: Topologies of different p-n junctions [55].

A thickness-based diode using MoS_2 is reported in [56], with a rectification ratio of $\approx 10^3$ and a small ideality factor (a value that compares the diode with the ideal diode) of 1.95. Besides the good electronic properties, it also has good photoresponsivity of $10\ A/W$ and high photosensitivity of 10^5.

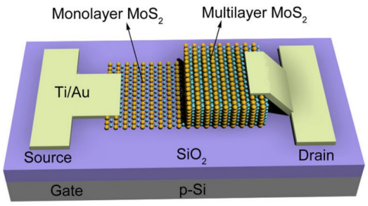


Figure 9: Schematic of the thickness-based diode [56].

In [57], it is reported that two different mixed dimension-based diodes are similar to metal-insulator-metal (MIM) diodes, but one of the metals is replaced by graphene, creating a metal-insulator-graphene interface (MIG). The difference between both approaches is the type of interface between graphene and the insulator, being a 2D or One dimensional (1D) interface. From the 2D to 1D interface, the capacitance and series resistance decreases, allowing to fully exploit the high mobility of graphene, which increases the device f_T (predicted to be up to $2.4\ THz$) and current density (from 7.5 [58] to $7.5\times10^{6}Acm^{-2}$ [59]).

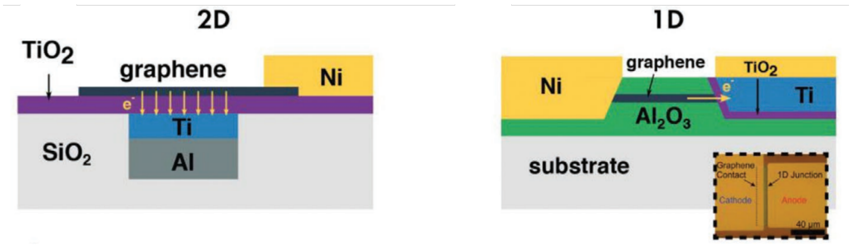


Figure 10: Schematic of the 2D (left) and 1D (right) MIG diodes [57]

2.3.2.2 Modelling of 2D materials based diodes

The modelling of 2D materials diodes has not been well explored, so modelling such devices relies on parameter extraction. In [60], it is described as a small signal equivalent, Figure 11, that is composed of a liner capacitance, C_1, and nonlinear bias-dependent capacitance, C_2, two leakages variable resistances, R_1 and R_2, and the graphene sheet resistance, R_G. In addition to the intrinsic region, the model also includes extrinsic parasitics.

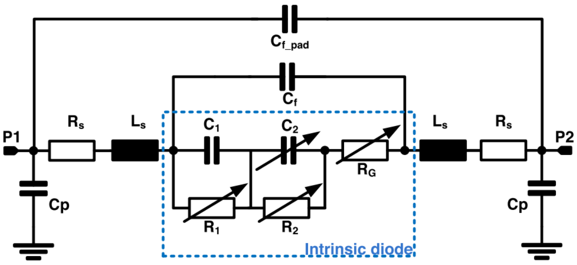


Figure 11: Small-signal equivalent circuit model of diodes [60].

2.4 Graphene Devices

Due to the high conductivity of graphene, GFETs can have large values of f_T and f_{max}. Therefore, GFETs are becoming the focus of much research for RF devices like frequency multipliers, mixers, and oscillators.

2.4.1 Graphene frequency multipliers

Due to the V-shaped transfer curve of GFETs, it is possible to obtain a frequency doubler when operating at the Dirac point. In simple terms, if a signal with DC bias equal to the Dirac point of the transistor is applied to the gate, V_{GS}, the output current I_{DS} has double the frequency.

In [47], a top/back-gated against back-gated frequency doubler is studied, showing a significant improvement in the operating frequency from $10\ kHz$ to $200\ kHz$ when the top gate is added to the back-gated device. For the top/back-gated device, the output power is concentrated at $400\ kHz$ with a relative power of $\approx 75\%$. Another frequency doubler on a flexible substrate is reported [61], which achieved a spectral purity higher than 97% and a high conversion gain of $-13\ dB$.

A W-shaped transfer curve is obtained when two GFETs with different Dirac points are combined in series. When operating at different points of the W-shape, it is possible to get a frequency tripler or quadrupler. A frequency tripler is reported in [62] with spectral purity higher than 70% at an output frequency of $600\ Hz$.

A different approach is implemented in [63] and [64], where the W-shaped transfer curve is achieved with a single GFET by biasing the back and top gate of top/back-gated transistors. In [63], a frequency tripler is studied, and a device with spectral purity higher than 90% was achieved at an output frequency of $3\ kHz$. In [64] a frequency quadrupler with spectral purity of 50% at $800\ kHz$ was reported.

2.4.2 Graphene mixers

It is reported in [65] that it is possible to implement an RF mixer with operating frequencies up to $10\ GHz$ while having a high conversion loss of $\approx 30\ dB$ at $1\ GHz$ using a single GFET. Another graphene RF mixer is studied in [66], where frequencies up to $10\ GHz$ and excellent thermal stability were achieved, being its peak performance around $4.5\ GHz$ with a conversion loss of $\approx 27\ dB$. In another study, [67], the authors study the effects of reducing channel length on the graphene mixer. With this study, the authors concluded that the conversion loss increases by decreasing the channel length while the Third-order Intercept Point (IIP3) increases.

2.4.3 Ring oscillators

Another implementation of graphene transistors is reported in [68]. In this paper, the authors propose the implementation of GFETs as ring oscillators. A ring oscillator is a circuit built of an odd number of cascaded logic inverters in a loop. This loop induces instability and therefore induces oscillations at high frequencies. Each inverter must be identical, and over-unity voltage gain $(A = g_m/g_{ds} > 1)$ is required. The FOM used for this kind of device is the maximum oscillation frequency, f_O, since it is smaller than f_T. Although the positive voltage of the drain induces a shift on the Dirac point [69], the complementary GFETs of the inverters were obtained using a back gate voltage to ensure a proper change of the Dirac point. In this study, the authors made three types of devices: large ($L = 3\ \mu m$ and $W = 20\ \mu m$), medium ($L = 2\ \mu m$ and $W = 10\ \mu m$) and small ($L = 1\ \mu m$ and $W = 10\ \mu m$), obtaining $284\ MHz < f_O < 350\ MHz$, $504\ MHz < f_O < 750\ MHz$ and $1\ GHz < f_O < 1.28\ GHz$ for each device, respectively.

A similar ring oscillator is presented in [70], in which the authors also studied the effects of changing the transistors' channel size, access length, and source and drain contact thickness. The best device achieved a $f_O = 4.3\ GHz$.

2.4.4 LC tank oscillators

Although full graphene-based LC tank oscillators have not been accomplished yet, the implementation of graphene inductors, capacitors, and transistors alone to study their performance in LC tank oscillators has been reported.

The capacitor developed in [31] was implemented in an LC tank by adding a $2\ mH$ inductor in series, achieving a tunable resonant tank from 1.45 to $1.73\ MHz$ and Q-factor ranging from 65 to 25.

In [71], the performance of a graphene LC tank used in an oscillator was assessed through simulation. This simulation relied on graphene capacitor and inductor values found in the literature, and an oscillation frequency of $1.5\ GHz$ was achieved with a phase noise of $-134\ dB/Hz$.

2.5 Discussion

From the information gathered in this chapter, it can be concluded that state-of-the-art on 2D material-based device modelling for circuit-level simulation is too poor. Most of the research in this field is done towards fabrication due to the yearly stage of the investigations. State-of-the-art in graphene-based capacitors and inductors fabrication and modelling for RF applications is not as explored as for GFETs. So, since the GFET shows more interest but lacks a well-defined set of equations to define the device's behaviour, GFET models must be pushed forward to assist investigations in this field. Following this line of thought, the following chapters will present a comparison study between three models proposed in the literature, both in DC and RF domains, to understand which one is most reliable for circuit-level simulation.

3

Device modelling

Performance assessment of standard transistors plays an important role when designing a device, which is also true regarding graphene transistors. Therefore, the ability to simulate and predict the device's performance is essential, be it to reduce the trials when it comes to the design or to ensure the whole process goes right.

There are three types of models: Analytical Model (AM), Semi-Empirical Model (SEM) and Empirical Model (EM). AM provides an understanding of the device behaviour based on a set of equations. The SEM rely on parameters extracted from fabricated devices but are less complicated and can be easily implemented in standard EDA tools. Finally, the EM are similar to the SEM but can only simulate the device behaviour in a single operating point.

As discussed in 2.3.1.1, there are three topologies of GFETs: top-gated, back-gated and top/back-gated. The overall operation of the three topologies is the same, whereby applying a static differential potential between the drain and source terminals, there is a current that flows between those terminals, which can be modulated by a second voltage between the gate and source terminals. When introducing a second gate, usually a back gate, it is possible to shift the Dirac point, tuning the device to the desired end. This behaviour is what many proposed models try to achieve, but only the following three will be discussed due to their compatibility with EDA tools as well as close results with real devices.

In the following section, it is essential to distinguish the intrinsic from the extrinsic nodes, so the intrinsic nodes are referred to with a lowercase subscript (e.g. Intrinsic gate-source voltage (V_{gs})) and extrinsic nodes with an uppercase subscript (e.g. Extrinsic gate-source voltage (V_{GS})).

3.1 Parameters extraction

To better understand what is happening in the device, GFETs are characterised in two domains, the DC and RF domains. It is possible to extract the $I_{DS} - V_{GS}$ curve, g_m and graphene mobility from the DC domain. From the RF domain, it is possible to complement the DC measurements by allowing extraction of all the capacitances between interfaces, contact resistance and inductance and determine the FOMs of the transistor directly from the measurement.

3.1.1 DC analysis

The most standard system to measure the DC behaviour of a GFET, without a back gate, is composed of three probes, two sources with current and voltage readout (not necessary, but to ease the measuring process), and a microscope. The first step is to use the microscope to choose and place the probes on each terminal. After that is done and all the probes are connected to the sources (not to forget to merge the ground signals), a fixed V_D is applied to the drain, and by sweeping V_G register the I_{DS} values. Finally, a plot of $I_{DS} - V_{GS}$ with the registered data can be done. The exact process is done if another device must be measured. This process can be eased by using an automatic probe station, simply by calibrating the system to the position of the devices and then defining the range of voltages and the devices to measure, and the probe station takes care of all the work.

After measuring the $I_{DS} - V_{GS}$ profile, it is possible to obtain the g_m profile, Figure 12, by applying a numerical derivative to the data in the following way:

$$g_m[i] = \frac{I_{DS}[i+1] - I_{DS}[i]}{V_{GS}[i+1] - V_{GS}[i]} \tag{3.1}$$

where i is the nth measure.

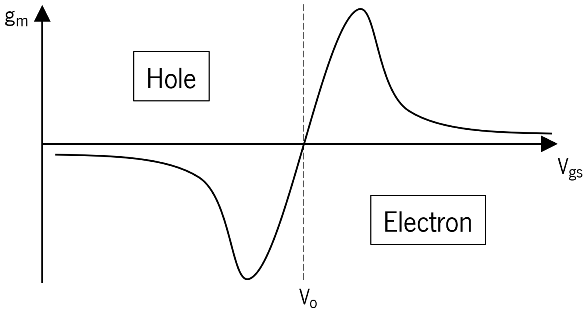


Figure 12: Transconductance profile.

To obtain the mobility of graphene the field-effect mobility equation for a FET is used :

$$\mu = \frac{L|g_m|}{WC_gV_{DS}} \tag{3.2}$$

where L and W are the channel length and width, C_g the gate capacitance per area. This method is generally used because of its simplicity, but it underestimates the mobility value as it does not consider contact resistance. If a more realistic measure is needed, it is recommended to do Hall measurements [72]. In 3.3.1 a method to extract the mobility will be presented by fitting the measurements with analytical equations.

3.1.2 RF analysis

Different from the DC measurements a more complex setup is needed for RF measurements. The GFET can be seen as a two-port system, which means a signal must be fed to the gate and another to the drain.

These signals are composed of a DC component, used to set a device operating point and an RF signal. A bias tee is used to merge the DC and RF signals. In simple terms, a bias tee is a device with two inputs and one output. One of the inputs is a RF signal (removes any DC component from it), and the other is a DC signal (removes any AC component from it). The output is the RF signal with the desired DC component, Figure 13.

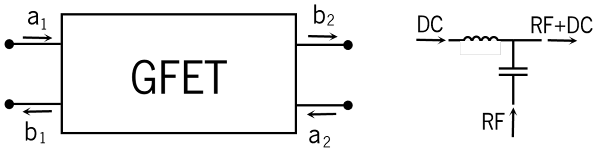


Figure 13: Two-port system GFET (left) and equivalent bias tee circuit (right).

The RF signal is sent by a Vector Analysis Network (VNA), and the same device reads the reflected and transmitted signals. The VNA is usually set up for a range of frequencies, and the device is responsible for sending the RF input signals as well as measuring the transmitted and reflected signals at each frequency, building the S-params matrix as follows:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.3}$$

where a is the input signal, b is the output signal, S_{11} is the input port voltage reflection coefficient, S_{12} is the reverse voltage gain, S_{21} is the forward voltage gain, and S_{22} is the output port voltage reflection coefficient.

From the S-params, it is possible to obtain more valuable parameters like the Hybrid parameters (H-params), from which it is possible to determine the f_T of the transistor and Admitance parameters (Y-params) and Impedance parameters (Z-params) that allow extracting values for the device's capacities, inductances and resistances to be used to model it.

Admittance is the inverse of impedance $\left(Y = Z^{-1}\right)$. From the S-params the Y-params are obtained as follows:

$$\begin{aligned} Y_{11} &= \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}Y_0 & Y_{12} &= \frac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}Y_0 \\ Y_{21} &= \frac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}Y_0 & Y_{22} &= \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}Y_0 \end{aligned} \tag{3.4}$$

where $Y_0 = Z_0^{-1}$ is the port admittance and Z_0 is the port impedance. Usually, the port impedances are the same and have a value of 50 Ω. The Z-params are obtained by inverting the above expressions of the Y-params. From the perspective of Y-params and Z-params, the two-port network equivalent circuits are represented in Figure 14. These circuits are essential because if the equivalent circuit of the measuring device is known, its component values can be extracted by comparing the parameters circuit with the device circuit.

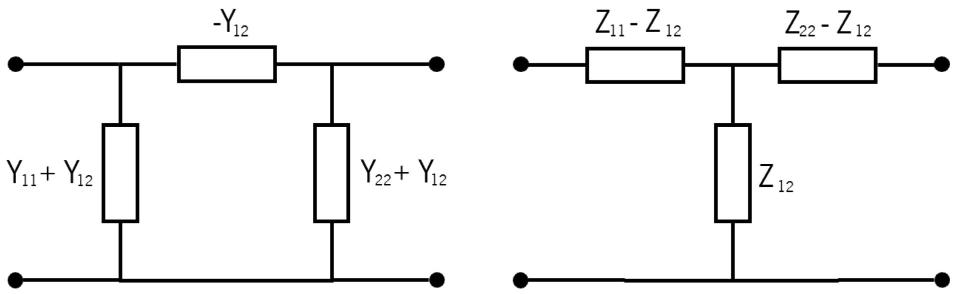


Figure 14: Two-port system equivalent circuit from the Y-parameters (left) and Z-parameters (right).

Every time a set of measurements is performed in the RF domain, the setup must be calibrated to remove the cables' and probes' added parasitic effects. This task is accomplished by measuring a standard impedance substrate and then subtracting it from the raw measurements of the device. Another factor that affects the device's performance is the parasitic elements like parasitic capacitances, represented in blue, and parasitic impedances, represented in green in Figure 15. The method to remove the effect of parasitic elements from the measured S-params is called Open-Short De-embedding. This method requires two extra structures to be fabricated alongside the device, the Short and Open structures. In the transistor case, the Short structure consists of shortening the channel, and the Open structure does not have a channel.

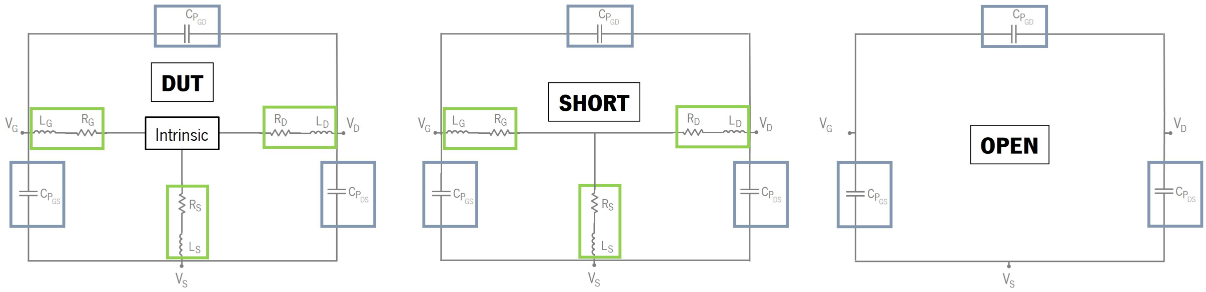


Figure 15: De-embedding equivalent circuits. The device under test (left) is the complete device, the short (centre) has the channel shorted to all contacts, and the open (right) has the channel open.

By looking at the Open equivalent circuit from Figure 15 and the Y-params equivalent circuit from Figure 14, and knowing that the admittance of a capacitor is $Y_C = jwC$, the following equations can be extracted:

$$C_{P_{GD}} = \frac{\text{Imag}\left[-Y_{O_{12}}\right]}{w} \qquad C_{P_{GS}} = \frac{\text{Imag}\left[Y_{O_{11}} + Y_{O_{12}}\right]}{w} \qquad C_{P_{DS}} = \frac{\text{Imag}\left[Y_{O_{12}} + Y_{O_{22}}\right]}{w} \tag{3.5}$$

where Y_O are the Y-params of the Open structure obtained by direct convertion of the same structure's measured S-params using the Equation 3.4.

Extracting the parasitic impedances from the Short circuit is not as direct as the previous method. By subtracting the Y_O from the Y_S, Y-params of the Short structure, and then converting to Z-params

$\left(Y_{OS} = Y_S - Y_O \Rightarrow Z_{OS} = \frac{1}{Y_S - Y_O}\right)$ only the green impedances remain, and by comparing to the Z-params equivalent circuit of Figure 14 and knowing that the impedance of a resistor in series with an inductor is $Z_{RL} = R + jwL$, the following equations can be extracted:

$$R_G = \text{Real}\left[Z_{SO_{11}} - Z_{SO_{12}}\right] \qquad R_D = \text{Real}\left[Z_{SO_{22}} - Z_{SO_{12}}\right] \qquad R_S = \text{Real}\left[Z_{SO_{12}}\right] \tag{3.6}$$

$$L_G = \frac{\text{Imag}\left[Z_{SO_{11}} - Z_{SO_{12}}\right]}{w} \qquad L_D = \frac{\text{Imag}\left[Z_{SO_{22}} - Z_{SO_{12}}\right]}{w} \qquad L_S = \frac{\text{Imag}\left[Z_{SO_{12}}\right]}{w} \tag{3.7}$$

The final step is to remove both the parasitic capacitances and impedances from the Device Under Test (DUT). So, to perform the de-embedding process, the first step is to remove the parasitic capacitances using the Y-params of the Open structure and then remove the parasitic impedances using the Z-params obtained to extract parasitic impedances, Y_{OS}. So, the final expression for the Y-params of the intrinsic device is:

$$Y_{intrinsic} = \frac{1}{\frac{1}{Y_{DUT} - Y_O} - \frac{1}{Y_S - Y_O}} \tag{3.8}$$

The values of the intrinsic components can be obtained by comparing the Y-params equivalent circuit to the device's intrinsic equivalent circuit.

3.2 Analytical Model

In [52] an AM was proposed that captures the three operating regions of the GFET while allowing the model to be compatible with EDA tools. This model only captures the intrinsic part of the device, so the downside of this model is that it is only suitable for DC or low-frequency analysis. Since the other models described in this document do not consider a back gate, the back gate described in the above-mentioned paper is ignored.

As shown in Figure 16, the proposed model assumes an equal access resistance from the contacts to the channel, R_S, a capacitance between the gate and the channel, C_g, a current source, I_{ds}, and a variable quantum capacitance, C_q.

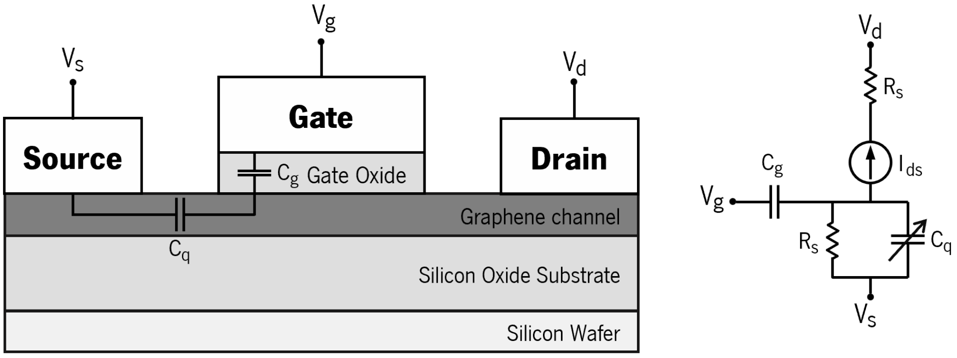


Figure 16: Top-gated graphene transistor layout (left) and proposed equivalent circuit model (right).

The quantum capacitance measures the energy required to pump carriers into the channel and has the same V-shape as the GFET characteristic DC response. In this model, it is described as the sum of minimum quantum capacitance that occurs at the Dirac point, $C_{q_{min}}$, plus a variable quantum capacitance, $C_{q_{var}}$ $\left(C_q = C_{q_{min}} + C_{q_{var}}\right)$. Both quantities can be evaluated using the following equations:

$$C_{q_{min}} = \frac{q^2\sqrt{n_o}}{\sqrt{\pi}\hbar v_F} \tag{3.9}$$

$$C_{q_{var}}(\varphi_s) = \frac{2q^2k_BT}{\pi\left(\hbar v_F\right)^2}\ln\left[2\left(1+\cosh\left(\frac{q\varphi}{k_BT}\right)\right)\right]LWN \approx q^2\frac{2}{\pi}\frac{q|\varphi_s|}{(\hbar v_F)^2} \tag{3.10}$$

where q is the electron charge, n_0 is the minimum carrier density, $\hbar$ is the reduced Plank's constant, v_f is the fermi velocity and φ_s is the surface potential. The reduced form of the Equation 3.10 is only valid when the energy of moving charges in the channel is much larger than the thermal energy, $q\varphi_s >> k_BT$.

The surface potential is given by:

$$\varphi_s = \frac{C_g(V_{gs}-V_o)}{C_g + C_{q_{min}} + \frac{1}{2}C_{q_{var}}(\varphi_s)} \tag{3.11}$$

By solving a system of equations with Equation 3.10 and Equation 3.11 rises two solutions for the surface potential, a positive Equation 3.12 and a negative Equation 3.13.

$$\varphi_s^+ = -\frac{\delta C_{q_{var}}}{\delta\varphi_s}\left[C_g + C_{q_{min}} - \sqrt{2\frac{\delta C_{q_{var}}}{\delta\varphi_s}C_g(V_{gs}-V_o) + (C_g + C_{q_{min}})^2}\right] \tag{3.12}$$

$$\varphi_s^- = \frac{\delta C_{q_{var}}}{\delta\varphi_s}\left[C_g + C_{q_{min}} - \sqrt{-2\frac{\delta C_{q_{var}}}{\delta\varphi_s}C_g(V_{gs}-V_o) + (C_g + C_{q_{min}})^2}\right] \tag{3.13}$$

where $\frac{\delta C_{qvar}}{\delta\varphi_s} = q^2\frac{2}{\pi}\frac{q}{\left(\hbar v_f\right)^2}$. For a particular point of operation, the solution for the surface potential is either a positive or negative solution. It must have the assumed sign, and it is a real number.

Similar to standard FETs, GFETs have a triode region and a unipolar saturation region, but instead of a cut-off region, they have an ambipolar saturation region. In the triode and unipolar saturation regions, the conduction is done only by holes or electrons, whereas in the ambipolar saturation region, conduction is done by both holes and electrons. For both hole and electron conduction, these regions are limited by Intrinsic drain-source voltage (V_{ds}) voltages that will later be defined using numerical equations.

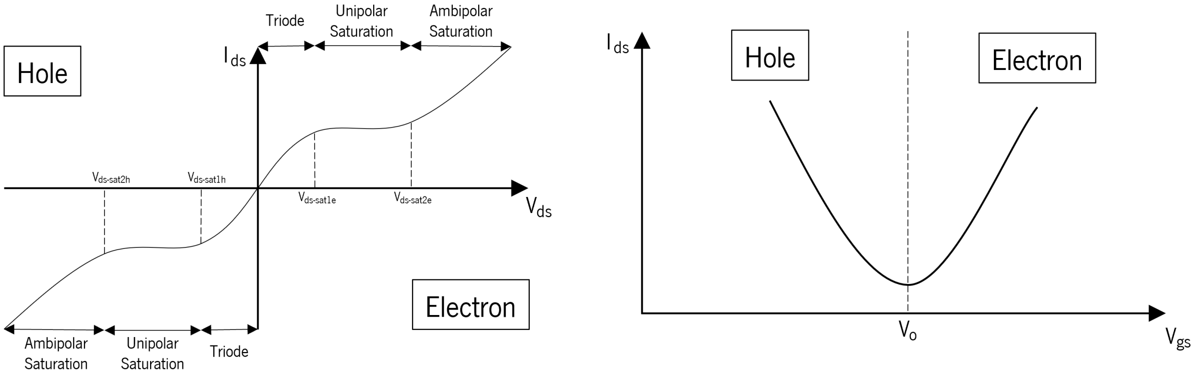


Figure 17: GFET characteristic curves: I_{ds} vs V_{ds} (left) and I_{ds} vs V_{gs} (right).

This model derives I_{ds} equations using the drift-diffusion model for hole and electron separately since the type of carrier is the majority depending on the gate bias. The solutions are as follows:

Table 2: Analytical model equations from [52].

	Hole $(V_{gs} < V_o)$	**Electron** $(V_{gs} > V_o)$
Triode	$\frac{1}{4R_s}\left[-V_c - V_{ds} + 2Y\left(\frac{V_{ds}}{2} - V_{ov}\right)\right.$ $\left.-\sqrt{\left(V_c - V_{ds} + 2Y\left(\frac{V_{ds}}{2} - V_{ov}\right)\right)^2 - 4V_cV_{ds}}\right]$	$\frac{1}{4R_s}\left[V_c - V_{ds} - 2Y\left(\frac{V_{ds}}{2} - V_{ov}\right)\right.$ $\left.-\sqrt{\left(-V_c + V_{ds} + 2Y\left(\frac{V_{ds}}{2} - V_{ov}\right)\right)^2 + 4V_cV_{ds}}\right]$
Limit 1 $(V_{ds_{sat1}})$	$\frac{1}{(1+Y)^2}[2V_{ov}Y(1+Y)+$ $(1-Y)(V_c - \sqrt{V_c^2 - 2V_cV_{ov}(Y+1)})]$	$\frac{1}{(1+Y)^2}[2V_{ov}Y(1+Y)+$ $(Y-1)(V_c - \sqrt{V_c^2 + 2V_cV_{ov}(Y+1)})]$
Unipolar Saturation $(I_{ds_{sat}})$	$\frac{1}{R_s(1+Y)^2}[-V_c + (1+Y)V_{ov}+$ $\sqrt{V_c^2 - 2(1+Y)V_cV_{ov}}]$	$\frac{1}{R_s(1+Y)^2}[V_c + (1+Y)V_{ov}-$ $\sqrt{V_c^2 + 2(1+Y)V_cV_{ov}}]$
Limit 2 $(V_{ds_{sat2}})$	$V_{ds_{sat1}} - \frac{1}{2}\lvert V_{ov} - V_{ds_{sa1}}\rvert$	$V_{ds_{sat1}} + \frac{1}{2}\lvert V_{ov} - V_{ds_{sa1}}\rvert$
Ambipolar Saturation	$I_{ds_{sat}} - \frac{W}{2L}\mu_h C_{top} V_{ds_{sat2}}^2 \left(\frac{V_{ds}}{V_{ds_{sat2}}} - 1\right)^2$	$I_{ds_{sat}} + \frac{W}{2L}\mu_e C_{top} V_{ds_{sat2}}^2 \left(\frac{V_{ds}}{V_{ds_{sat2}}} - 1\right)^2$

$$V_c = Lv_{sat}/\mu \qquad Y = BWv_{sat}C_{top}R_s \qquad V_{ov} = V_{gs} - V_o \qquad C_{top} = \frac{C_g C_p}{C_g + C_q} \qquad v_{sat} = \mu E_c$$

where W and L are the width and length of the channel, v_{sat} is the saturation velocity, μ_n is the carrier mobility, E_c is the critical electric field, β is a fitting parameter that can go from 1 to 1.4 and C_{top} is the effective gate capacitance.

3.3 Semi-empirical Model

A large signal model is proposed in [73], which allows for DC and RF analysis while being compatible with EDA tools. This model shows excellent results with measured devices since, unlike other models, it captures the difference in contact depending on the carrier type in the channel due to charge transfer between graphene and metal contacts. This difference in the contact resistance reflects an asymmetry in the transfer curve of the GFET.

This model can be divided into two parts, the intrinsic and extrinsic parts. In DC and low frequency, the extrinsic part can be ignored, but at larger frequencies, the extrinsic part becomes relevant and must be accounted for RF simulation to best match real results. Being a SEM, it relies on extracted parameters from fabricated devices, allowing for better approximation between measured and simulated results. This model is composed of a current source, I_{ds}, gate resistance and inductance, R_G and L_G, drain resistance and inductance, R_D and L_D, source resistance and inductance, R_S and L_S, drain-to-source capacitance, C_{ds}, the gate-to-drain capacitance, C_{gd}, the gate to source capacitance, C_{gs} and parasitic gate-source, gate-drain and drain-source capacitances, $C_{P_{GS}}$,$C_{P_{GD}}$ and $C_{P_{DS}}$.

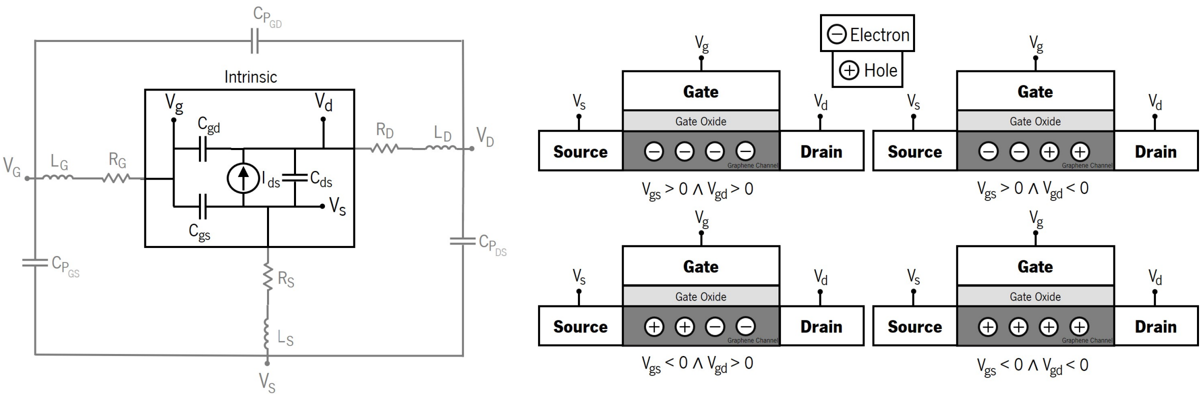


Figure 18: Large-signal model equivalent circuit (left) and majority carrier type in the graphene channel in different voltage bias (right).

The authors took advantage of the symmetric structure of the device to model I_{ds} using V_{gs} and Intrinsic gate-drain voltage (V_{gd}) as variables since, depending on the combination of these voltages, the type of majority carrier in the channel changes. As can be seen in Figure 18, there are four situations. If both voltages are greater than zero, the transport in the channel is done by electrons. If both voltages are lower than zero, the transport is done by holes. The other two situations are a mix of carriers, where the holes are closer to positive voltage and electrons closer to the negative potential.

A quantum capacitance was used in the previous model, but it can be ignored most of the time due to its greater values than the geometrical gate capacitance. Since it appears in series with the geometrical capacitance, the smallest capacitance dominates. This approximation only becomes a problem when ultrathin gate dielectric is used (dielectric thickness lower than $10\ nm$ [74]). Having this in mind, the authors decided to ignore quantum capacitance allowing for a simpler model. Like the previous model, the drift-diffusion model was used to get an expression for the four situations discussed above, obtaining the following expressions:

$$I_{ds_1} = \frac{u_e V\_o Q_o}{\sqrt[m]{1+\left(\frac{u_e\left|V_{gs}-V_{gd}\right|}{L\bar{v}_{sat}}\right)^m}} \frac{W}{L} f\left(\bar{V}_{gs}, \bar{V}_{gd}\right) \tag{3.14}$$

$$I_{ds_2} = \frac{u_e V\_o Q_o}{\sqrt[m]{1+\left(\frac{u_e\left|V_{gs}-V_{gd}\right|}{L\bar{v}_{sat}}\right)^m}} \frac{W}{L} f\left(\bar{V}_{gs}, 0\right) + \frac{u_h V\_o Q_o}{\sqrt[m]{1+\left(\frac{u_h\left|V_{gs}-V_{gd}\right|}{L\bar{v}_{sat}}\right)^m}} \frac{W}{L} f\left(0, \bar{V}_{gd}\right) \tag{3.15}$$

$$I_{ds_3} = \frac{u_h V\_o Q_o}{\sqrt[m]{1+\left(\frac{u_h\left|V_{gs}-V_{gd}\right|}{L\bar{v}_{sat}}\right)^m}} \frac{W}{L} f\left(\bar{V}_{gs}, 0\right) + \frac{u_e V\_o Q_o}{\sqrt[m]{1+\left(\frac{u_e\left|V_{gs}-V_{gd}\right|}{L\bar{v}_{sat}}\right)^m}} \frac{W}{L} f\left(0, \bar{V}_{gd}\right) \tag{3.16}$$

$$I_{ds_4} = \frac{u_h V\_o Q_o}{\sqrt[m]{1+\left(\frac{u_h\left|V_{gs}-V_{gd}\right|}{L\bar{v}_{sat}}\right)^m}} \frac{W}{L} f\left(\bar{V}_{gs}, \bar{V}_{gd}\right) \tag{3.17}$$

$$f\left(x, y\right) = x\sqrt{1+x^2} - y\sqrt{1+y^2} + \ln\left(\frac{\sqrt{1+x^2}+x}{\sqrt{1+y^2}+y}\right) \tag{3.18}$$

$$\bar{v}_{sat} = \frac{v_F \beta}{\sqrt[4]{n_o^2 + \left(\frac{C\left(V_{gs}+V_{gd}\right)}{2q}\right)}} \tag{3.19}$$

$$\bar{V}_{gs} = V_{gs}/V\_o \qquad \bar{V}_{gd} = V_{gd}/V\_o \qquad V\_o = Q_o/C \qquad C = \frac{C_{gd}+C_{gs}}{WL} \qquad Q_o = qn_o$$

where μ_e and μ_h are electron and hole mobility, n_o is the residual carrier density due to disorder and thermal excitation, C is the gate capacitance per area, W and L are the channel width and length, q is the electron charge, β which relates to the phonon wavelength of the dominant scattering phonon ($\beta = 4 \times 10^{11} cm^{-1}$ for graphene on SiO_2 [37]), and m is a fitting parameter. Merging the above equations in a single equation is easily done using a combination of step functions where the variables are V_{gs} and V_{gd}, but continuity is required, so it is helpful to use the $\Theta\left(x\right)$ function. In this regard, the single I_{ds} and $\Theta\left(x\right)$ equations are:

$$\begin{aligned} I_{ds} = I_{ds_1}\Theta\left(V_{gs}\right)\Theta\left(V_{gd}\right) + I_{ds_2}\Theta\left(V_{gs}\right)\Theta\left(-V_{gd}\right) + \\ + I_{ds_3}\Theta\left(-V_{gs}\right)\Theta\left(V_{gd}\right) + I_{ds_4}\Theta\left(-V_{gs}\right)\Theta\left(-V_{gd}\right) \end{aligned} \tag{3.20}$$

$$\Theta\left(x\right) = \frac{1+\tanh\left(V_1 x\right)}{2} \tag{3.21}$$

where V_1 is a fitting parameter. To include the unintentional charging in the channel at low V_{ds}, the V_o variable is introduced ($V_{gs} = V_{gs} - V_o$ and $V_{ds} = V_{ds} - V_o$). This V_o corresponds to the Dirac voltage at low V_{ds}.

As it was referred to, there is a difference in contact resistance depending on the carrier type present in the channel, and to model this, the authors added a carrier-dependent series resistance to the contact resistance. Another approximation is that both source and drain contact resistance are equal since it scales with channel width rather than the contact area [75]. Finally, the contact resistances have the following equation:

$$R_S = R_D = R_o + R_{ext}\left(V_{gs}, V_{gd}\right) \qquad R_{ext}\left(x,y\right) = R_{ext_o}\frac{1+\tanh\left(V_2 x\right)}{2}\frac{1+\tanh\left(V_2 y\right)}{2}$$

where R_o is the resistance when $V_{gs} < 0$ and $V_{gd} < 0$, R_{ext_o} is the resistance added to account for the difference in the resistance due to different majority carriers, and V_2 is a fitting parameter.

3.3.1 Parameters extraction

The extrinsic parameters can be extracted as described in 3.1.2, excluding R_S and R_D, since their purpose is to capture the difference in contact resistance depending on the carrier type. In this regard, both parameters are extracted from the DC measurements of the $I_{DS} - V_{GS}$ curves at low drain voltages. This is a requirement since, at low drain voltage, Equation 3.14 and Equation 3.17 and the intrinsic and extrinsic drain-source resistance can be reduced to:

Table 3: Device resistance analysis.

	Holes	**Electron**
Intrinsic: $R_{ds} = V_{ds}/I_{ds}$	$\frac{1}{\alpha_h}\sqrt{1+\left(V_{GS}/V\_o\right)^2}$	$\frac{1}{\alpha_e}\sqrt{1+\left(V_{GS}/V\_o\right)^2}$
Extrinsic: $R_{DS} = \frac{V_{DS}}{I_{DS}} = R_S + R_D + R_{ds}$	$2R_o + \frac{\alpha_h}{\sqrt{1+\left(V_{GS}/V\_o\right)^2}}$	$2R_o + 2R_{ext_o}\frac{\alpha_h}{\sqrt{1+\left(V_{GS}/V\_o\right)^2}}$
$\alpha_{e,h} = \frac{L}{W\mu_{e,h}Q_o}$		

By fitting the R_{DS} profile with the above equations, it is possible to extract the values of R_S, R_D, Vo and $\alpha_{h,e}$. When biased at the Dirac point, the intrinsic capacities can be extracted by measuring the device S-params. This operation point is mandatory since, at this point, the device is not operating as an active device, and a resistance can substitute the I_{ds} current source. In this way, after de-embedding the measurements as described in 3.1.2, the following parameters can be extracted:

$$C_{gd} = \frac{\text{Imag}\left[-Y_{12}\right]}{w} \qquad C_{gs} = \frac{\text{Imag}\left[Y_{11} + Y_{12}\right]}{w} \qquad C_{ds} = \frac{\text{Imag}\left[Y_{22} + Y_{12}\right]}{w} \tag{3.22}$$

Finally, the remaining parameters are simply calculated as follows:

$$C = \frac{C_{gs} + C_{gd}}{WL} \qquad Q_o = CV\_o \qquad u_{e,h} = \frac{L}{W\alpha_{e,h}Q_o} \tag{3.23}$$

3.4 Empirical Model

Similar to the previous model, the model presented in [53] uses a similar large signal model, but three resistances are added to the model, the gate-to-drain resistance, R_{gd}, the gate-to-source resistance, R_{gs} and drain-to-source resistance, R_{ds}. Different from the previous models, I_{ds} is modelled using a fixed g_m from measurements $\left(I_{ds} = g_m \times V_{gs}\right)$. This means that the model can only be used to simulate a narrow range of operations. In the referred paper, it was intended to simulate the S-params and then extract the FOMs of the GFET.

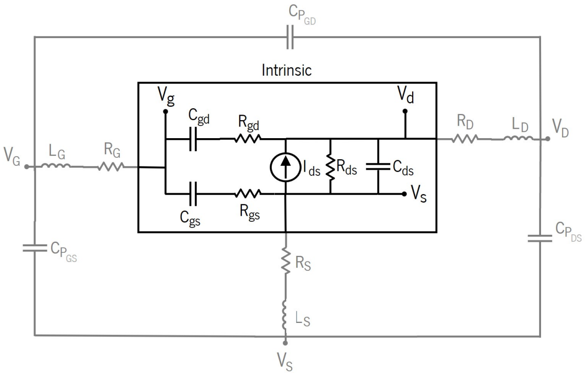


Figure 19: Large-signal model equivalent circuit.

Because this is an EM, all parameters can be extracted from the measurement of the S-params and DC analysis. As it was referred in 3.1.1, obtaining the g_m profile from the DC measurements is possible.

The other parameters can be obtained from the intrinsic Y-params using the following expressions:

$$D = 1 + w^2 C_{gd}^2 R_{gd}^2 \tag{3.24}$$

$$C_{gd} = -\frac{\text{Imag}\left[Y_{12}\right]}{w}\left[1 + \left(\frac{\text{Real}\left[Y_{12}\right]}{\text{Imag}\left[Y_{12}\right]}\right)^2\right] \tag{3.25}$$

$$R_{gd} = \frac{\text{Real}\left[Y_{12}\right]}{\text{Imag}\left[Y_{12}\right]} \cdot \frac{1}{wC_{gd}} \tag{3.26}$$

$$R_{gs} = \frac{\text{Real}\left[Y_{11}\right] - \frac{w^2 C_{gd}^2 R_{gd}}{D}}{\text{Imag}\left[Y_{11}\right] - (wC_{gd})/D} \cdot \frac{1}{wC_{gd}} \tag{3.27}$$

$$C_{ds} = \frac{\text{Imag}\left[Y_{22}\right]}{w} - \frac{C_{gd}}{D} \tag{3.28}$$

$$C_{gs} = \frac{1}{w} \cdot \left[\text{Real}\left[Y_{11}\right] - \frac{w^2 C_{gd}^2 R_{gd}}{D}\right] \cdot \left[\frac{\text{Imag}\left[Y_{11}\right] - \frac{wC_{gd}}{D}}{\text{Real}\left[Y_{11}\right] - \frac{w^2 C_{gd}^2 R_{gd}}{D}} + \frac{\text{Real}\left[Y_{11}\right] - \frac{w^2 C_{gd}^2 R_{gd}}{D}}{\text{Imag}\left[Y_{11}\right] - \frac{wC_{gd}}{D}}\right] \tag{3.29}$$

3.5 Parameter extraction tool

This section presents a GUI based on the SEM since as it will be shown in the next chapter it was the best model. This GUI can be used to acquire the model parameters from measured data. These parameters can be used to do simulations using the Verilog-A model or just to use them to compare with other fabricated devices.

This GUI was developed in Python using the PySimpleGUI, and to process the RF data it was used the scikit-rf library. This chapter is not code-descriptive but representative of the application's features.

The main window displays the equivalent circuit of the model and has two buttons to choose the mode, *DC* or *RF*, and an *About* button with some information about the model and the GUI.

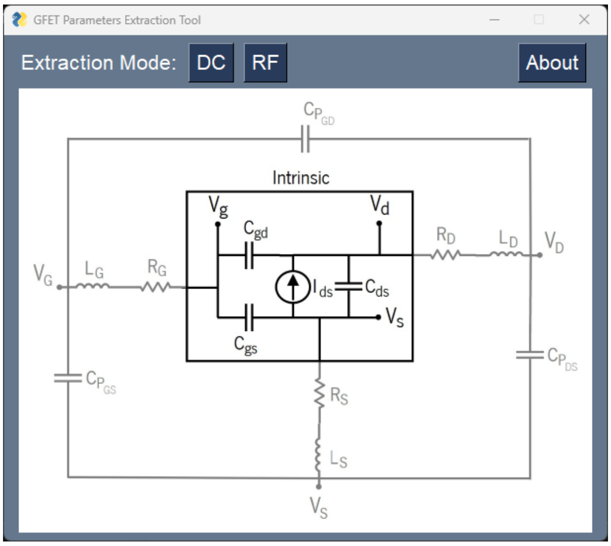
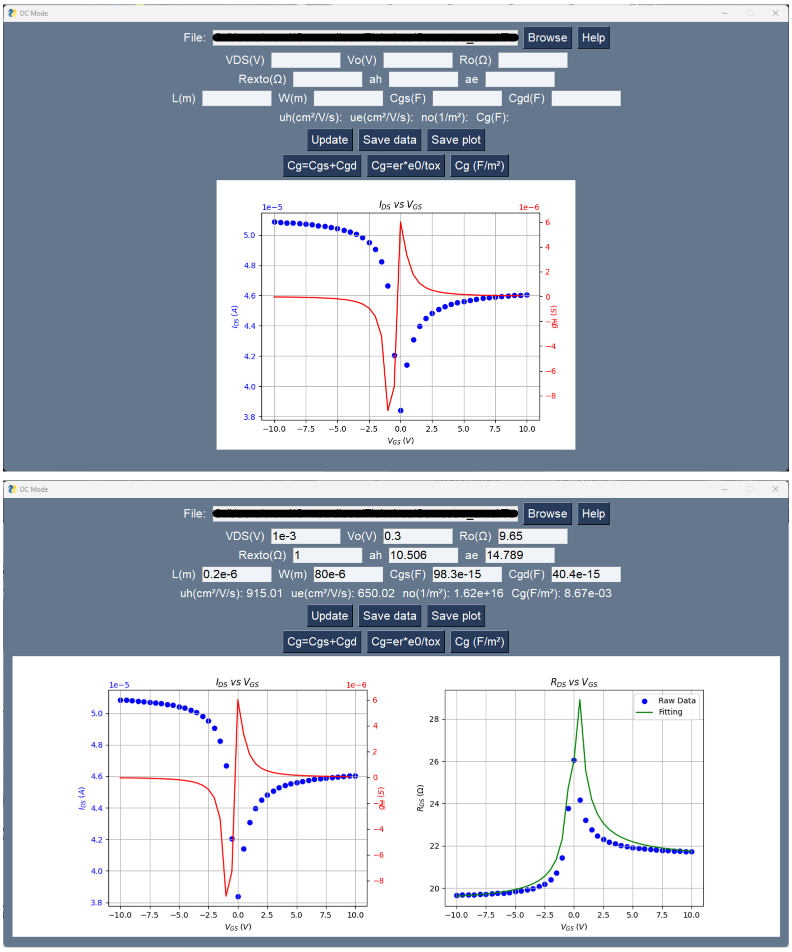


Figure 20: GUI main window.

A second window appears when the *DC* button is pressed. The DC data file must be loaded in this window using the *Browse* button. After selecting the file, a plot of the $I_{DS} - V_{GS}$ and $g_m - V_{GS}$ is displayed. To do the parameters extraction, the user must guess the parameters he does not know and then press the Update button. When pressed, a second plot of the $R_{DS} - V_{GS}$ profile appears, and the user must fit the green line into the blue dots. This is done by changing the parameters and then pressing the Update button again. Once the fitting is as close as it can get, the user can save the plot by pressing the *Save plot* button and save all the data in a .txt file by pressing the *Save data* button. Three other buttons allow for switching the gate capacitance per area approach. The three available methods use the geometric gate capacitance $\left(C_g = \frac{\epsilon_r \epsilon_0}{t_o x}\right)$, or the C_{gs} and C_{gd} capacitances $\left(C_g = \frac{C_{gs}+C_{gd}}{WL}\right)$, or introducing the value of the gate capacitance per area.



File: [redacted]

VDS(V) 1e-3 Vo(V) 0.3 Ro(Ω) 9.65

Rexto(Ω) 1 ah 10.506 ae 14.789

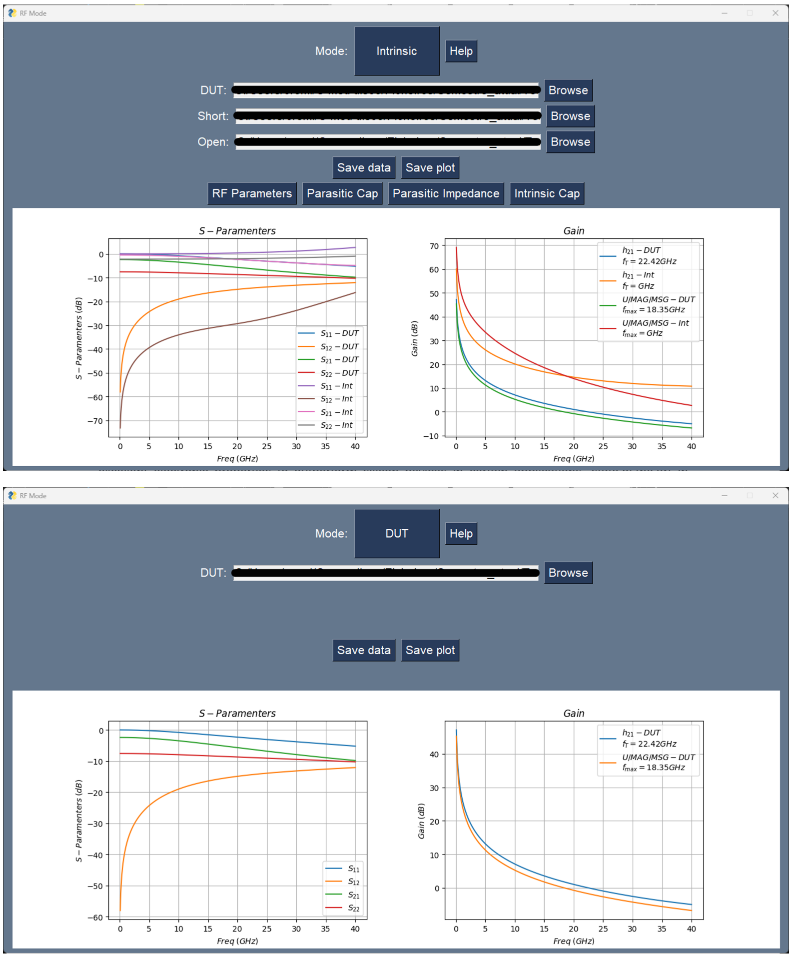
L(m) 0.2e-6 W(m) 80e-6 Cgs(F) 98.3e-15 Cgd(F) 40.4e-15

uh(cm²/V/s): 915.01 ue(cm²/V/s): 650.02 no(1/m²): 1.62e+16 Cg(F/m²): 8.67e-03

Figure 21: GUI after selecting the DC file (top) and GUI after pressing the Update button (bottom).

A second window appears when the *RF* button is pressed. In this new window, the de-embedding method discussed in 3.1.2 is implemented. The DUT, Short and Open files must be added by pressing each individual *Browse* button, and immediately a plot of both intrinsic and extrinsic S-params, H_{21} parameter and $U/MSG/MAG$ appears. This plot implements a simple method to get both intrinsic and extrinsic f_T and f_{max}. This is done by checking if the first value of the gain is positive and the last negative.

If that condition is satisfied, the FOMs are assumed to be at the smallest value of the modulus of the gain, which is the closest point to $0\ dB$. Since some measurements may have noise, the user must be critical of the extracted FOMs. In this window, by pressing the lowest buttons, different plots show the parameters extracted using the described method to de-embed. In this mode, it is also possible to save the data by pressing the *Save data* button and save the presented plot by pressing the *Save plot* button. The large *Intrinsic* button can be pressed to switch to a DUT-only analysis, where there is no need for the de-embedding files, and only the DUT FOMs are evaluated.



Mode: Intrinsic

DUT: [redacted]

Short: [redacted]

Open: [redacted]

Mode: DUT

DUT: [redacted]

Figure 22: RF mode after adding files (top) and DUT mode (bottom).

This GUI allows quick and easy parameter extraction and evaluation of the f_T and f_{max} in both intrinsic and extrinsic domains. Furthermore, the GUI was evaluated against simulated data allowing for the extraction of the parameters used in the simulations in both DC and RF modes.

4

Device and circuit simulation

In this chapter, the three models will be evaluated in five different circuit simulations. The first is DC analysis, where both V_{GS} and Extrinsic drain-source voltage (V_{DS}) sweeps will be performed. The second is the RF analysis, where S-params will be simulated, and then the FOMs extracted. The third is the first device and corresponds to an inverter. The fourth is a ring oscillator and the last is a frequency doubler.

In all the simulations presented in this chapter, the following parameters from [53] are used. Since not all parameters are available in the paper, their values were chosen to best fit the data presented.

Table 4: Parameters used on simulation. First tree lines from [53] and the remaining chosen to the best fitting.

W(μm)	L(μm)	$t_{ox}(nm)$	$u_h(cm^2V^{-1}s^{-1})$	$u_e(cm^2V^{-1}s^{-1})$	$C_{gs}(fF)$
80	0.2	5	915	650	98.3
$C_{gd}(fF)$	$C_{ds}(fF)$	$R_{gs}(\Omega)$	$R_{gd}(\Omega)$	$R_{ds}(\Omega)$	$R_G(\Omega)$
40.4	2.1	3.5	304	14.6	9.5
$R_D(\Omega)$	$R_S(\Omega)$	$L_G(pH)$	$L_D(pH)$	$L_S(pH)$	$V_o(V)$
9.3	10.2	82.8	27.3	21.3	-0.25
$\|g_m\|(mS)$	$R_o(\Omega)$	$R_{exto}(\Omega)$	V_o	m	V_1
21	$\frac{R_D+R_S}{2}$	1	0.3	1	2
V_2	$C_{P_{GS}}$	$C_{P_{GD}}$	$C_{P_{DS}}$	E_c	B
3	20	4	18	4.5e5	1

4.1 Models Implementation

The chosen method to implement the models begins by gathering model equations. After that, a Verilog-A file using the collected information is written and then saved to the EDA library directory. The last step is to create a component symbol on the EDA.

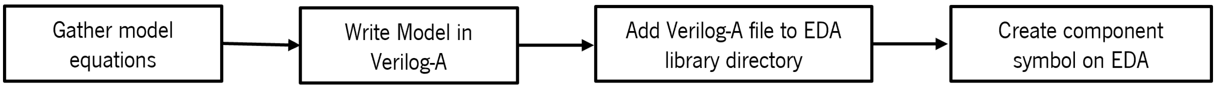
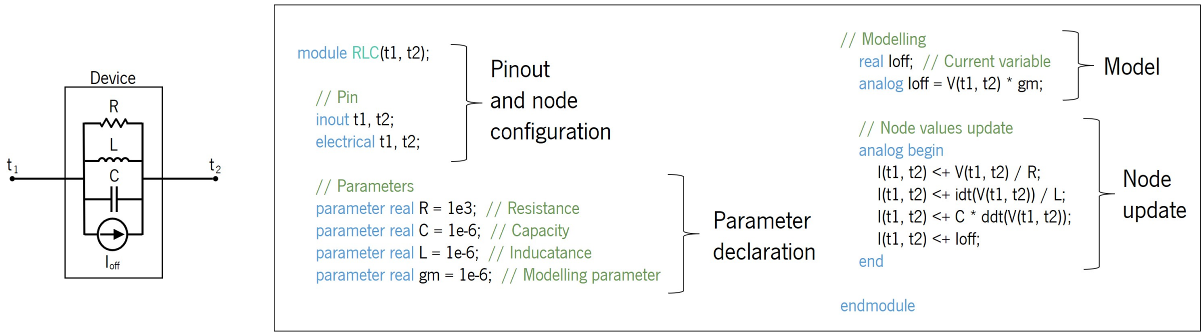


Figure 23: Diagram of model implementation in EDA.

The Verilog-A language is a programming language used for analogue circuit modelling that is based on electrical node analysis. This language was chosen since many EDA tools support it. Like all programming languages, Verilog-A also has some rules. The most important are:

- The name of the device in the Verilog-A file must be the same as in the EDA;
- The inputs/outputs of the device in the Verilog-A file must match the ones in the EDA;
- All variables must be initialized;
- The sum of all currents going in or out of a node must be zero;
- All math and logical operations must be inside the *analogue* environment;

In the Verilog-A file, the device's model can be divided into four major parts: pinout and node configuration, parameters declaration, model equations and electrical node values update. For better understanding, a simple RLC parallel circuit in parallel with a current source is used, Figure 24. The first part defines the device name and pin names that will later be used to link with the EDA. After that, follows the parameters, which are just variables that can be changed inside the EDA. The third part uses the model equation to evaluate the device values. The last one consists of doing node analysis using the known expressions for the current or voltage of a resistance, inductor and capacitor and adding the modelled current source. The same code structure was used to implement all models.



```
module RLC(t1, t2);

   // Pin
   inout t1, t2;
   electrical t1, t2;

   // Parameters
   parameter real R = 1e3;  // Resistance
   parameter real C = 1e-6;  // Capacity
   parameter real L = 1e-6;  // Inducatance
   parameter real gm = 1e-6;  // Modelling parameter

// Modelling
   real Ioff;  // Current variable
   analog Ioff = V(t1, t2) * gm;

   // Node values update
   analog begin
      I(t1, t2) <+ V(t1, t2) / R;
      I(t1, t2) <+ idt(V(t1, t2)) / L;
      I(t1, t2) <+ C * ddt(V(t1, t2));
      I(t1, t2) <+ Ioff;
   end

endmodule
```

Figure 24: RLC parallel in parallel with a current source circuit, I_{off}, (left) and Verilog-A code of the circuit (right).

4.2 Device simulation

4.2.1 DC analysis

The DC analysis was performed by sweeping the V_{GS} from $-2\ V$ to $2\ V$ for three different V_{DS}, to study the effect of the V_{DS} on the transistor characteristic curve. Since the EM uses a fixed value for g_m, it can only simulate the DC behaviour of the transistor in a single operating point. Therefore, the current source (I_{ds}) from the SEM is used to simulate the DC behaviour of the EM to understand the differences between the EM and SEM. As shown in Figure 25, there is a massive difference between the AM and the remaining. This is due to the model capturing the ideal behaviour of the GFET, which is very different from the empirical behaviour of the device. It can also be seen that the AM does not work for big V_{DS}. This happens due to the lack of continuity between the model regions when changing from the hole to electron conduction. Despite that, the model can easily be used outside the EDA to get a comparable value for the I_{DS} away from the Dirac voltage for low V_{DS} applications. By comparing the SEM against the EM, it can be seen that the difference in the conduction by holes and electrons is due to the dependence of the contact resistance with the type of carrier in the channel. It can also be seen that by increasing the value of the V_{DS} the V_{Dirac} also increases.

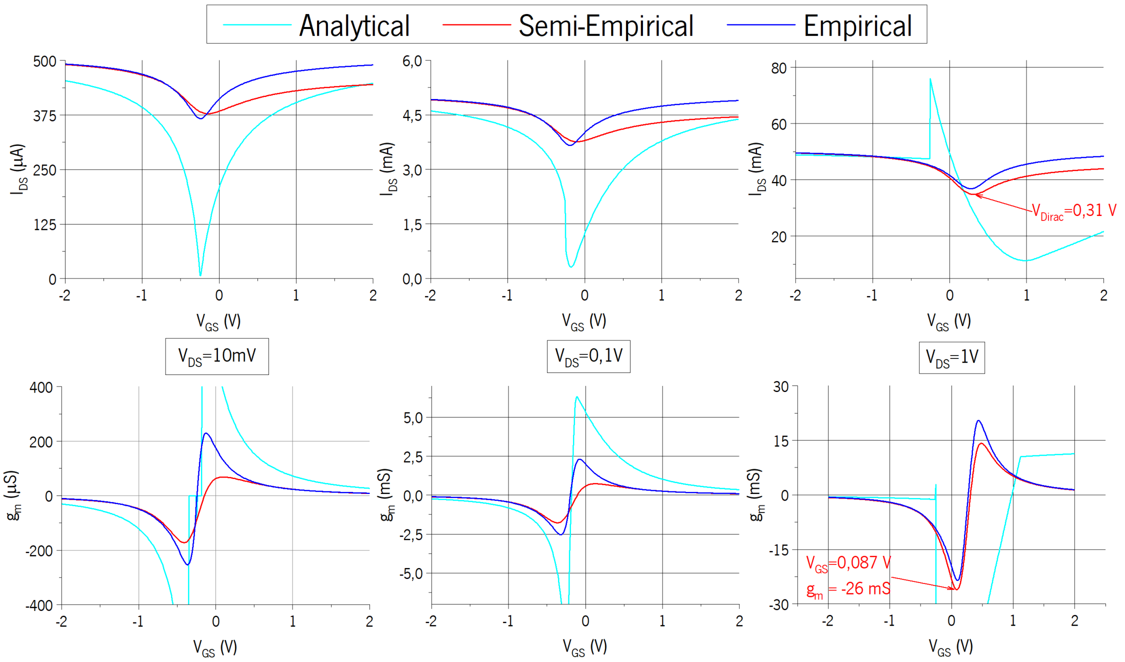


Figure 25: I_{DS} vs V_{GS} and g_m vs V_{GS} for $V_{DS} = 10\ mV$ (left), $0.1\ V$ (centre) and $1\ V$ (left) for the three models.

By using the SEM and adjusting the value of the R_{ext_o} parameter, the model very closely predicts the measured data from the paper, Figure 26. One thing to consider is that since the model has a smother I_{DS} curve, the g_m profile shows greater values when compared to the measurements.

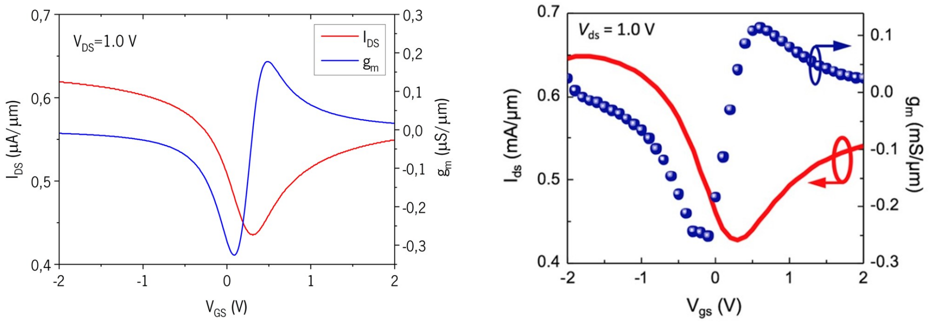


Figure 26: I_{DS} vs V_{GS} and g_m vs V_{GS} plots normalised over channel width ($80\mu m$) simulated using the semi-empirical data (left) and measurements from [53] (right).

Another critical DC analysis is the $I_{DS} - V_{DS}$ characteristic. As expected, the SEM and EM are similar, and the AM differs from them. In these plots, the operation regions proposed in the AM can be seen, but when operated at the Dirac point ($V_{GS} = -0.25\ V$) the model does not behave well for negative V_{DS}. So, one more time, the SEM shows the best simulation.

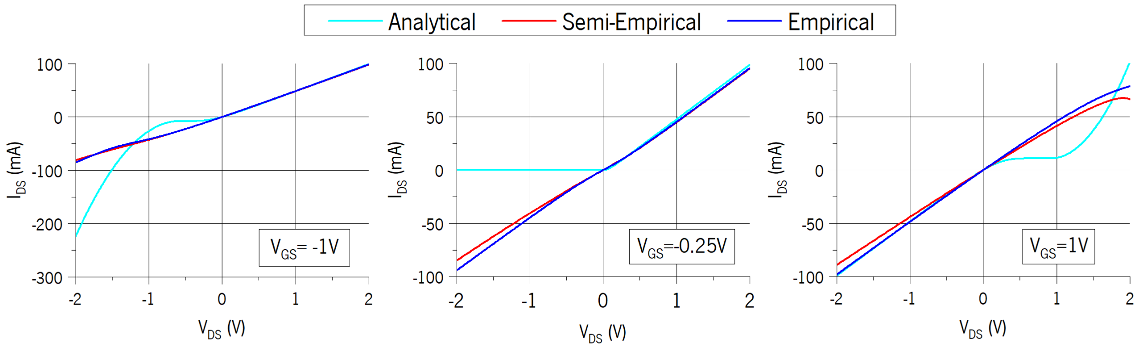


Figure 27: I_{DS} vs V_{DS} for $V_{GS} = -1\ V$ (left), $V_{GS} = -0.25\ V$ (centre) and $V_{GS} = 1\ V$ (right).

4.2.2 RF analysis

The RF analysis allows for the extraction of the model parameters and the evaluation of the f_T and f_{max}. This analysis also allows for de-embedding the intrinsic device when measuring data, but since this is a simulation, the de-embedding can be performed in two ways. It may be easy to think that removing the extrinsic elements directly from the simulated device would be preferred (changing the *mode* variable of the device to 1). However, both the gate-source and drain-source voltage would need to be adjusted to get the device in the same operation state, which would require re-simulating the $I_{DS} - V_{GS}$ and $g_m - V_{GS}$ profiles and then extracting the relevant voltages. Another way to do it is by simulating the Open and Short structures and performing the de-embedding technique. The last one is the approach used in this analysis, Appendix A. This allows for the evaluation of both extrinsic and intrinsic frequencies. In the case of the AM, it cannot predict the RF behaviour of the device since its implementation, in reality, is only a current source, it has no other components in the circuit design. As far as the SEM and EM, both can predict RF behaviour. The only difference is that in the case of the EM, the g_m must be introduced manually as a fixed value. If the RF power is increased, the fixed g_m will not allow for a reliable simulation. But for this analysis, a low-power RF signal ($0\ dBm$) is used for the S-params simulation.

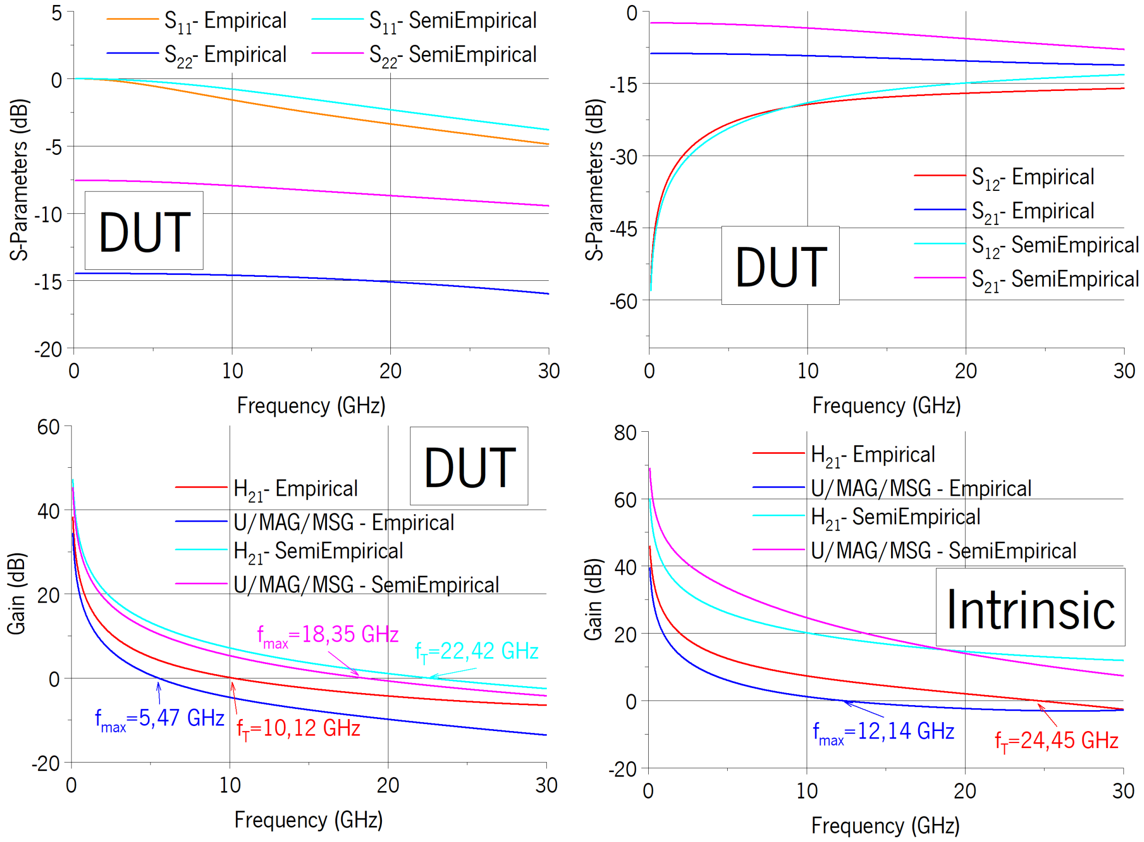


Figure 28: S-parameters simulated for both Empirical and Semi-Empirical model (2 top graphs) and f_T and f_{max} determination for both models for the DUT (bottom left) and intrinsic device (bottom right).

The first simulation is performed at the largest g_m. This point is relevant since f_T and f_{max} show greater values at this operation point. In the case of the EM, the g_m is maximum at $V_{GS} = -0.1\ V$ and has a value of $21\ mS$. As for the SEM, the maximum g_m has a value of $26\ mS$ at $V_{GS} = 0.085\ V$, Figure 25. Since the maximum g_m occurs at slightly different V_{GS}, different V_{GS} is used to simulate the S-params in each model, to achieve the maximum performance. This approach allows for the extraction of both maximum f_T and f_{max} and verifies the influence of g_m in these FOMs. The same $V_{DS} = 1\ V$ is applied to match the paper's data. The de-embedding process was implemented by simulating Open and Short circuits, as in Figure 15, to obtain the intrinsic FOMs of the simulated device. The simulations for both models are grouped in Figure 28. As can be seen, the bigger g_m allows for an overall best performance, be it the smaller attenuations on the S-params or the greater f_T and f_{max} for both DUT and intrinsic devices. For the DUT device of the EM, the FOMs simulated have similar values to the ones in the paper ($f_T = 5.6\ GHz$ and $f_{max} = 10.1\ GHz$), but when looking at the intrinsic ones, the values are much larger than the real ones ($f_T = 6.8\ GHz$ and $f_{max} = 15.8\ GHz$).

This happens because, in simulation, everything is perfect. The simulated Open and Short circuits allow for the complete removal of the extrinsic elements. As for the actual measurements, since the structures are an approximation to a model, some elements may not be removed when de-embedding, leading to smaller values of the FOMs when compared to the simulation.

The other simulation was to verify the superposition of S_{12} and S_{21} at the Dirac point. The superposition of these parameters happens when the device becomes a passive device, which occurs when g_m becomes zero. With the EM does not make sense to do this simulation since it is easy to assume that when $g_m = 0$, the current source does not produce any current, so the circuit becomes passive. But it is rather interesting to do it on the SEM since the current source is not defined as $g_m \times V_{GS}$. So, for this simulation, the V_{DS} was also $1\ V$, and V_{GS} was set to the Dirac point, with a value of $0.310\ V$, Figure 25. As was expected, at the Dirac point, S_{12} and S_{21} are at superposition, and the device can be assumed as passive in this operation point. This simulation also confirms the assumption that using an RF analysis makes it possible to find the Dirac voltage.

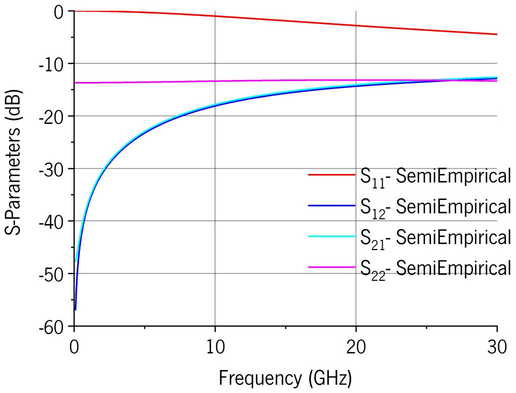


Figure 29: S-Parameters simulated with the Semi-Empirical model at the Dirac point.

4.2.3 Discussion

In the DC analysis, it was possible to see that the AM does not work for large V_{DS} values and does not show a realistic behaviour of the device. Therefore, it is not appropriate for the type of simulation desired for this study. Since the EM can only simulate a single operation point, it is unsuitable for DC analysis. Although the EM using the equations of the SEM had similar behaviour with real data, it cannot capture the difference in hole and electron contact resistance. The SEM fitted the best since it was close to the plot from the paper and even captured the different contact resistance.

In the RF analysis, only the SEM and EM were used. This analysis shows that the EM is much closer to the real FOMs than the SEM. This happens due to the maximum g_m difference. In the SEM, since the device transfer curve is simulated, the g_m is not the same as the actual device, showing slightly higher values, resulting in higher FOMs. One thing affecting the FOMs is that the parasitic capacitances are unknown, so the ones assumed may not be in close range with the real ones. Another conclusion is that when it comes to simulation, it is entirely possible to remove the full effect of extrinsic components when de-embedding, which yields much higher intrinsic frequencies. As for real de-embedding, the model assumes a set of known elements arranged in a specific configuration that may not entirely reproduce the complete actual device. It was also possible to see that at the Dirac point, the device has no gain and therefore becomes a passive device, which in terms of S-params, means that $S_{12} = S_{21}$.

From this device analysis, the model selected for circuit simulation is the SEM one. This choice comes from the excellent agreement with both DC and RF simulations from this model, whereas the other two cannot predict in both desired domains.

4.3 Circuit simulation

In this section, three circuits were simulated to verify if the SEM allows testing the GFET in different implementations. The first circuit is a digital inverter. This circuit is relevant since it is a fundamental building block of digital electronics and can be found in ring oscillators, multiplexers, and decoders. The second circuit is a ring oscillator. A ring oscillator outputs a signal with a defined frequency. This signal can be used as a clock signal of digital circuits. The last circuit is a frequency doubler. As the name implies, a frequency doubler outputs a signal with double the input signal frequency. This can also be used in digital electronics to increase the clock frequency.

4.3.1 Inverter

An inverter based on GFETs is achieved by adding two GFETs in series, Figure 30. This is the same configuration as CMOS inverters, where the top transistor behaves as p-type and the bottom as n-type. The principle of this kind of inverter is that when one transistor is at maximum conduction, the other must be turned off, but in the case of GFETs it must be close to the Dirac point. Due to the slightly different V_{DS}, a slight difference in the V_{Dirac} of the GFETs occurs, making it possible to implement an inverter using matching GFETs. This configuration leads to the W shape transfer curve. An inverter can be implemented when operating the device with V_{In} between the lowest points in the W shape curve.

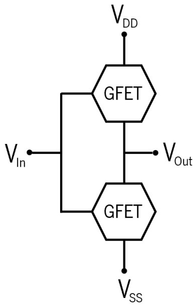


Figure 30: Inverter diagram.

In Figure 31, the W-shape transfer curve, the voltage output and the output to a square wave are presented with a V_{DD} of $1\ V$ and V_{SS} of $0\ V$ (reference voltages). As can be seen, the W-shape transfer curve is not well defined, and the output voltage is not centred and does not get close to the reference voltages. It can also be seen in the square wave simulation that although the output signal is inverted, the signal is too small when compared to the V_{In}.

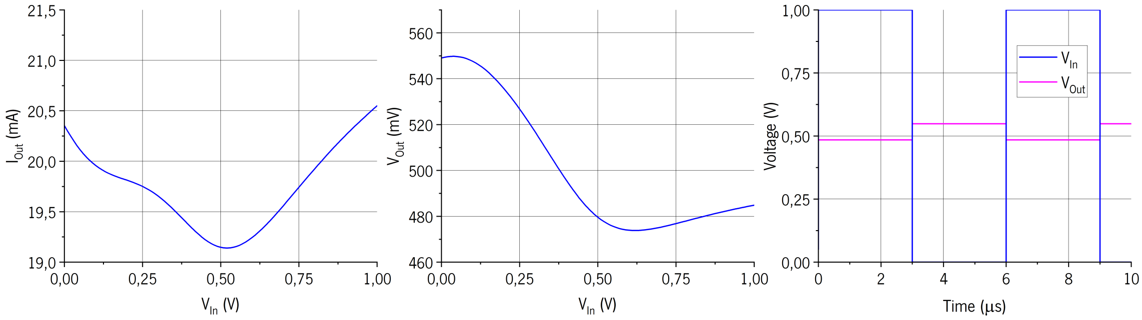


Figure 31: Inverter output current (left) and voltage (centre) for V_{In} between 0 and $1\ V$, and inverter response to a square wave (right) for $L = 0.2\mu m$.

The principle of this kind of inverter is that when one transistor is at maximum conduction, the other must be turned off, but GFETs do not turn off. One way to achieve a close behaviour is to have a low Dirac current. Since the output voltage has low amplitude, the usage of this device in cascading devices, e.g. Ring Oscillator, is not possible. To allow further simulation, the I_{DS} at Dirac voltage is reduced by increasing the channel length from $0.2\ \mu m$ to $1\ \mu m$. As shown in Figure 32, the W-shape transfer curve is better defined and the current is lower as it was intended. This well-defined W-shape produces an output voltage much closer to the reference voltages but remains not centred. When feeding a square wave to the device, the output is inverted and has a more comparable amplitude to the initial signal. Since the output voltages are closer to the reference voltages, implementing this device in cascading circuits is possible.

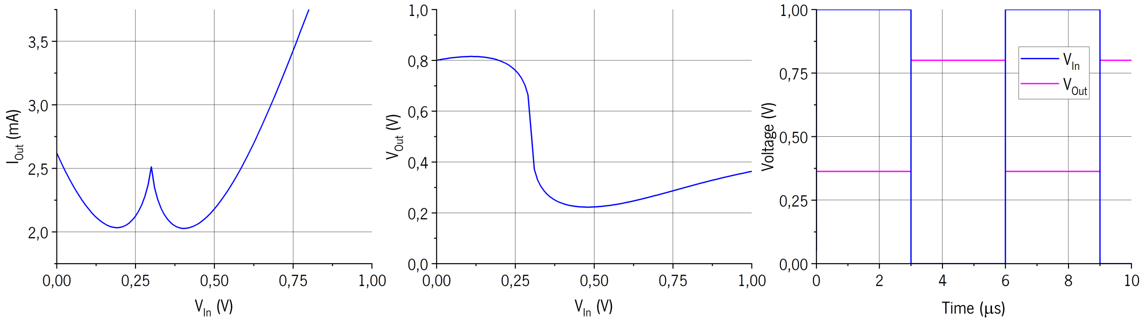


Figure 32: Inverter output current (left) and voltage (centre) for V_{In} between 0 and $1\ V$, and inverter response to a square wave (right) for $L = 1\ \mu m$.

This can be slightly improved by centring the middle point of the W-shape by unmatching the transistor V_o. This was done by replacing V_o with $V_o + 0.38$ in the upper GFET. This allows an almost symmetrical curve centred at $0.5\ V$. This also decreases the difference between the reference and output voltage. This V_o parameter is the Dirac voltage at low V_{DS}. From this analysis can be concluded that the ability to shift the Dirac voltage may be a requirement to get a well-behaved inverter. In a real device it can be changed by using a two-gate configuration, where one of the gates is responsible for the shift of the Dirac voltage.

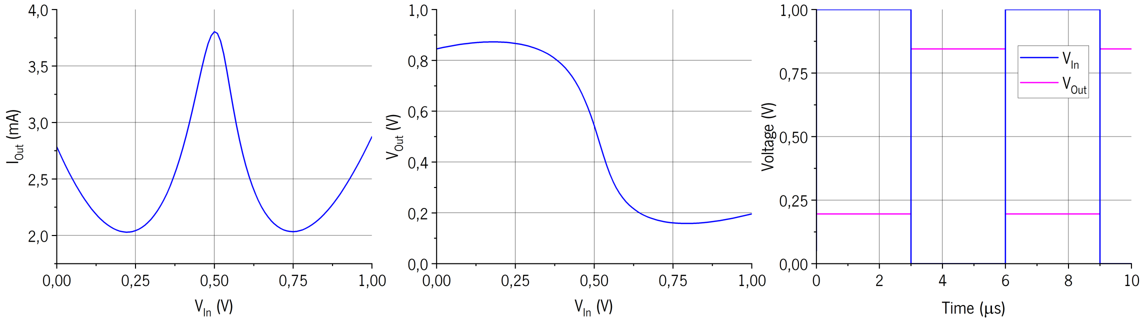


Figure 33: Inverter output current (left) and voltage (centre) for V_{In} between 0 and $1\ V$, and inverter response to a square wave (right) for $L = 1\ \mu m$. and different V_o.

4.3.2 Ring Oscillator

The ring oscillator has an odd number of cascaded logic inverters in the loop. For example, in the following simulations, a cascade made of 3 inverters is used, with a fourth inverter used to decouple the oscillator from the measurements, Figure 34.

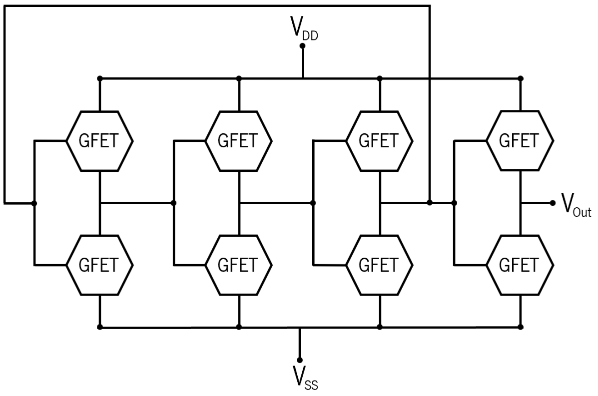


Figure 34: Ring oscillator diagram.

As for the inverter simulations, V_{DD} is set to $1\ V$ and V_{SS} is set to ground. In this kind of simulation, an initial voltage on the loop may need to be defined to make the device unstable. The inverters used were the ones simulated in the previous section. As briefly discussed in the last section, the inverter using the paper parameters cannot output a sufficient signal to feed the next stage since its output voltages are very different from the reference voltages.

As for the other two inverters, it is possible to implement the proposed ring oscillator, Figure 35. This configuration achieved a frequency of $1.14\ GHz$ for the matching V_o and $1.97\ GHz$ for the unmatching

V_o inverters. These two simulations conclude that the better the W-shape is centred to the V_{DD} and V_{SS}, the higher the frequency of the ring oscillator. The frequencies were extracted by finding the frequency of the maximum value of the spectrum of V_{Out}.

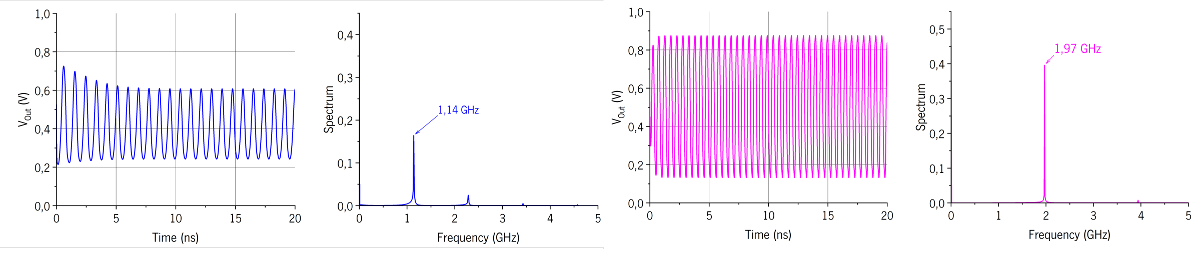


Figure 35: Ring oscillator output and frequency spectrum with $L = 1\ \mu m$, for equal V_o (blue) and different V_o (magenta).

4.3.3 Frequency doubler

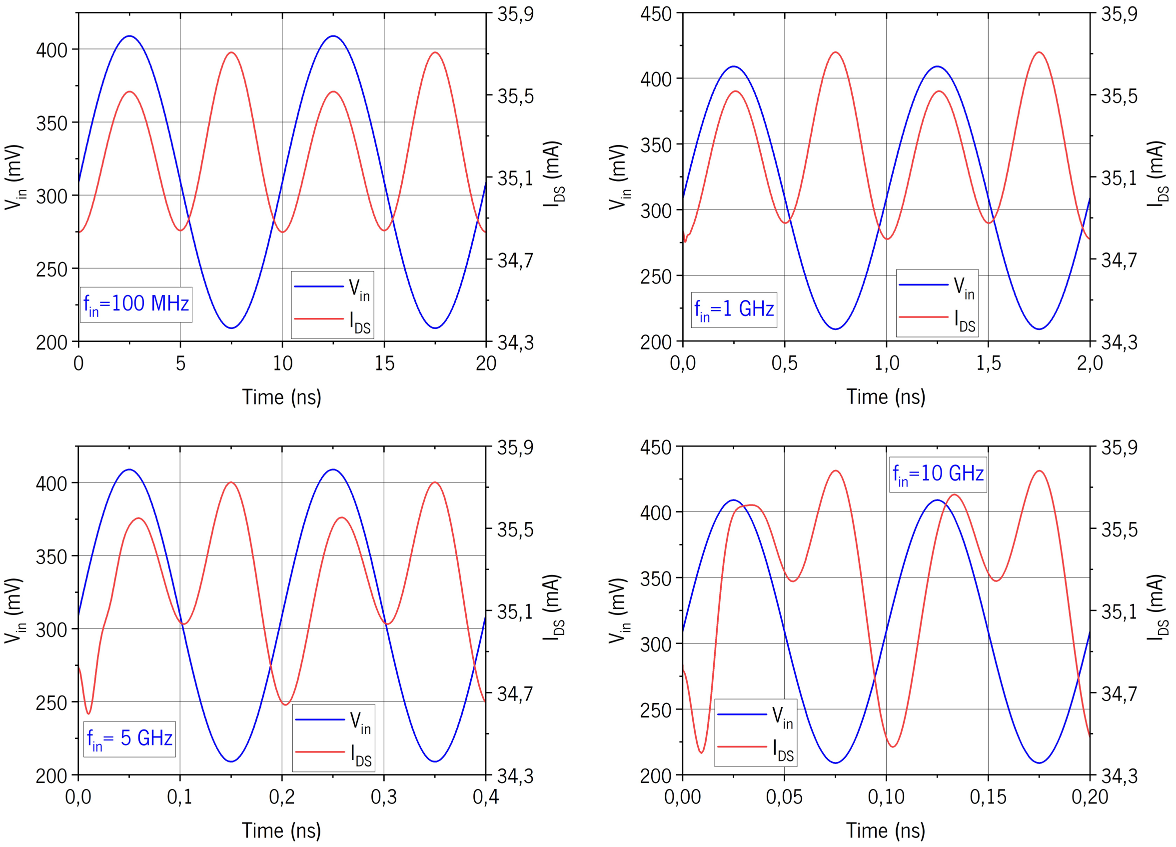


Figure 36: Simulated frequency doubler characteristic at four different input frequencies: 100 MHz (top left), 1 GHz (top right), 5 GHz (bottom left) and 10 GHz (bottom right).

A frequency doubler is a device that can produce an output with double the input frequency. In the case of the GFET as a frequency doubler, the input is at the gate, and the output is at the drain terminal. By looking at the transfer curve of the GFET, it becomes clear that when an AC signal centred on the Dirac voltage is applied to the gate, the output I_{DS} will have double the input signal frequency. It was only used the SEM since the AM would not be affected by the input frequency, which means it would be possible to use any input frequency that the output would be doubled.

Thus, the simulation for SEM was done using a sine wave V_{GS} centred on $0.31\ V$ with an amplitude of $100\ mV$ and $V_{DS} = 1\ V$, for three different frequencies, $100\ MHZ$, $1\ GHz$, $5\ GHz$ and $10\ GHz$. These frequencies were chosen to test the device far and close to the FOMs. As shown in Figure 36, the difference between the conduction of holes and electrons is present in the output of the device by the different peaks, the smallest representative of the conduction of electrons and the other the conduction of holes. Thus, it can be concluded that a key element of this device is having a hole and electron conduction almost symmetrical, as well as precisely centring the input wave on the Dirac voltage. Another aspect that can be observed is the input frequency's influence on the device's response. Since the GFET is frequency limited, as the output frequencies approach the FOMs, the output starts to be delayed to a point that does not represent the behaviour of a frequency doubler.

4.3.4 Discussion

In the inverter simulation, it was seen that the current at the Dirac point plays a vital role in this type of device. If the current is not low enough, they may invert the signal but with voltages much smaller than reference voltages, leading to the inability to use this device in more complex designs. It was also possible to conclude that unmatched Dirac voltage between the GFETs allows to centre the output voltage.

In the ring oscillator simulation, it was possible to prove that the small output signal from the inverter cannot feed the next stage and that the better the inverter output, the higher the ring oscillator frequency.

The frequency doubler was implemented by operating the device around the Dirac voltage. It was possible to see that as the frequency of the input signal increases, the device cannot double the frequency, showing that the model is frequency dependent and may allow estimating the maximum input frequency in the case of a frequency doubler. It was also possible to conclude that the difference in the conduction by holes and electrons affects the performance of the frequency doubler. Another important conclusion is that to double the frequency of the input signal, the GFET must be operated at the Dirac voltage, which means that the input signal must have a DC component equal to the Dirac voltage.

5

Conclusion

In this dissertation, methods to extract parameters from both DC and RF measurements were studied, and a GUI based on the SEM was developed to help further implementation of this model.

Simulating GFET-based circuits is crucial to understanding which devices can be done and how they will behave. In this regard, this study was conducted by doing some simulations using three different GFET models to conclude which one would best behave in various configurations. The SEM was the only model that could be used in all the presented simulations. It was also possible to compare the model against DC and RF-measured data showing very close results. The simulations were carried out beyond the measured data from the paper, and an inverter, ring oscillator and frequency doubler were implemented. These last simulations conclude that it is essential to have a simulation tool to predict different devices based on GFET since some configurations need specific characteristics to function correctly.

The gathered information in this writing makes it possible to conclude that the research on 2D materials has a long way to go. Although graphene is the most researched 2D material and shows excellent electronic properties to outperform silicon devices in specific applications, the state-of-the-art in devices' fabrication and modelling predictions have yet to be well established. Moreover, the devices' performance reported in the literature shows excellent potential to improve or substitute RF circuit designs. Still, more research on this matter needs to be conducted to assess the true potential of such devices.

5.1 Future work

Since some applications may require a back-gate to shift the Dirac point, adding a back-gate dependency to the SEM would be essential, allowing further investigation on GFETs based circuits. Another critical factor so that the model can become more general is the implementation of a noise dependency allowing for more realistic simulations. With both additions, the model would become complete and able to predict more closely real measurements and allow more complex simulations to be performed.

Another important approach to be carried out is to use the model to investigate and propose circuits based on the GFETs different from those already present in the literature.

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A

Open and Short structures simulation

The S-params of the Open and Short structures were simulated using discrete components on the EDA with the values from Table 4.

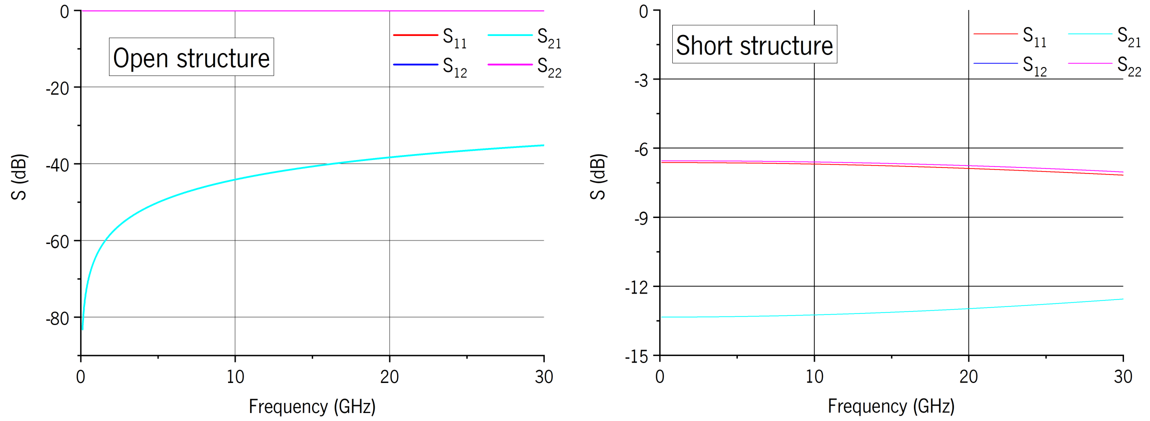

Figure 37: S-parameters simulated for both Open (left) and Short structures (right).