ON-CHIP ARRAY OF THERMOELECTRIC PELTIER MICROCOOLERS

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Abstract: This article reports on the theoretical modelling, the Finite Element Modelling (FEM) simulation, the fabrication process and preliminary results of the first on-chip thermoelectric microcooler array (64 pixels arranged in a 8×8 array), with each pixel independently controlled. This microcooler array uses co-evaporated V–VI compounds of Bi_2Te_3 and Sb_2Te_3 as thermoelectric layers, and can be fabricated using planar thin-film technology, lithography and wet etching on top of a silicon wafer, where the CMOS electronic circuits were previously made.

Keywords: Telluride Peltier microcooler array.

TRANSDUCERS & EUROSENSORS '07
The 14th International Conference on Solid-State Sensors, Actuators and Microsystems, Lyon, France, June 10-14, 2007

1. INTRODUCTION

Integration of efficient solid state thermoelectric microdevices with microelectronics is desirable for local cooling and thermoelectric microgeneration [1-3], since they can be used to stabilize the temperature of devices, decrease noise levels and increase operation speed. An array of such devices can also be used for lab-on-chip application.

Due to silicon fabrication compatibility, polycrystalline SiGe alloys and polycrystalline Si are commonly used in thermopile applications. Their use in microcoolers has been attempted [4] but the performance is very low compared with that of tellurium compounds, which have been used for many years in conventional large area Peltier devices. Thin films of n-type Bi_2Te_3 and p-type Sb_2Te_3 (Figure 6) with absolute value of Seebeck coefficient in the range 150-250 $\mu V.K^{-1}$, in-plane electrical resistivity of 7-15 $\mu\Omega.m$, carrier concentration 3×10^{19}-20×10^{19} cm^{-3} and Hall mobility 80-170 $cm^2.V^{-1}.s^{-1}$ were obtained by the authors [5]. The thermoelectric figure of merit (ZT) for these films is near unity for n-type and 0.6 for p-type. These values are comparable to the best found in literature for the bulk materials. It is demonstrated that 15ºC cooling bellow room temperature is possible to achieve using such thin-film materials in microcoolers.

2. DESIGN OF MICROCOOLER ARRAY

The array of microcooler was designed to accommodate 64 pixels (organized in 8×8 structure) of microcoolers. Each pixel can be controlled independently. Figure 1 represents a single pixel cross section. When a current flows from the n-type thermoelectric element (TE) to the metal cold pad and from this to the p-type TE, heat is absorbed in the metal - TE element junctions, by Peltier effect. The same applies to contact pads on electronics, where heating is generated by Peltier effect.

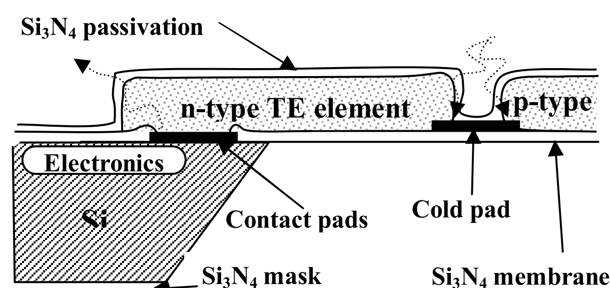

Figure 1: Drawing of a pixel of the microcooling array (not on scale).

A CMOS microchip was designed, with the electronics to address and control each pixel of the array, memorizing the state of microcooler

Figure 2 shows the circuit repeated for 9 (of the 64) pixels. Its working principle is the following: For producing the maximum cold, the voltage at the 30 kΩ resistors must be zero. In this case, the MOSFETs are not conducting and the current

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circulates from the coolers trough the 5Ω resistors to $-V_{bias}$, which must be in the order of 0.5V. The power dissipated in the 5Ω resistors is below 1mW, which is an acceptable value for the application.

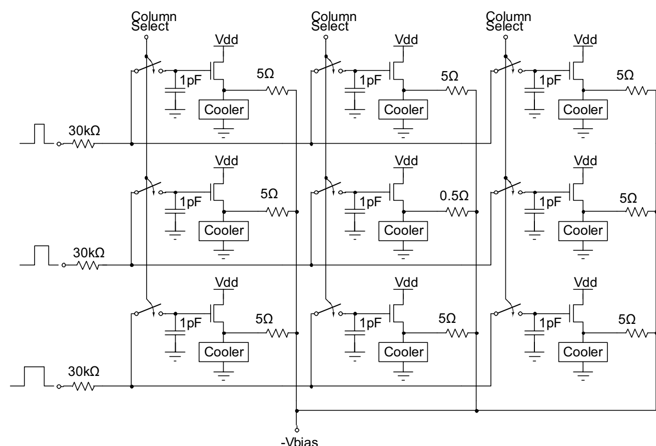

Figure 2: Electronic circuit showing 9 of the 64 pixels of the device.

When a pulse is applied to a 30kΩ resistor, the 1 pF capacitor selected by the Column selector will charge with a voltage that depends on the width of the pulse. In this case, the corresponding MOSFET will conduct, producing simultaneous phenomena: the current in the 5Ω and the current in the MOSFET will increase dissipating more power; the current in the cooler will decrease, decreasing cooling. All these will lower the efficiency of the cooler. In this way, it is possible to control each pixel independently.

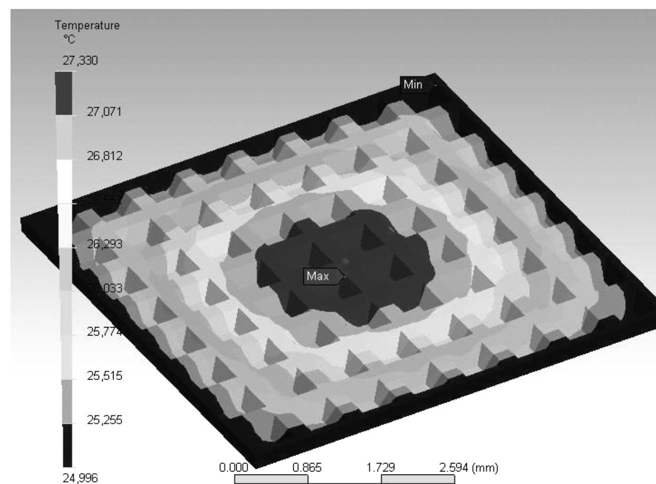

Figure 3: Backside view of the simulated structure that supports the pixels showing that maximal heating is 2.3ºC above room temperature, with all pixels turned on at full power.

Figure 3 shows the overall expected heating of the backside of the chip due to the control electronics, Peltier effect and Joule heating. A power dissipation of 1mW was considered in each 5Ω resistor and a current of 14mA is supplied to each microcooler. A 500 µm thick silicon wafer was used, and the borders of the array were bounded to a fixed temperature of 25ºC. A maximum temperature of 27.4 ºC was obtained on the silicon wafer.

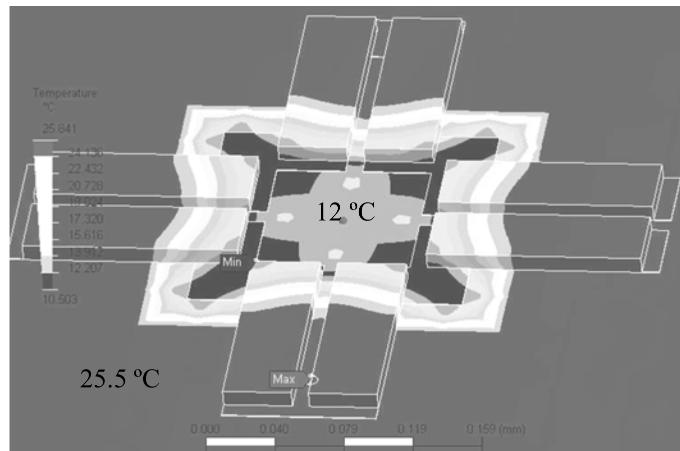

Figure 4: Single pixel microcooler simulation shows the possibility to obtain 15ºC of cooling at the centre of the pixel.

FEM simulation was also used to calculate the expected temperature drop on each pixel. A temperature drop of 15ºC, bellow room temperature was obtained (Figure 4). To obtain this cooling capacity, a membrane (200 nm thick) of silicon nitride supports 4 pairs of TE elements (40µm × 100µm × 10µm), powered with 14 mA current. Contact resistivity of 10^{-10} $\Omega.m^2$ was used on simulations. Radiation and convection was considered on the cooled surface (10 $Wm^{-2}K^{-1}$). Thermoelectric properties of n-type and p-type elements were considered as achieved on previous experimental results [5]. Results obtained from FEM simulation on a single pixel microcooler agree with theoretical calculations [8].

3. FABRICATION STEPS

The Si wafer with control electronics is covered with a Si_3N_4 layer where two vias are opened to access the metallic pads on top that will provide connection to the thermoelectric elements (Figure 1). The n-type thermoelectric material is deposited by co-evaporation [6,7] and patterned by

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photolithography on top of the wafer (Figure 5). An etchant based on nitric acid can be used to etch telluride films without etching the metal contact pads [9]. Without removing the photoresist used to pattern the n-type material, p-type material is deposited on top of the wafer. This layer is also patterned using photolithography and wet etching on nitric acid based etchant.

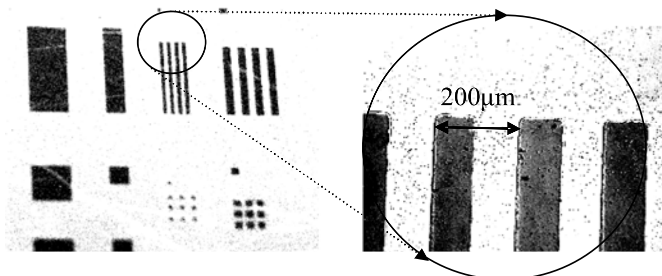

Figure 5: Micrographs of etched Bi_2Te_3 structures

Photoresists are then removed (from n-type and p–type materials) and a passivation layer of Si_3N_4 is used to avoid degradation of the thermoelectric films in contact with atmospheric oxygen. The last step of fabrication is the etching of the back side of the Si wafer using KOH, to fabricate a membrane of Si_3N_4 on each pixel, that supports the microcooler elements. This membrane achieves significant reduction of thermal conduction between the cold and the hot sides of the Peltier device. Electronic circuits in the wafer are confined to the regions between the microcoolers to prevent damage during the last KOH fabrication step. Moreover, the back side of the wafer is covered with another patterned Si_3N_4 layer which will act as a mask during the etch step to release the membrane.

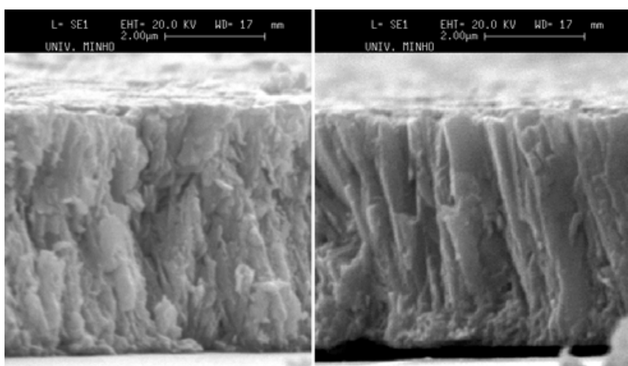

Figure 6: SEM photo of Bi_2Te_3 (left) and Sb_2Te_3 (right) thin films.

4. DISCUSSION AND RESULTS

An enlarged microcooler individual pixel was fabricated and tested on top of a polyimide substrate that emulates the Si_3N_4 membrane (Figure 7). The fabrication of these enlarged microcooler (using shadow masks during deposition of thermoelectric materials) allowed a rapid fabrication of a demonstration prototype, without all the steps required to fabricate the microcooler as previous referred. The working principle of the microcooler and the quality of materials were demonstrated and evaluated.

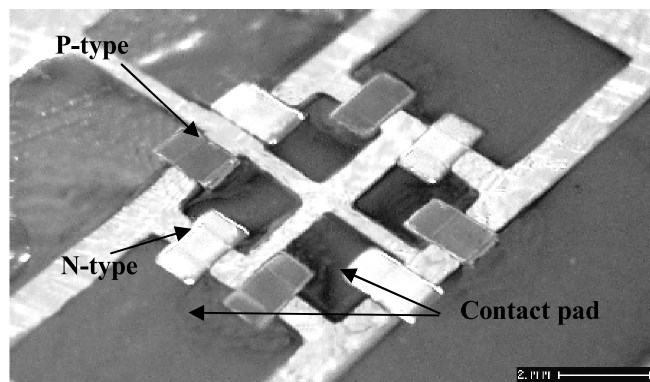

Figure 7: Photo of a microcooler pixel, on top of a polyimide substrate.

The performance of the microcooler was analyzed by use of a thermal image map generated with an infrared microscope. An image was obtained with a 4 mA current through the device and cold and hot sides are clearly identified (Figure 8).

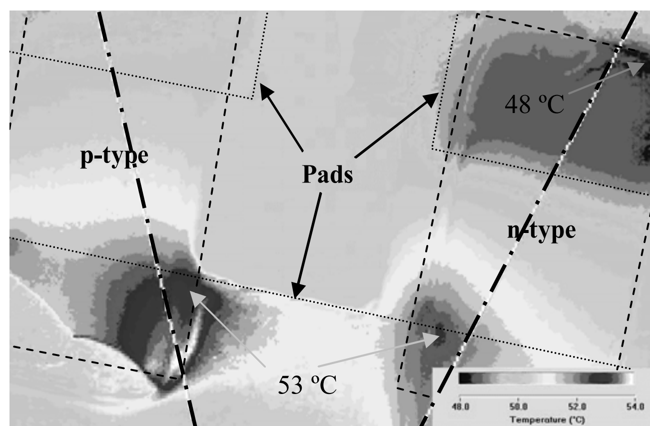

Figure 8: Thermal image of n-type and p-type thermoelectric elements presented on figure 7, powered with 4mA current, under vacuum.

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A temperature difference of 5 ºC was measured between the hot and the cold sides, under vacuum. The distance from expected results is due too high contact resistances between metal pads and thermoelectric elements. A contact resistance of 10^{-6} Ω.m^2 was measured. This value is expected to be reduced to less than 10^{-9} Ωm^2 using a layered fabrication process [2]. The high temperature achieved on the hot side of the device results from the low dissipation capability due to the low thermal conductivity of the substrate used in the prototype (polyimide) compared with the substrate used in simulation (silicon covered with silicon nitride). The low thermal conductivity in contact pads also contributes for this higher temperature on the hot side of the device.

5. CONCLUSIONS

An array of microcoolers, with 64 pixels, with each pixel controlled independently to cool or heat was designed and simulated, and the respective fabrication process was described. A temperature difference of ±15ºC could be achieved in each pixel. Thermoelectric thin-films with high figure of merit were obtained by co-evaporation, suitable for fabrication of such microcoolers, and lithographic pattern techniques were applied on these films.

A large area pixel of the microcooler was fabricated and its performance analysed under microscopic infrared imaging. A temperature difference of 5ºC was obtained. Differences from expected performance are due to high electrical resistance and low thermal conductance obtained in the pad - thermoelectric material interface. Efforts are being made to reduce contact resistance and fabricate thermoelectric elements with lower dimensions.

ACKNOWLEDGMENTS

This work was supported by ADI (MPYROM) and Portuguese Foundation for Science and Technology (SFRH/BD/18142/2004). First author also would like to thank Gao Min and D.M. Rowe for help in fabrication of thin films and F. Volklein for thermal conductivity measurements.

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