A Novel Multilevel Interleaved-Based PFC Rectifier with Modular DC Interfaces

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***Abstract*—As it has been recognized, mainly over the last decades, PFC rectifiers are more and more fundamental and are increasingly present in several applications in the perspective of limiting power quality problems. In line with this reality, this paper proposes a novel topology of single-phase PFC rectifier. On the AC-side, the proposed PFC rectifier operates with sinusoidal current in phase with the voltage, but, additionally, it presents these very important advantages: Multilevel voltage operation; Interleaved-based current control; Modular design, allowing to establish *n* DC interfaces on the DC-side. The proposed PFC rectifier is comprehensively detailed, and the validation is carried out with a configuration that allows to have two independent DC interfaces, resulting in an operation with five different voltage levels, and in a current control with a ripple with a frequency that corresponds to four times the value of the switching frequency of each switching device. The validation was carried out addressing the operation of the proposed PFC rectifier in steady-state and transient-state.**

***Keywords*—PFC Rectifier, Multilevel, Interleaved-Based, Modular DC Interfaces, Power Quality.**

I. INTRODUCTION

As broadly revealed and investigated, sustainability is a crucial topic covering different areas within electrical grids, where the convergence for smart grids is recognized as a priority [1]. Inside the extended scope of smart grids, many technologies are emerging and other are coming up again, such as the possibility of DC electrical grids [2][3]. This possibility is decisively, coming up again, due to the native DC operation of technologies as renewables from PV panels, storage based on batteries or ultra-capacitors, and electric vehicles, both contemplating on-board and off-board chargers. In such state, it is well-known that the use of power electronics converters is essential for the progress of power grids [4]. Consequently, such reality pushes the enhancement of innovative power electronics converters, where the power quality constraints and the efficiency are topics that are assuming a special preponderance. Therefore, due to the innumerous applications where power converters are used, new topologies and control algorithms are constantly emerging, as presented in [5], [6], and [7]. Among all applications of power converters, a distinct relevance is given to power factor correction (PFC) rectifiers due to power quality concerns. PFC rectifiers are mainly used as front-end converters offering an initial stage to control the current on the power grid interface, both in single-phase or three-phase systems, while back-end converters are used as a second stage to adapt the voltage levels with or without isolation [8][9][10]. More precisely in terms of principle of operation, PFC rectifiers can be based on boost or buck structures and, in more detail, e.g., such structures can be based on multilevel or interleaved topologies [11][12]. Regarding multilevel, the traditional NPC converter emerged on 1980s [13], and since such decade, numerous innovative multilevel arrangements were proposed, with prominence on flying capacitor and cascaded structures [14][15]. Multilevel converters can be used with diverse purposes, including the option to minimize the requirements of passive filters. Since the operating voltage is mainly based on the fundamental component, therefore, it is obvious that increasing the voltage levels is an interesting tactic to reduce the passive filters. Moreover, a multilevel converter permits the reduction of the maximum voltage applied to each power device. Nevertheless, expanding the voltage levels means increasing the hardware and the control complexity. In terms of utilization, multilevel converters can be applied for a vast set of applications, including motor drives [16], interface of renewables [17], power conditioners [18], and EV front-end chargers [19]. In terms of specific multilevel topologies, several arrangements are possible, including five-level NPC [20], T-type [21], three-phase NPC-based [22], Vienna-type [23], and packed U-cell [24]. Aligned with the context of multilevel converters, a novel multilevel PFC rectifier is proposed. Additionally, it operates in interleaved-based mode, also guaranteeing the multilevel feature, and permitting modular DC interfaces. On the DC-side, the proposed PFC rectifier permits the reconfiguration for *n* DC interfaces, meaning that it can be reconfigured to operate with several voltage levels and, consequently, the operation in interleaved mode also increases. These three features, DC interfaces, voltage levels, and interleaved-based operation, are related and are performed in simultaneous operation. It is important to note that PFC rectifiers with double DC interfaces are used in diverse applications. A dual output PFC with interleaved operation is proposed in [25], but considering the parallel of two back-end converters. A dual DC output PFC is presented in [26], but both DC interfaces have a common ground, i.e., they are not independent. A dual output PFC interleaved is presented in [27] and a dual output PFC rectifier is presented in [28], but in both cases the DC interfaces have a common ground. However, none of these allows the possibilities of individual DC interfaces, i.e., without a common ground. Fig. 1 shows the conceptual representation of PFC rectifiers, highlighting the traditional PFC characterized by single AC and DC interfaces and the proposed PFC with modular structure on the DC-side allowing *n* DC interfaces from a single AC interface.

As contributions of the proposed PFC rectifier, it can be highlighted: (i) PFC rectifier that operates, simultaneously, with

multilevel and interleaved-based features; (ii) PFC rectifier with modular DC-side capable to be reconfigured for operating with n DC interfaces; (iii) PFC rectifier with a reconfigurable structure to allow independent DC interfaces directly influencing the multilevel voltages and the interleaved-based operation; (v) Proven validation of the proposed PFC rectifier for the possible operation modes in steady-state and transient-state, including the simultaneous operation with DC interfaces, voltage levels, and interleaved-based operation. The details of the proposed PFC rectifier concerning its modular structure and operation is analyzed in section II, while the dedicated algorithm for controlling the AC-side current and the DC-link voltages is presented in section III. The proven validation of the claimed advantages of the proposed PFC rectifier is presented in section IV considering distinct scenarios and a detailed operation, and the conclusions are given in section V.

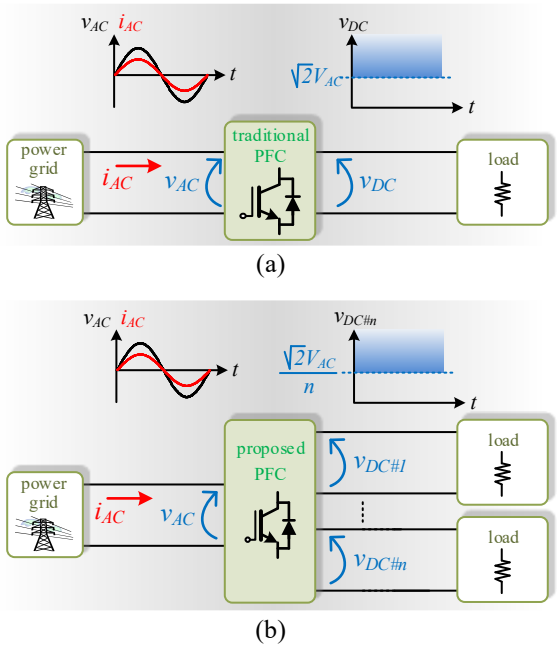

Fig. 1. Conceptual representation of PFC rectifiers considering: (a) Traditional PFC with a single DC interface; (b) Proposed PFC with a modular structure on the DC-side allowing n DC interfaces.

II. Proposed PFC Rectifier: Analysis of the Principle of Operation

Fig. 2 shows the structure of the proposed PFC rectifier. As shown, on the AC-side the interface with the power gird is performed with a diode bridge, while on the DC-side the proposed PFC rectifier is constituted by n active interfaces (each one with two switching devices and two diodes). As mentioned, the proposed PFC rectifier can have n DC interfaces, always guaranteeing the sinusoidal current and unitary power factor on the AC-side.

Each active interface permits the operation with a maximum of 3 voltage levels, therefore, since the DC interfaces are linked with a common point, the PFC rectifier permits the operation with a maximum number of voltage levels (n_{VL}) defined by:

$$n_{VL} = 2n + 1\,. \tag{1}$$

The multilevel feature is very relevant, however, as mentioned, the proposed PFC rectifier also permits an interleaved-based operation. Therefore, since each switching device of each DC interface is controlled with independent PWM carriers shifted 180 degrees, the resultant current on the inductors (i_{L1}, i_{Ln}) for n DC interfaces has a ripple whose frequency is defined by:

$$f_{\Delta iL\{1,2\}} = 2n\, f_{SW}\,. \tag{2}$$

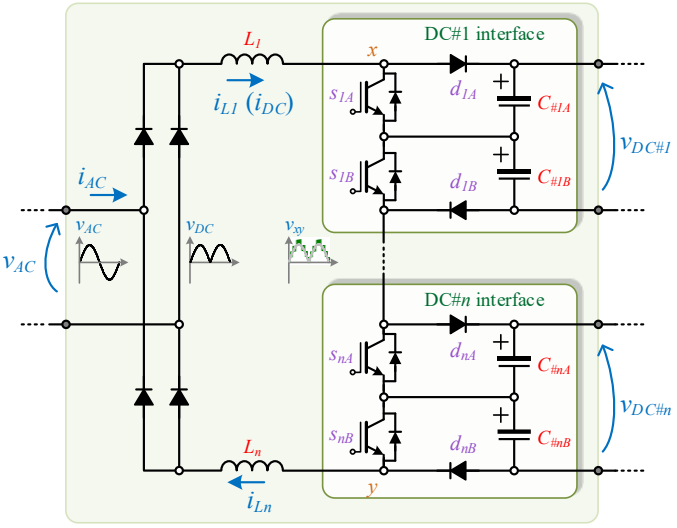

Fig. 2. Detailed structure of the proposed PFC rectifier showing its modularity for n DC interfaces.

Based on (1) and (2), for n=2, the proposed PFC rectifier permits the operation with 5 distinct voltage levels and a controlled current having a ripple with a frequency four times more than the individual switching frequency. These features, mainly considering that they are combined for any conditions of operations, represents attractive functionalities of the proposed PFC rectifier. As the multilevel feature permits the operation of the power devices with lower voltages, the maximum voltage applied to each switching device ($v_{sn\{A,B\}}$) and to each diode ($v_{dn\{A,B\}}$) of each DC interface is defined as function of the voltage of each DC interface ($v_{DC\#n}$), according to:

$$v_{sn\{A,B\}} = v_{dn\{A,B\}} = \frac{v_{DC\#1} + \cdots + v_{DC\#n}}{2n}\,. \tag{3}$$

It is valuable to highlight that the proposed PFC rectifier is based on a boost structure, therefore, the sum of the voltage of the DC interfaces must be greater than the maximum instantaneous value of the AC-side voltage (cf. Fig. 1). With the objective to control the PFC rectifier for an interleaved-based operation, it is necessary to consider individual PWM carriers and a single control reference. Consequently, the PWM carriers must be phase-shifted with an angle (ϕ_{PWM}) obtained from:

$$\phi_{PWM} = \frac{360}{n}\,, \tag{4}$$

and the amplitude must be in accordance with the sum of the voltages of all DC interfaces. The control reference is obtained according to the control algorithm presented in Section III.

III. Proposed PFC Rectifier: Controlling Algorithm

The proposed PFC rectifier operates with main objectives of controlling the AC-side current and the DC-link voltages. The control of the AC-side current is performed according to the operating power of each DC-link, but independently of the number of individual DC interfaces on the DC-side. Analyzing Fig. 2, it is possible to establish the following relation of voltages:

$$|v_{AC}(t)| - v_{L1}(t) - v_{L2}(t) - v_{PFC}^{*}(t) = 0\,, \tag{5}$$

where $v_{PFC}^{*}(t)$ corresponds to the PFC operating instantaneous voltage, v_{L1} and v_{L2} to the instantaneous voltages in the coupling filters L_1 and L_2, while $|v_{AC}(t)|$ to the instantaneous abs value of the AC-side voltage. This equation is valid for any operation mode and operating power. Considering that the objective is to control the current on the coupling L_1 and L_2 filters, such equation can be written as:

$$|v_{AC}(t)| - L_1\frac{d}{dt}i_{L1}(t) - L_2\frac{d}{dt}i_{L2}(t) - v_{PFC}^{*}(t) = 0\,. \tag{6}$$

The voltage $|v_{AC}(t)|$ can be obtained directly from the acquired voltage of the AC-side voltage, but it can introduce issues if such voltage is not purely sinusoidal, e.g., if the AC-side voltage contains harmonic distortion, frequency deviation, flicker, or other power quality problem, then such issues will be reflected on the consumed AC-side current. Thus, a phase-locked loop is used to mitigate such occurrence. Since the current on L_1 is the same of the current on L_2, then the previous equation can be simplified to:

$$|v_{AC}(t)| - (L_1 + L_2)\frac{d}{dt}i_{L\{1,2\}}(t) - v_{PFC}^{*}(t) = 0\,. \tag{7}$$

From the analysis of this equation and Fig. 2, it is recognized that the current $i_{L\{1,2\}}$ is the variable that is controlled according to the operating voltage of the PFC rectifier. In other words, the amplitude and waveform of the current is controlled as a function of the PFC operating voltage v_{PFC}^{*}. This voltage is controlled with a fixed frequency and compared with a PWM carrier, guaranteeing that the proposed PFC rectifier operates with fixed switching frequency. Since the state of the PFC rectifier is defined according to the sampling frequency, it is important to analyze the control algorithm in discrete time. Therefore, by utilizing a forward Euler method, the previous equation is written as:

$$\begin{aligned} &|v_{AC}[k,k+1]| - v_{PFC}^{*}[k,k+1] - \\ &\left(i_{L\{1,2\}}[k+1,k+2] - i_{L\{1,2\}}[k,k+1]\right)\frac{(L_1+L_2)}{T_s} = 0\,, \end{aligned} \tag{8}$$

which represents the digital implementation of the main control equation for the period correspondent to [k, k+1]. Dissecting in further detail, the PFC rectifier must operate with a voltage v_{PFC}^{*} during the interval [k, k+1], determined with the values of the measured voltage v_{AC} and the measured current $i_{L\{1,2\}}$ also during the same interval [k, k+1], as well as the current for the period [k+1, k+2], which corresponds to the current that the PFC rectifier must reach after a sampling control [k, k+1]. Consequently, such current corresponds to the reference current of the PFC rectifier. Summarizing, it is necessary to establish the reference of current for the interval [k, k+1] that is applied in equation to define the operating voltage of the PFC rectifier. As previously mentioned, the waveform of the reference of current is defined by the signal from the phase-locked loop, but the amplitude is established as a function of the operating power. The equation that defines the reference of current is established by:

$$i_{L\{1,2\}}^{*}[k,k+1] = \frac{|v_{AC}[k,k+1]|}{{V_{AC}}^{2}[k,k+1]}\sum_{n=1}^{N}\left(p_{DC\#n}[k,k+1]\right)\,, \tag{9}$$

where N corresponds to the number of DC-link interfaces and it is verified that it is necessary to consider the RMS value of the AC-side voltage, whose digital implementation for [k, k+1] is defined by:

$$V_{AC}[k,k+1] = \frac{1}{M}\sqrt{\sum_{i=1}^{M} v_{ac}[i]^2}\,, \tag{10}$$

where, for a sampling frequency of 40 kHz, M is 800. The operating power of each DC interface is divided in two parcels: the power obtained directly from the voltage and current during each sampling time and the power necessary to control the DC-link voltage. The DC-link voltage can be controlled by a PI.

IV. Proposed PFC Rectifier: Computational Validation

The validation of the proposed PFC rectifier was carried out with the software PSIM, considering $n = 2$ (cf. Section II), an AC-side voltage with RMS value of 230 V, coupling inductive filters of 500 µH, coupling capacitive filters of 5 mH, sampling frequency of 40 kHz, and switching frequency of 20 kHz. Fig. 3 shows, during five cycles of the AC-side voltage, the AC-side voltage and current, and the current on the DC-side, i.e., at the input of the active stage of the proposed PFC rectifier. The current on the AC-side has a sinusoidal waveform, which is the main characteristic of the PFC rectifier. In addition to the sinusoidal waveform, the current and voltage on the AC-side are in phase, thus ensuring operation with a unit power factor. On the other hand, as expected, the current on the DC-side has a rectified current waveform. In fact, as previously described, the current is controlled on the active side of the proposed PFC converter ($i_{L\{1,2\}}$), i.e., the reference current has the waveform of this rectified current. Fig. 4 shows again the voltage and current on the AC-side of the proposed PFC rectifier, during a cycle of the AC-side voltage, as well as the voltage in each capacitor of the DC interface #1. In the case of the voltage in each capacitor of the DC interface #2, the waveform is the same, showing the same behavior. With this result, it is possible to verify that the voltage of each of the capacitors of the DC interface #1 has a frequency that is twice the frequency of the AC-side voltage, representing a traditional characteristic of a conventional PFC rectifier. This result was obtained considering a reference voltage of 100 V, where it is possible to visualize that this value is reached when the voltage and current on the AC-side side reaches the maximum, zero or minimum values.

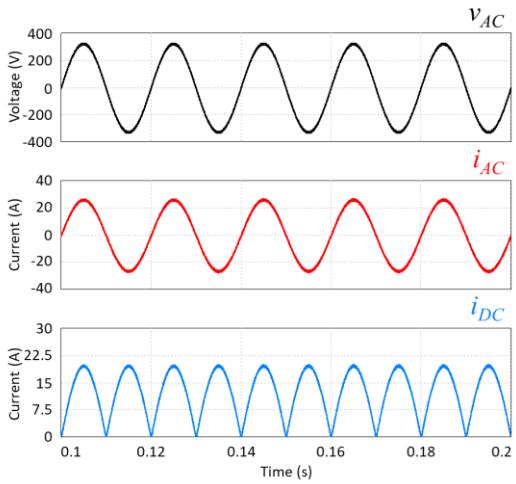

Fig. 3. Validation in steady-state, showing the AC-side voltage and current (v_{AC} and i_{AC}), and the current on the DC-side (i_{DC}), i.e., at the input of the active stage of the proposed PFC rectifier.

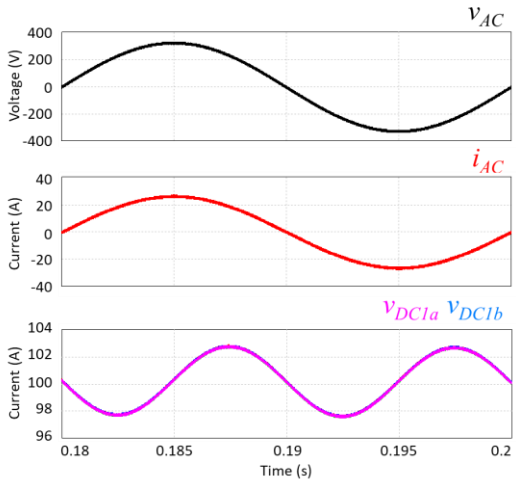

Fig. 4. Detail of voltage in each capacitor of the DC interface #1 ($v_{DC\#1a}$ and $v_{DC\#1b}$) and its relationship with the AC-side voltage (v_{AC}) and current (i_{AC}).

In Fig. 5, it is possible to verify the current on the DC-side (which is the current that is controlled on the active side of the proposed PFC rectifier), the operating voltage of the PFC on the active side and the voltage in each capacitor of both #1 and #2 DC interfaces. The voltage of each capacitor is controlled to a value of 100 V (as it turns out, it corresponds to the voltage detail shown in the Fig. 4), resulting in a maximum voltage value that the PFC rectifier is capable of operating, with a value of 400 V. Thus, the operating voltage of the PFC rectifier has up to a maximum of 5 different voltage levels, as clearly shown in Fig. 5. These levels are obtained according to the voltage of each capacitor of each DC interface and according to the maximum value of the voltage on the AC-side. As previously mentioned, it is possible to increase the number of operating levels of the PFC rectifier, increasing the number of active elements on the DC side of the proposed PFC rectifier. The PFC voltage has a frequency of 100 Hz, i.e., as expected, double the frequency of the AC-side voltage. Obviously, the voltage value in each capacitor can be adjusted to obtain other voltage levels. If the voltage at each DC interface is not controlled to the same value, the voltage of the PFC will not be balanced between the different levels, despite maintaining the same frequency, and in an extreme case it may cease to operate with the five identified levels.

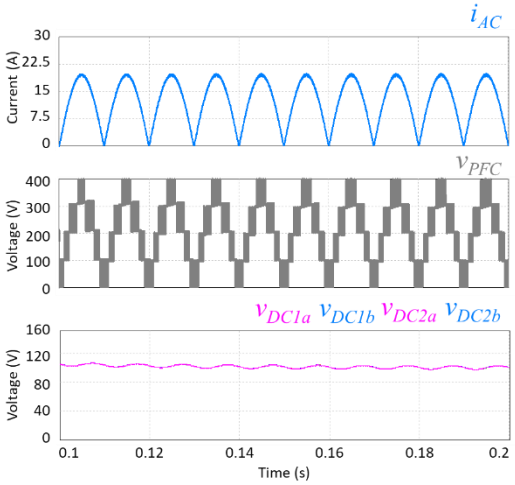

Fig. 5. Validation of the DC-side current (i_{DC}), and its relationship with the operating voltage of the proposed PFC rectifier (v_{PFC}), and with the voltage in each capacitor of the DC interfaces #1 and #2 ($v_{DC\#1a}$, $v_{DC\#1b}$, $v_{DC\#2a}$, $v_{DC\#2b}$).

Fig. 6 shows the current on the active side of the PFC rectifier compared to its reference, allowing to verify that the current follows the reference. In detail, it is possible to verify the value change in the reference current. As it turns out, the reference current is updated with a frequency of 40 kHz, which corresponds to the sampling frequency. In this figure, it is also possible to verify in detail the operating voltage of the PFC rectifier and establish the relationship between this voltage and the current. In this specific case, it is verified that the operating voltage of the PFC rectifier varies between 200 V and 300 V, and when the PFC assumes the value of 200 V, the current ripple presents a positive slope and when the PFC assumes the value of 300 V, the current ripple has a negative slope. Although the switching frequency of each IGBT is 20 kHz, the resulting current has a ripple with a frequency of 80 kHz (i.e., four times higher), validating the interleaved-based operation. Obviously, the operating voltage of the PFC rectifier also has a frequency of 80 kHz in the change between voltage levels. In this figure, it is also possible to verify the four carriers, each with a frequency of 20 kHz, and the respective comparison signal, which is common to all carriers, allowing the PFC rectifier to operate with characteristics of an interleaved converter and that each IGBT is switched with a frequency of 20 kHz.

Fig. 7 shows the four carriers, the comparison signal with the carriers, as well as the 4 control signals of the IGBTs. As it turns out, the IGBTs are in the on state when the carrier is higher than the reference signal and in the off state when it is lower. As expected, the control signals of the IGBTs are 90 degrees apart (360 divided by 4, which is the number of IGBTs). As previously mentioned, increasing the number of DC interfaces on the active side of the PFC rectifier, it is necessary to increase the number of carriers and, therefore, the phase shift between them is smaller (i.e., 360 to divide by n, where n is the number of IGBTs). In this way, the proposed PFC rectifier is controlled guaranteeing the same principle of operation as an interleaved converter, where the resulting current presents a ripple with a frequency four times

higher than the switching frequency of each IGBT. This result was obtained under the same conditions as the results shown in the Fig. 6, with the duty-cycle being approximately 33%.

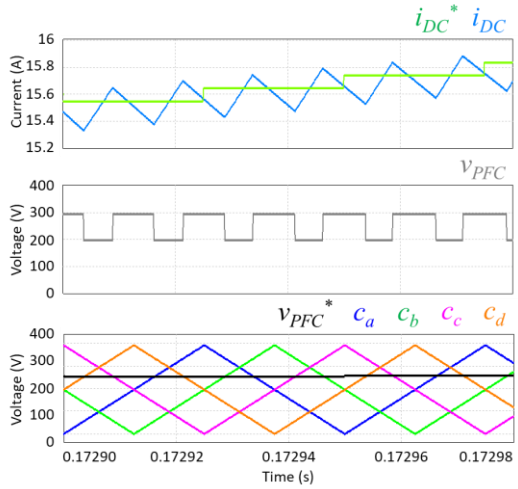

Fig. 6. Detail of the comparison between the DC-side current (i_{DC}) and its reference (i_{DC}*), as well as the relationship with the operating voltage of the PFC rectifier (v_{PFC}), PWM carriers (c_a, c_b, c_c, c_d), and PWM control reference (v_{PFC}*).

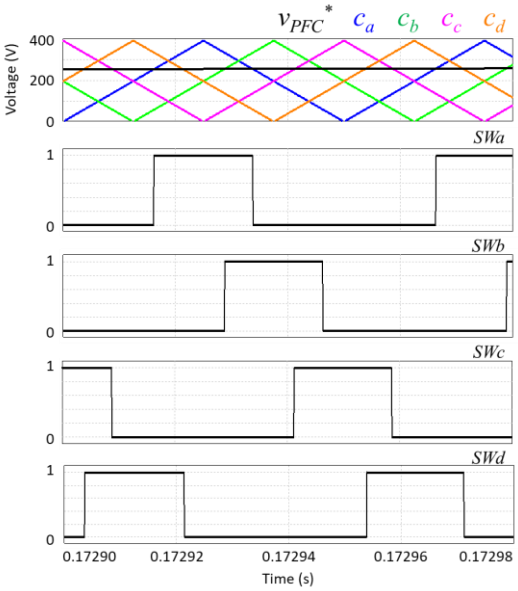

Fig. 7. Detail of the comparison between the PWM control reference (v_{PFC}*) and the PWM carriers (c_a, c_b, c_c, c_d), and the resultant control signals for each IGBT (S_{Wa}, S_{Wb}, S_{Wc}, S_{Wd}) of the proposed PFC.

Fig. 8 shows a detail of the current on the DC-side, the operating voltage of the PFC rectifier and the voltage applied to each IGBT. As can be seen, and as expected, the current presents a ripple with a positive or negative slope according to the variation of the operating voltage of the PFC rectifier. The variation of the operating voltage of the PFC rectifier is established according to the switching state of each IGBT, therefore, the voltage in each IGBTs is variable. It is a specific case, but it is proved that the maximum voltage applied to each IGBT assumes a maximum value of 100 V, which corresponds to the sum of the voltage in each of the capacitors of a given DC interface. As in the time interval presented, the current takes on small values (between 2 A and 4 A), the operating voltage of the PFC rectifier varies between 0 V and 100 V and the IGBTs are never in the on state at the same time, so, logically, the voltage in each IGBT is never overlapping. In this situation, the duty-cycle is approximately 10%.

On the other hand, Fig. 9 shows a result like the previous one, but in a period when the current reaches its maximum value. Thus, in this case, it is verified that the operating voltage of the PFC rectifier assumes values varying between 300 V and 400 V. In this situation, the IGBTs are mostly in the on state and there are times when are in the on state at the same time, with overlapping voltages. This situation is very different from the previous case, as the duty-cycle is approximately 90%.

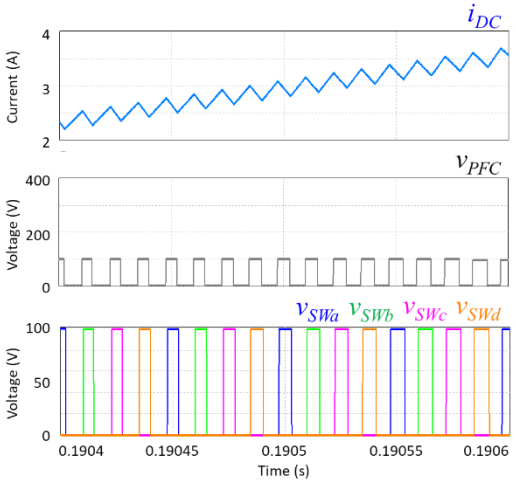

Fig. 8. DC-side current (i_{DC}), operating voltage of the proposed PFC rectifier (v_{PFC}), and the control signals of each IGBT (v_{SWa}, v_{SWb}, v_{SWc}, v_{SWd}), for operation with a duty-cycle of almost 10%.

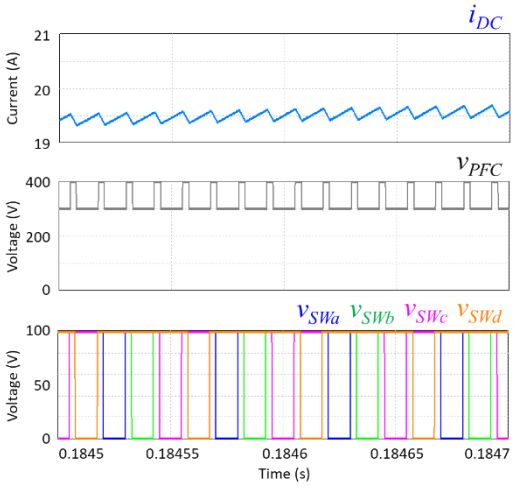

Fig. 9. DC-side current (i_{DC}), operating voltage of the proposed PFC rectifier (v_{PFC}), and control signals of each IGBT (v_{SWa}, v_{SWb}, v_{SWc}, v_{SWd}), for operation with a duty-cycle of almost 90%.

A detail is shown in Fig. 10, where it is possible to visualize the evolution of the current on the DC-side due to a sudden change in the reference current. Before the variation, the current perfectly follows its reference, being centered on the reference. When the variation occurs, in this case an instantaneous reduction of the current value by 50%, the PFC rectifier controls the current so that it can follow the reference in the shortest

possible time. The steady-state is reached after 50 µs, representing a satisfactory dynamic response and without causing any disturbance in the current waveform, except for the necessary change according to the reference.

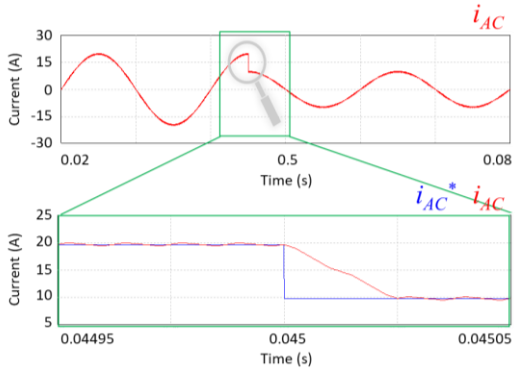

Fig. 10. Detail in transient-state showing the AC-side current (i_{AC}) and its reference (i_{AC}*) considering a sudden variation of 50% in the reference.

V. Conclusions

A proposed multilevel interleaved-based PFC rectifier with a design that permits a modular DC-link is proposed in this paper. The explanation of the proposed PFC rectifier and the control algorithms are shown according to the principal features, such as the multilevel operation, the interleaved-based current control, and the modular possibility of obtaining distinct DC-links. Along the paper is demonstrated that these features are combined at the same time, representing an added value of the proposed PFC rectifier. The validation was performed considering two independent DC-links. The obtained results permit to verify that the proposed PFC rectifier, besides the operation with sinusoidal current and unitary power factor, operates with five voltage levels and a controlled current with a frequency that corresponds to the quadruple of the switching frequency of each switching device. The presented results validate the advantages of the proposed PFC rectifier for distinct conditions of operation, in steady-state and transient-state, and highlight the possibility of operating with all the features mentioned at the same time.

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