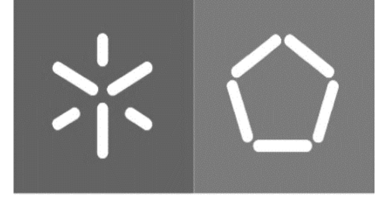
Universidade do Minho
Escola de Engenharia

Gonçalo Fernandes Ferreira de Almeida

Power management circuit for piezoelectric energy harvester

July 2020



Universidade do Minho
Escola de Engenharia

Gonçalo Fernandes Ferreira de Almeida

Power management circuit for piezoelectric energy harvester

Master dissertation
Master degree in Biomedical Engineering
Medical Electronics

Dissertation supervised by
Professor Paulo Mateus Mendes
Professor Tao Dong

July 2020

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Thank You! Obrigado!

STATEMENT OF INTEGRITY

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Circuito de controlo para acumulação de energia piezoelétrica

RESUMO

Esta dissertação de mestrado apresenta um estudo na área *CMOS* em circuitos analógicos / digitais inseridos num circuito integrado responsável por estabelecer interface entre o transdutor e a sua aplicação. O design de circuitos de referência (tensão e corrente) e a implementação de um oscilador limitado pela tensão de referência são descritos nesta dissertação. Estes circuitos assumem uma função crucial para o objetivo primordial do projeto. A tecnologia *CMOS* empregada foi de 130nm com um *software* EDA do qual foi realizado o *layout*. A tecnologia escolhida foi um dos requisitos impostos pelo projeto.

O trabalho desenvolvido compreendeu todas as etapas necessárias para desenvolver um projeto de *ASIC*. Deu-se primazia a simulação dos circuitos, a otimização, o *layout* físico, a extração de parasitas, a validação do *layout* físico e a fabricação do circuito integrado.

Quando se aplicou uma fonte de tensão de 1-3.2V a um circuito de tensão de referência, este gerou uma tensão constante de 258mV, com uma sensibilidade de 0.49%/V. Este circuito apresentou um *PSRR* de 58dB, a 100Hz.

O oscilador produziu um sinal periódico de 84.81kHz e teve a capacidade de controlar o *switch* responsável pelo armazenamento da tensão extraída do piezoelétrico para um condensador.

A corrente de referência foi capaz de gerar 41.5nA, a 2V de fonte de alimentação, com 0.19nA/°C. Embora, os coeficientes de temperatura nos circuitos de referência não tenham sido satisfatórios, estes apresentaram capacidade em polarizar outros circuitos no chip produzido.

Palavras-Chave: *ASIC*, circuitos de baixo consumo, circuitos de referência, *CMOS*, oscilador.

Power management circuit for piezoelectric energy harvester

ABSTRACT

The master dissertation presents a study in the area of mixed analogue/digital signals of CMOS circuits integrating a power management circuit for energy harvester. Focusing on the development of a current and voltage referencing circuits, and a current starved voltage-controlled oscillator addressing low power demands. The circuit components are designed based on 130nm CMOS technology. A physical layout of all the intervenient components described in this project report was developed for fabrication purposes. The choice of this technology adjusts to the research requirements benefiting its robustness, costliness, and performance.

The developed work comprises the necessary steps to perform an ASIC project, comprising on circuit schematic optimization and simulation, physical layout design, parasitic extraction, validation of the physical layout, integrated circuit fabrication.

A robust voltage reference is capable of outputting a stable 258.35mV with a line sensitivity of 0.49%/V in response to a 1-3.2V voltage supply, also presenting an excellent power supply rejection ratio of 58dB at 100Hz. An implemented current starved voltage-controlled oscillator generates an average periodic signal at a frequency of 84.81kHz. This circuit shows the capability to produce a local clock time to release the stored scavenged from the energy harvester to an application. A current reference can generate a 41.5nA at 2V of power supply, with a 0.19nA/◦C. Although the temperature coefficient is not very useful, a self-biased current and voltage reference shows the capability to provide bias for other circuits within the integrated circuit.

Keywords: ASIC, CMOS, low-power circuits, oscillator, referencing circuits.

CONTENTS

CHAPTER 1 Introduction 1

CHAPTER 2 State of the art 5

2.1 MOSFET modelling 7

2.2 Bipolar Junction Transistor 12

2.2.1 Different Configurations 13

2.3 BJT versus MOSFET 15

2.4 Short-channel MOSFET 17

2.5 Short-channel effects 19

2.5.1 PN Reverse-Bias Current (I1) 19

2.5.2 Weak Inversion (I2) 20

2.5.3 Drain-Induced Barrier Lowering (I3) 21

2.5.4 Gate Induced Drain Leakage (I4) 23

2.5.5 Punch-through (I5) 24

2.5.6 Narrow Width Effect (I6) 25

2.5.7 Gate Oxide Tunneling (I7) 25

2.5.8 Hot Carrier Injection (I8) 26

2.6 Leakage current reduction techniques 27

2.6.1 Multi-threshold voltage designs 27

2.6.2 Voltage Supply Scalling 28

2.6.3 Transistor Stacking 28

2.7 Reference Circuit 30

2.7.1 Voltage Reference 31

2.7.1.1 Voltage reference operating in strong inversion MOSFETs 32

2.7.1.2 Voltage reference operating in subthreshold inversion MOSFETs 33

2.7.1.3 Voltage reference consisting of subthreshold inversion MOSFETs 34

2.7.2 Current reference 35

2.7.2.1 Current reference based on self-biasing without resistors 36

2.7.2.2 Current Reference consisting of subthreshold MOSFETs 36

2.7.3 Summary reference circuits ... 37
2.8 Oscillator ... 39
2.8.1 Important oscillator properties ... 39
2.8.1.1 Non-deterministic frequency stability ... 39
2.8.1.2 Power dissipation ... 40
2.8.1.3 Deterministic frequency stability and accuracy ... 40
2.8.1.4 System integration and miniaturization ... 40
2.8.2 Electrical Oscillators ... 41
2.8.2.1 LC Harmonic Oscillator ... 42
2.8.2.2 RC Harmonic Oscillator ... 43
2.8.3 Electrical Relaxation Oscillator ... 44
CHAPTER 3 Development ... 47
3.1 Voltage reference ... 48
3.1.1 Circuit Theory ... 49
3.1.1.1 Subthreshold Operation of MOSFETs ... 49
3.1.1.2 Deep-triode region MOSFETs ... 50
3.1.2 Circuit Topology ... 51
3.1.2.1 Start-up Circuit ... 52
3.1.2.2 PTAT current generator circuit ... 53
3.1.2.3 CTAT Voltage Generator Stage ... 55
3.1.3 Results and Discussion ... 55
3.1.4 Layout Design ... 59
3.1.5 Summary ... 60
3.2 Current Staved Voltage Controlled Oscillator ... 62
3.2.1 Results and Discussion ... 63
3.3 Current Reference ... 71
3.4 Layout ... 76
3.5 Future Biomedical Applications ... 78
CHAPTER 4 Conclusion ... 80
CHAPTER 5 Support Material ... 90

5.1 Fabrication Report (wafer Acceptance test and site report) 90
5.2 Layers Report 91
5.3 Circuit Schematics 92
5.4 Physical Layout 93
5.4.1 Ring Pads 93
5.4.2 Voltage Reference 94
5.4.3 Current Reference 95
5.4.4 Current Starved VCO 96
5.5 Chip Photos 97
5.5.1 Overall Chip 97
5.5.2 Pads and ESD protection 98
5.5.3 Comparator Array 2 99
5.5.4 VCO (with Voltage Reference) 100
CHAPTER 6 Publications 101
6.1 Paper 1 101
6.2 Paper 2 101

List of Figures

Figure 1: Illustration of available energies extracted from different sources in typical application environments (Squires, 2015). 2

Figure 2: Schematic of the proposed Power Management Circuit. 3

Figure 3: CMOS inverter:(a) Physical structure, (b) cross-sectional diagram (Anderson & Anderson, 2018). 6

Figure 4: Illustration of an equivalent circuit when all the terminals of a NMOS transistor are grounded. Verification of the existence of inversely biased diode between the p-n junction of the drain, source terminals and the substrate (Ayers & Ayers, 2018). 8

Figure 5: Illustration of the triode operation region on a NMOS transistor with $V_{GS} > V_{th}$ and $V_{DS} > 0$ (Smith et al., 2008). 9

Figure 6: Illustration of NMOS transistor cross-section, and its behavior on saturation region. Presence of a pinch-off point due to the high potential applied on the drain terminal (Bahcall, Kadanoff, Bienenstock, Bahcall, & Condensate, 2005). 10

Figure 7: I_{DS} - V_{DS} output characteristics of the different MOSFET operation regions (Ayers & Ayers, 2018). 10

Figure 8: Structure of a Bipolar Junction Transistor: (a) npn transistor, and (b) pnp transistor (Cowles, 2017). 12

Figure 9: Traditional scaling-down factors on MOSFET parameters (Bohr & Young, 2017). 17

Figure 10: Total chip dynamic and static power dissipation trends based on the International technology Roadmap for Semiconductors. The two power plots for static power represent the 2002 ITRS projections normalized to those for 2001. The dynamic power increase assumes a doubling of on-chip devices every two years (Kim et al., 2003b). 18

Figure 11: Leakage mechanisms in short-channel transistors (Rahmat bin Sanudin, 2005). 19

Figure 12: I_D versus V_G NMOS characteristics. Visualization of the different short-channel leakage current, such as GIDL, DIBL, weak inversion and junction leakage (K Roy et al., 2003). 20

Figure 13: Variation of the depletion region underneath the gate, resulted from the different minority carrier concentration whenever the channel of the MOSFET is biased in weak inversion (K Roy et al., 2003). 21

Figure 14: Difference of the potential barrier of the electrons in short and long channel MOSFET, and its influence on the variation of drain potential (Tonk, 2016). 22

Figure 15: Threshold voltage shift of a MOSFET device for drain voltages of 0.1V and 1.5V in linear and saturation regions (Stockinger, 2000). 23
Figure 16: Influence of the electric field from the gate and temperature dependence associated with gate induced drain leakage (Alnuaimi, Nayfeh, & Koldyaev, 2013). 24
Figure 17: Illustration of depletion region resulted in punch-through leakage current (Tonk, 2016). 25
Figure 18: Parameters in the fabrication process that influence the threshold voltage, (a) different channel doping profiles, (b) variation on channel length, (c) oxide thickness (K Roy et al., 2003). 28
Figure 19: Transistor stack effect, (a) Stacking effect in two-input NAND gate (K Roy et al., 2003), (b) Subthreshold leakage current in different stacks of off-transistors (Dilip, Prasad, & Bhavani, 2012). 29
Figure 20: CMOS schematic and layout, in the layout view, the component with the red rectangle is the CMOS resistor. It is possible to observe the difference of occupied area between the CMOS resistor and transistors. 31
Figure 21: Voltage reference consisting of M_3-M_8 operating in strong inversion region, and M_1 and M_2 operating in subthreshold region (De Vita et al., 2006). 33
Figure 22: Voltage reference circuit operated in the strong inversion and subthreshold regions using high-V_{th} devices (De Vita & Iannaccone, 2007) 34
Figure 23: Voltage reference consisting on all MOSFET operated in subthreshold region, except for M_{R1}, which operates in triode region (Ken Ueno et al., 2009). 35
Figure 24: Modified β multiplier self-biasing circuit without resistors. Transistor M_1 and M_2 operates in subthreshold region, M_3 operates in triode region, and M_4 operates in saturation region (Oguey & Aebischer, 1997). 36
Figure 25: Schematic of a current reference consisting in subthreshold MOSFET, except M_3 which is a MOS resistor, operating in triode region, and M_4 which is a diode-connected transistor, operating in saturation region (K. Ueno et al., 2015). 37
Figure 26: LC-Oscillator configuration, (a) Colpitts, (b) Hartley. 43
Figure 27: RC oscillator feedback network using a BJT to sustain the circuit (Arim, Lam, & Ordin, 2014). 44
Figure 28: Circuit schematic of a conventional relaxation oscillator and its output waveform (Gierkink & Tuij, 2002). 45
Figure 29: Resistorless voltage reference circuit schematics. Composed by a start-up circuit, a PTAT current generator, and a CTAT voltage generator. 48

Figure 30: I-V behavior of a MOSFET in triode region. Presence of two different behaviors that complemented results in the MOSFET triode region. 51

Figure 31: Schematic of the Start-up circuit. This circuit ensures the bias to the voltage reference optimal point. 53

Figure 32: Simulation results about the variation of the output reference voltage with the increment of voltage supply. 56

Figure 33: Simulation results about the variation of the output reference voltage with temperature. 57

Figure 34: Simulation results of the power supply rejection ratio depending on the frequency at V_{DD}=2V. 58

Figure 35: Power consumption of the voltage reference voltage with variation of the voltage supply and increment of temperature. 58

Figure 36: Voltage reference measurements through different voltage supplies and temperatures. 59

Figure 37: Schematic of the current starved VCO. 63

Figure 38: Current Starved VCO output waveform. A) a representation of the behavior of the periodic output voltages of the three implemented delay stages (N=3) of a current starved VCO. The working region of MOS devices are also indicated. B) a representation of the charging process, and C) discharging process. 65

Figure 39: Variation of the oscillator frequency and maximum output voltage through voltage supplies alterations. Categorization of two independent oscillation region, being the oscillation zone the appropriate for circuit purpose. 66

Figure 40: Variation of the oscillatory frequency with the increment of temperature. Verification of the influence of the inappropriate TC of the voltage reference. 67

Figure 41: Oscillator power consumption with variation of voltage supply and temperature. 68

Figure 42: Variation of the period jitter for a specific period of time. 69

Figure 43: Statistical Monte Carlo Analysis of frequency oscillation deviation for V_{DD}=3V at 27°C. The voltage reference was kept at 257.7mV. 70

Figure 44: A) Chip micrograph view of the proposed Current Starved VCO. B) Respective layout design and differentiation of sub-circuit blocks. 70

Figure 45: Illustration of the current reference function. It shows how is possible to achieve the temperature compensated current. 71

Figure 46: Architecture of a current reference using deep triode (MR1, MR2) and subthreshold MOSFET (M3). This circuit consists in three different sub-circuits, a PTAT current, CTAT, and a current adder. 71
Figure 47: Simulation results about the PTAT behavior of the current reference sub-circuit. 73
Figure 48: Simulation results concerning the current reference CTAT sub-circuit. 73
Figure 49: Variation of the output current due to fluctuations of voltage supply. 74
Figure 50: Variation of the output current with variation of temperature and voltage supply. 75
Figure 51: Power consumption of the current reference circuit for different temperatures and voltage supplies. 76
Figure 52: Schematic representation of a sandwich ELISA format, exemplification of a signal detection between a biomarker and substrate (Xuan Chen et al., 2019). 78
Figure 53: Schematic representation of a redox reaction detection on a functionalized FET gate, which the released electron activates a flowing current through the device. The amount of produced current is proportional to the binding reaction between the aptamer and the biomarker (Xiaoyan Chen et al., 2019). 79
Figure 54: Wafer acceptance test and site report. 90
Figure 55: Statistics of the number of layers used on the layout the IC. 91
Figure 56: Complete circuit and its schematic in Cadence software. 92
Figure 57: Layout of the ring pads provided by the external foundry. 93
Figure 58: Layout of the developed voltage reference circuit. 94
Figure 59: Layout of the developed current reference circuit. 95
Figure 60: Layout of the developed current starved VCO. 96
Figure 61: Implemented IC chip, under a microscope view, with 20 × amplification. 97
Figure 62: Microscope view of the pads and ESD protection with 100 × amplification. 98
Figure 63: Microscope view of the voltage reference integrated in the negative input of the peak detector with 100 × amplification. 99
Figure 64: Microscope view with 100 × amplification of the voltage controlled VCO with integrated voltage reference. 100

List of Tables

Table 1: Output characteristics and its bias conditions of the operation region of a NMOS type MOSFET 11

Table 2: Condition and modes of operation of a bipolar junction transistor. 13

Table 3:Intrinsic characteristics of different bipolar junction transistor configurations. 14

Table 4:Overview comparison between the MOSFET (NMOS) and the BJT (npn). 16

Table 5: Advantages (green) and disadvantages (red) of electrical and mechanical oscillators. 42

Table 6: Aspect ration of the critical transistors of the voltage reference circuit. 52

Table 7: Research Comparison 61

Table 8: Specifications of the current starved VCO components. 63

Table 9: Dimension of the critical transistor of the current reference circuit. 72

Acronyms

ASIC	*Application Specific Integrated Circuits*
BGR	*Bandgap Voltage Reference*
BJT	*Bipolar Junction Transistor*
CMOS	*Complementary Metal-Oxide-Semiconductor*
CTAT	*Complementary To Absolute Temperature*
DC	*Direct Current*
DIBL	*Drain-Induced Barrier Lowering*
DRC	*Design Rule Check*
ERC	*Electric Rule Check*
FET	*Field-Effect Transistor*
GIDL	*Gate Induced Drain Leakage*
IC	*Integrated Circuit*
KVL	*Kirchhoff's Voltage Law*
LED	*Light-Emitting Diode*
LNA	*Low-Noise Amplifier*
LOCOS	*LOCal Ocidation of Silicon*
LVS	*Layout Versus Schematic*
MEMS	*MicroElectroMechanical Systems*
MOS	*Metal-Oxide.Semiconductor*
MOSFET	*Metal-Oxide-Semiconductor Field-Effect- Transistor*
NMOS	*N-type Metal-Oxide-Semiconductor*
PMC	*Power Management Circuit*
PMOS	*P-type Metal-Oxide-Semiconductor*
PTAT	*Proportional To Absolute Temperature*
PVT	*Process, Voltage and Temperature*
RF	*Radiofrequency*
Si	*Silicon*
SMIC	*Semiconductor Manufacturing International Corporation*
TC	*Temperature Coefficient*

VCO	*Voltage-Controlled Oscillator*
VLSI	*Very-Large System Integrated*
WSN	*Wireless Sensor Network*

CHAPTER 1 INTRODUCTION

Internet availability among people favored the emergence of myriad linked smart devices with a connecting interface. It is capable of recognizing, enhance, and share information without or less human intervention (Silva, Khan, & Han, 2017). This needful universal bond of people, objects, and services (Internet of Things) has become the catchword for the modern wireless communication era.

WSN devices have a leading role in “pervasive computing” areas. It incorporates diversified applications, such as smart buildings, monitoring physiological parameters, environmental sensing, monitoring industrial operations, and biomedical applications (Kausar, Reza, Saleh, Saleh, & Ramiah, 2014).

Advancements in microelectronic technology allowed integration of more functionalities within a small device and flourished other auspicious technologies, such as batteries. However, in many battery powered-up WSN applications, the batteries constitute a bottleneck to electronic demands and, environmental nightmares. Its continuous replacement and disposal limit the device lifetime and higher environment endanger. Also, most of these applications are in hard-to-reach-places, which contributes to higher maintenance costs. (Kausar et al., 2014).

A WSN consists of a vast number of sensor nodes; each device possesses different functionalities, which, as a network, has multi-tasking performance. However, upon the process of communication, these devices consume a high level of energy, which reduces its lifetime if powered-up by a small battery. A new energy technology needs to address the battery dependency issue and consequently extend the WSN lifetime effectively. Energy Harvesting is a promising technology that can fulfill that gap. Empower a self-sustainable WSN scavenging the needed power supply from green energy sources. As possible to observe in Figure 1, the different transducer elements and its area harvested power.

Energy Source		Harvested Power
	Photovolataic	
	– Office	10 $\mu W/cm^2$
	– Outdoor	10 $\mu W/cm^2$
	Vibration/Motion	
	– Human	4 $\mu W/cm^2$
	– Industry	100 $\mu W/cm^2$
	Thermal Engergy	
	– Human	25 $\mu W/cm^2$
	– Industry	1-10 mW/cm^2
	RF	
	– GSM (900MHz)	0.1 $\mu W/cm^2$
	–Wi-Fi (2.4GHz)	0.01 $\mu W/cm^2$

Figure 1: Illustration of available energies extracted from different sources in typical application environments (Squires, 2015).

The continuous downscale and efficiency of CMOS technology and microtechnology concerning micro-scale transducers allowed the increment of the harvested power (ALAEI, 2016), (Covaci & Gontean, 2020). Although the difference between the scavenged power and the power consumption of the WSN is getting closer, it still is not enough. Research must be conducted to explore the convenient solution to surmount the power restraint problem. Due to the compatibility between the vibrational (piezoelectric) transducers and MEMS technology allowed an increment of harvested power per unit area (Mamilla, Kumar, & Avulalokesh, 2013), (Saadon & Sidek, 2015). The application purpose of the research project needs high voltage, high energy density, and little mechanical damping. Therefore, a coupled energy harvester (piezoelectric + electromagnetic) constitutes the power generated source of the research project.

The harvested power density for mechanical energy depends on the frequency and magnitude of the applied force, the inertial mass, the maximum displacement, the resonance frequency, and the amplitude of vibration (Covaci & Gontean, 2020).

A naïve approach consists of expanding the energy harvester size, which directly increases the amount of available energy. This implementation is restricted due to the occupied area. However, recent researches are modifying the structure and layers of the piezoelectric (Covaci & Gontean, 2020), (Saadon & Sidek, 2015), Another possible alternative ensures that the minimum scavenged energy is adequate to provide the required energy by the application. But, the lack of green source availability makes this method unsuitable.

A valuable approach reflects on the behavior of piezoelectric crystals. Since most energy harvesters operate in a frequency range inferior to the resonant frequency. Therefore, the piezoelectric elements can be approximated to parallel capacitors (Z. Yang, Zhou, Zu, & Inman, 2018). Scavenged energy is susceptible to the crystal’s vibration frequency. To extract maximum power, a frequency

matching between the piezoelectric crystals and the environment must be accomplished (ALAEI, 2016). This procedure is highly unviable because of the green source's variable and intermittent characteristics.

Previous studies concerning the energy harvester's output signal characteristics have a few properties that must be paid attention, such as low-power signal, random fluctuations, and AC output signal. The last electrical characteristic defines the inaccessibility to power-up directly electronic devices nor charging batteries.

Figure 2 presents the proposed solution, which consists of an adaptive PMC. It possesses high energy efficiency, consuming less compared to the harvested energy. This IC is placed among the energy harvester and the application to extend its operation time and battery independency. It regulates the scavenged energy converting, storing, and relocating suitable energy to the required application under different ambient conditions (Chew, Ruan, & Zhu, 2019). The main requirements for this power management circuit are its low power consumption, along with efficiency and autonomous operation. The basis for this project is the paper entitled up-conversion power extraction circuit for low-frequency energy harvester proposed by (Li, Wen, Yin, & Wu, 2014).

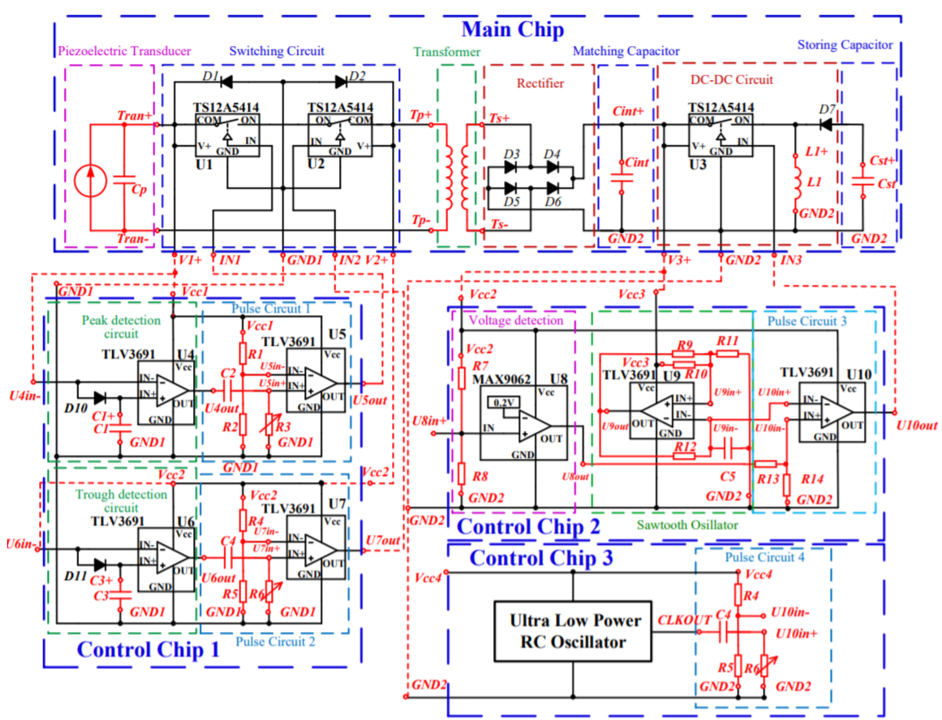


Figure 2: Schematic of the proposed Power Management Circuit.

The goal of the research is to design and simulate a low-power module integrated on a PMC IC. It can scavenge energy efficiently from a random low-power input signal generated by a piezoelectric and electromagnetic transducer. Implementing custom CMOS components, the designed IC is capable to extract the harvested power efficiently under a wide vibration frequency range. It can continuously

accumulate weak energy from the piezoelectric transducer for a long time. And whenever the application needs, e.g., sensor data communication, the system provides a higher output power in a short period.

This essay reports the development, design integrated circuits for harvesting interfaces, and all the necessary steps to perform an ASIC project (circuit schematic optimization and simulation, physical layout design, parasitic extraction, and validation of the physical design, integrated circuit fabrication, and further testing and analysis). It comprises essential analog circuits necessary to control the performance of the PMC IC, such as an oscillator, voltage, and current reference.

The reference circuit is essential to provide a constant voltage or current independent of the voltage supply, temperature, and process variation. These references are suitable to bias properly the building blocks from the main circuit, increasing their efficiency and power consumption. The implemented voltage reference has a crucial role in bursting the stored energy. It is included on the negative input of the voltage detector, where the accumulation peak is compared to the voltage reference through an external voltage divider. Once reached the peak, this circuit is responsible to burst the energy to fulfill its application. A current starved VCO is essential to set a local oscillator responsible for controlling an analog switch to charge the output capacitor.

CHAPTER 2 STATE OF THE ART

The remarkable characteristic of the transistor that was the fuel to the explosive growth in this technology era is that as their size decreases, their production cost reduces, and its speeds increase (Isaac, 2002). Over the last decades, CMOS technology changed the digital world as never before (Haensch, 2006). Several key developments in the semiconductor industry helped enable this revolutionary technology, such as the development of the Si MOSFET, IC, and CMOS circuits. The breakthroughs in semiconductor processing fabrication technology, as well as, a relatively straightforward scaling the transistor size allowed the MOSFET to overcome the BJT technology.

In recent CMOS technologies, dynamic power is decreasing. However, heat dissipation related to the static (leakage) power is increasing (Haron & Hamdioui, 2008). It constitutes the major disadvantage of this technology. In contrast, the advantages of CMOS, such as circuit complexity reduction, high speed transitions, high integration density, ease manufacturer, and high noise immunity, allowed this technology to be the most widely used and implemented in VLSI.

Analog systems carry the signals in the form of physical variables such as voltage, current, which are continuous in time. On the other side, digital systems link the perception of those variables with the physical world. Therefore, the analog circuits are the interface of the digital systems to the physical world. With the development of VLSI technology, it is possible to create a small multi-function device being pervasive in telecommunications, portable consumer electronics, implantable medical devices. Consequently, it is essential to model and design analog circuits to build an accurate, reliable device that allows a better perception of the physical world (Schneider & Galup-Montoro, 2010).

The MOSFET transistor is a semiconductor device that is widely used for switching and amplifying electronic signals in the electronic devices. The aim of the MOSFET is to control the voltage and current flow between the source and the drain. Its behavior is dependent on the existent capacitance that is the channel gate. The semiconductor under the oxide layer forms a bridge between the source and drain terminal. The existent oxide layer on the gate forms a capacitance. Therefore, the working operation of the MOSFET is dependent on the applied voltage on the gate, which accumulates or repels charges to form a depletion region.

As possible to observe in Figure 3, the detailed physical structure of CMOS technology. Due to CMOS complementary, it is possible to integrate with the same material the two existent types of MOSFET, p-type and n-type.

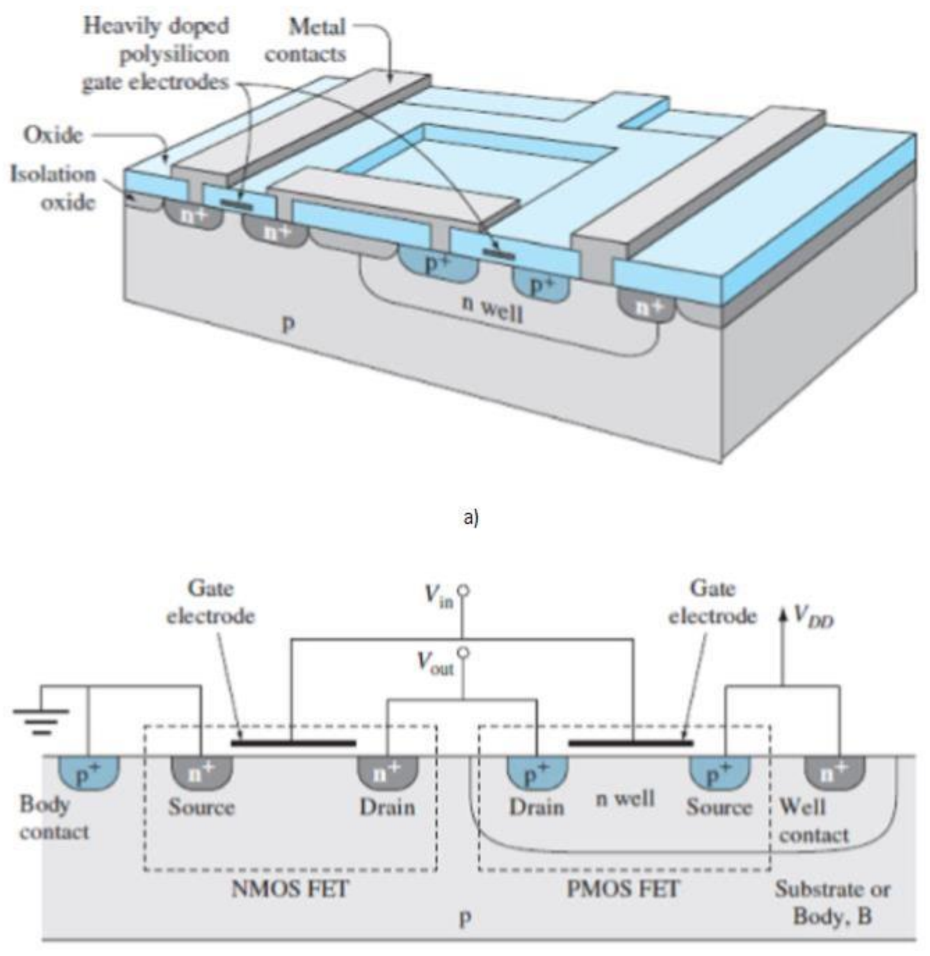


Figure 3: CMOS inverter:(a) Physical structure, (b) cross-sectional diagram (Anderson & Anderson, 2018).

2.1 MOSFET modelling

The trend toward mixed analog-digital signals creates the necessity for appropriate MOSFET modeling for analog and RF designs. Since its influence in analog systems, strong inversions were the only region to be the prevailing MOS operation region. However, with the current technological demands, CMOS technology tends to shrink more and more the channel length to maintain an acceptable level of required performance. Therefore, in this essay, the study of the trend MOSFET modeling is presented and employed on the designed circuits.

As the CMOS technology tries to stay along ith the new electronic demands, these upgrades brought the necessity to change the effective operation of a MOSFET. Nowadays, due to the implications of CMOS technology, the voltage supplies must be reduced to keep up with power requirements. Also, the MOSFETs are designed in a sub-micron (130nm) channel length region, which presents off-state leakage constraints. Therefore, the MOSFETs employed are operated in moderated or weak inversion regions (Schneider & Galup-Montoro, 2010).

The understanding of the MOSFET behavior was a vital process to design the circuits within the PMC IC. As an inversion layer at the MOSFET substrate-oxide interface acts as a conducting channel. Therefore, the depletion region creates a conductive track from the source and drain. Depending on the applied voltage in the gate channel, different operating regions are exhibited, which has a crucial impact on circuit behavior (Nagel & McAndrew, 2004). Within this dissertation, one of the requirements was the employment only of a standard CMOS transistor. It was exploiting the use of the MOSFET gate as a capacitor. Its operation was essential to design the current starved VCO. Also, MOS resistors were used to substitute the use of standard resistors. These standard electronic devices occupy a large layout area and are unreliable to be produced in CMOS.

The NMOS transistor is a strongly nonlinear device. The operation mode of the transistor is highly dependent on voltage bias conditions, as possible to observe in Table 1 and Figure 7. Therefore, four different operating regions are distinguished, such as the cut-off region, weak inversion, linear or triode region, and saturation region.

To start understanding the MOSFET behavior, let us consider that all the terminals are grounded. While the NMOS fabrication, see Figure 3, the source and drain terminals are heavily n+ doped, and the substrate is p-type. Therefore, if the potential on the gate is grounded, the surroundings of the drain and source terminals are made of a back-to-back p-n junction, behaving as inversely biased diodes, as represented in Figure 4. As an inversely biased diode has an extremely high resistance, the current conduction between the source and drain is inexistent. This region of operation is called the cut-off region,

because the potential applied to the gate was not enough to create a depletion region, to overcome the existence of the inversely biased diodes.

Another possible situation, also corresponding to the cut-off region is if resulted in the potential applied to the gate is enough to create a capacitance, being the silicon dioxide as a dielectric. This applied signal to the gate attracts positive charges to the gate, while negative charges are accumulating in the substrate, creating a depletion region under the gate. Nevertheless, no potential difference is created between the drain and the source to force the movement of the minority charges through the gate.

Gate

Source

Drain

Bulk

Figure 4: Illustration of an equivalent circuit when all the terminals of a NMOS transistor are grounded. Verification of the existence of inversely biased diode between the p-n junction of the drain, source terminals and the substrate (Ayers & Ayers, 2018).

When it commutes to on-state, the MOSFET pass through an operating region called weak inversion or subthreshold region. The conditions of the subthreshold region are the potential between the gate and source is approximately equal to the threshold voltage. And, the voltage potential between the drain and the source must be not null. In this case, a small drain current starts to flow through a non-completely conductive channel. As there are not many minority charges accumulated under the gate, and the potential exercised by the drain is not enough to attract the electrons from the source. Therefore, in the weak inversion (or subthreshold) region the current does flow by drift, but by diffusion.

The drain current through the transistor can be calculated similarly as the bipolar transistor. Equation 1 shows the expression to calculate the drain current, also mentioned as subthreshold current, in weak inversion. This similarity was one of the critical points to perform the reference circuits. The state-of-art of the referencing circuits rely on the intrinsic characteristics of BJT (Felipe & Calvillo, 2016), (Ribeiro, Gama, Costa, & Pereira, 2008). The designed circuits overcome the problem related to the BJT devices. Keeping up if the CMOS trend on using MOS resistor and subthreshold MOSFETs to perform the reference circuits. Therefore, the theory relied on the behavior of the BJT on the bandgap reference was the starting point to understand how a new circuit can be made relying on the transistor in a subthreshold region.

$$I_D = \frac{W}{L} \cdot \mu \cdot C_{ox} \cdot (\eta - 1) \cdot V_T^2 \cdot e^{\frac{V_{GS}-V_{th}}{\eta \cdot V_T}} \qquad 1$$

As V_{GS} raises and reaches the critical value equal to the threshold voltage, V_{th} a depletion region under the gate is formed, allowing a conducting channel between the source and drain terminals. If V_{DS} is positive, the drain current is proportional to the applied voltage on the drain terminal. This operating region is called the linear/triode region and its illustrated in Figure 5.

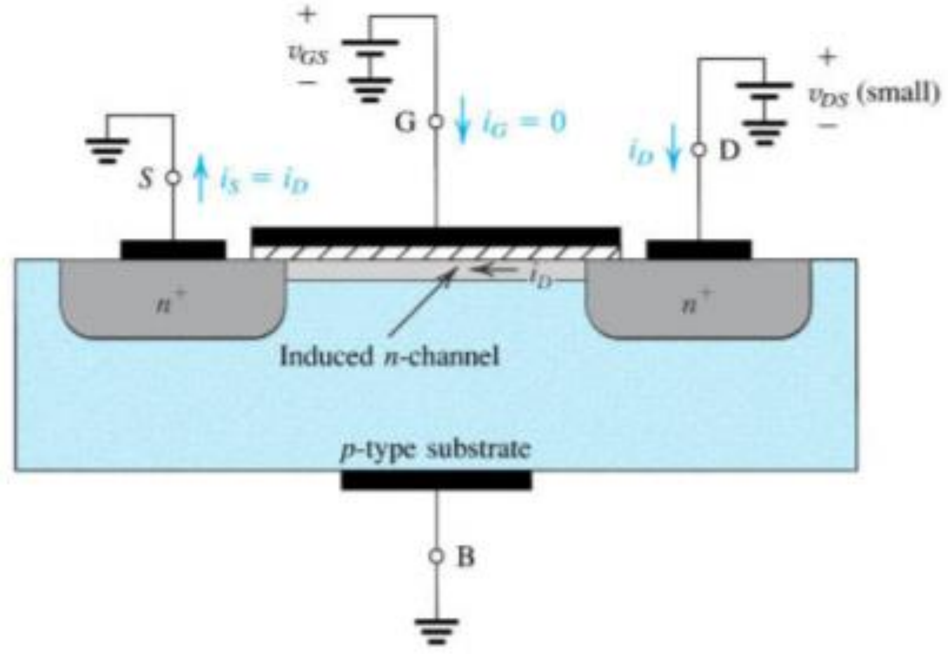


Figure 5: Illustration of the triode operation region on a NMOS transistor with $V_{GS} > V_{th}$ and $V_{DS} > 0$ (Smith et al., 2008).

The saturation region is achieved with a further increment of V_{DS}, see Figure 6. In this operation region, near the drain, the gate-to-substrate voltage is just enough to form a depletion region. Applying a higher drain voltage will cause the reduction of threshold voltage and the channel near the drain terminal will not be formed, occurring pinch-off. After this point, the drain current reaches its saturation and is no more influenced by the drain potential. The existent current flows by drift effect due to the horizontal electric field on the drain terminal that can drag the available minority carriers in the depletion region. To characterize all the operation regions aforementioned, Figure 7 and Table 1 comprises the I_{DS} - V_{DS} output characteristics and the conditions to settle these operation regions.

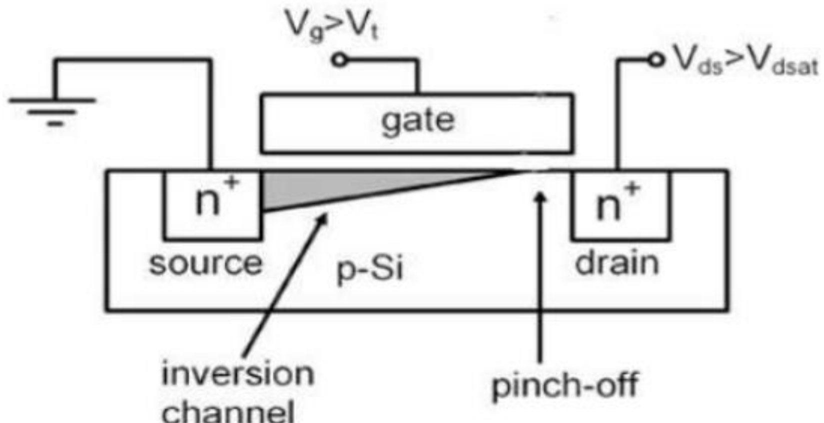


Figure 6: Illustration of NMOS transistor cross-section, and its behavior on saturation region. Presence of a pinch-off point due to the high potential applied on the drain terminal (Bahcall, Kadanoff, Bienenstock, Bahcall, & Condensate, 2005).

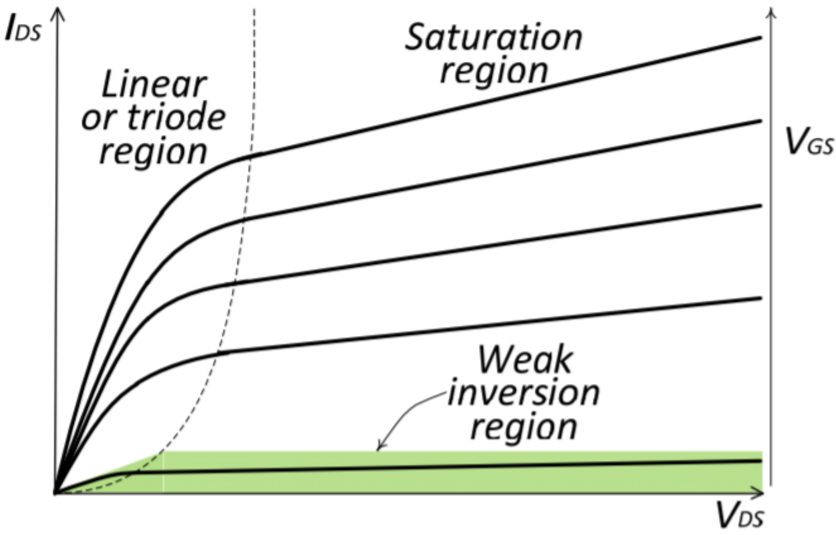


Figure 7: I_{DS} - V_{DS} output characteristics of the different MOSFET operation regions (Ayers & Ayers, 2018).

Table 1: Output characteristics and its bias conditions of the operation region of a NMOS type MOSFET

Region of Operation	Characteristic equation	Bias conditions
Cut-off	$I_{DS} = 0$	$V_{GS} < V_{thn}$
Weak inversion	$I_D = \mu \cdot C_{ox} \cdot (\eta - 1) \cdot W/L \cdot V_T^2 \cdot e^{\frac{V_{GS}-V_{thn}}{\eta \cdot V_T}}$	$V_{GS} \approx V_{thn}$ $V_{DS} > 0$
Linear or triode	$I_D = \mu C_{ox} W/L \left[(V_{GS} - V_{thn})V_{DS} - \frac{V_{DS}^2}{2}\right](1 + \lambda V_{DS})$	$V_{GS} \geq V_{thn}$ $V_{DS} \leq (V_{GS} - V_{thn})$
Saturation	$I_D = \frac{1}{2}\mu C_{ox}\, W/L[(V_{GS} - V_{thn})^2(1 + \lambda V_{DS})$	$V_{GS} > V_{thn}$ $V_{DS} > (V_{GS} - V_{thn})$

2.2 Bipolar Junction Transistor

BJT is a solid-state three-terminal current-controlled device that can be used electronically as a switch (Zhang, 2014). Figure 8 presents the three-terminals of the BJT, such as an emitter, a collector, and a base. A pair of PN Junction Diodes are placed symmetrically to form two different types of BJT (PNP and NPN). The name bipolar is due to the two minority carriers (electrons and holes) involved in the conduction process.

In a bipolar junction transistor, a small current that flows into the base controls the function of the BJT It regulates the amount of current between the collector and emitter terminals (Zhang, 2014). Therefore, unlike the most used transistor in VLSI (MOSFET), the BJT is a current-controlled device.

BJT can be combined with MOSFET to develop innovative circuits. The employed circuit agglomerate the advantages of both technologies. It apprehends the high-input impedance and low-power consumption of the MOSFET and very-high-frequency operation and high-current-driving capability of BJT (Cowles, 2017). The BJT devices are still popular in discrete circuit design. Its performance insensitivity to fabrication variation processes is an interesting approach to very-high-frequency applications (Cowles, 2017).

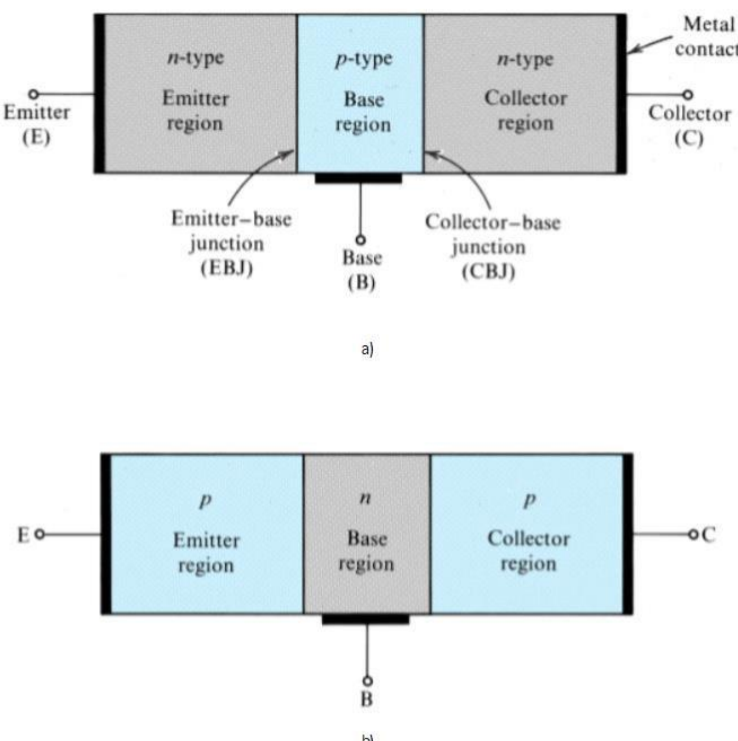


Figure 8: Structure of a Bipolar Junction Transistor: (a) npn transistor, and (b) pnp transistor (Cowles, 2017).

The functional difference between PNP and NPN is the polarity of the junctions during the device operation. The controlling current from the base and the controlled current from the emitter merge in

direction to the collector terminal. Therefore, to have a proper device functionality, as a current regulator, all the currents must flow in the same direction.

As the BJT is a current-controlled device, if the base does not have current, the transistor will act as an open switch. In this state, no current flows through the device. Another operation region is if the potential difference between the base and the emitter is larger than the forward barrier potential of the diode VBE. When the potential difference overcomes the depletion region created by the p-n junction (0.7V for silicon diodes and 0.3V for germanium diodes), a flowing current is measured.

If we apply the opposite polarity, due to electrostatic attraction, both the electrons and the holes will be spread will move away from the junction in which the depletion region will become wider. With the increase of the depletion region, the majority of carriers cannot cross the junction.

As the MOSFET, BJT can be used for several applications, and that depends on which region we are going to use the BJT. As shown in Table 2, there are three operation regions, and each one of them can be used for a specific application.

Table 2: Condition and modes of operation of a bipolar junction transistor.

Operation Region	Conditions	Mode
Cut-off	$V_{BE} < V_{cut-in}$ $V_{CE} > V_{supply}$ $I_B = I_C = 0$	Switch OFF
Linear	$V_{BE} = V_{cut-in}$ $V_{sat} < V_{CE} < V_{supply}$ $I_c = \beta I_B$	Amplification
Saturated	$V_{BE} = V_{cut-in}$ $V_{CE} < V_{sat}$ $I_B > I_{C,max}$ $I_{C,max} > 0$	Switch ON

2.2.1 Different Configurations

There are many possibilities to connect it within an electronic circuit with one terminal being common to both the input and output. In Table 3, different BJT configurations are shown, such as common base, common emitter, and common collector. Their different characteristics are dependent on the circuit configuration attributed to the input signal.

Table 3:Intrinsic characteristics of different bipolar junction transistor configurations.

Characteristics	Common Base	Common Emitter	Common Collector
Input Impedance	Low	Medium	High
Output Impedance	Very High	High	Low
Phase Angle	0°	180°	0°
Voltage Gain	High	Medium	Low
Current Gain	Low	Medium	High
Power Gain	Low	Very High	Medium

2.3 BJT versus MOSFET

As well the MOSFET as the BJT have their unique characteristics, their advantages, and disadvantages. It is difficult to discern which one is better. Their use is highly dependent on the purpose of the circuit. Therefore, it is necessary to understand the circuit requirements, such as power level, drive voltage, switching speed, efficiency, and cost, to come out with an idea about which one is suitable for the situation.

Typically, the MOSFET is more efficient when it comes to power supplies. For battery-powered devices, which the load is variable, and the power supply is limited, in this situation, the usage of BJT is not feasible. On the other side, whenever the circuit powers a load with a predictable current draw, e.g., drive a LED, the use of a BJT would be the best solution, because the base-emitter current can be set to a fraction of the LED current to achieve better efficiency. The MOSFET can be connected easily into large circuits.

In the case of BJT, this does not happen; they require an external resistor, which is unreliable in CMOS technology. It leads to higher power dissipation. In terms of temperature stability, both transistors present a positive TC (On-Semi, 2014). However, the MOSFET has resistor-like properties for smaller VDS values. This attribute provides better stability at higher temperatures, preventing the thermal runaway to occur (On-Semi, 2014). Higher the temperature, the higher is the device impedance, the less current the devices draw. However, since the minority carriers have a significant role on the BJT operation, the BJT is susceptible to thermal runaway (Deshpande, 2007). Last, but not least is the produced noise, the BJT is a bipolar transistor, using electrons and holes as charge carriers, producing higher noise compared to the MOSFET that only has one charge carrier.

Table 4 makes a cluster about the comparison characteristics between the MOSFET and BJT devices.

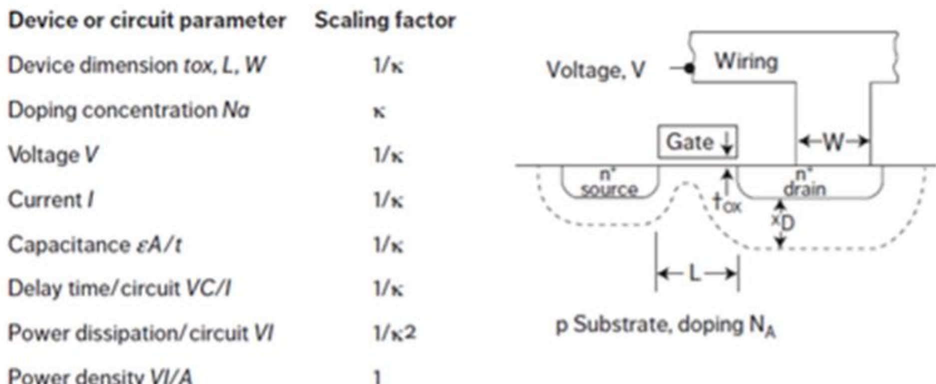
Table 4:Overview comparison between the MOSFET (NMOS) and the BJT (npn).

	NMOS	npn
Voltage Gain	Low	High
Current Gain	High	Low
Input impedance	Very high	Low
Output impedance	High	Low
Noise Level	Low	Medium
Method of control	Voltage	Current
Switching speed	Fast	Medium
Robustness	Easily damaged batic	Robust
Size	Smaller	Larger
Temperature Stability	More	Less
Cost	More expensive than BJT	Cheap
Manufacturer process	Difficult	Simple
Control Method	Input voltage	Input current
Dependence on transistor work	Controlling the depletion region in the channel by reverse bias	Minority carriers injected across the forward voltage in junction
Power Consumption	Less	High
Offset voltage	Absent	Present
Sensitivity	Less	More
	Exhibit properties of a resistor	

2.4 Short-channel MOSFET

The never-ending demand for miniaturization and low power has led to a new dimension in the integrated circuit, the era of deep sub-micron technology and nanotechnology. The continuous shrinking in channel length has posed new challenges such as short-channel effects, high leakage current, and static power dissipation. Some approaches have prevented the escalate dominance of the leakage current, e.g., the insulation material silicon oxide between the gate and the channel changed to minimize the leakage current through those structures (K Roy, Mukhopadhyay, & Mahmoodi-Meimand, 2003). However, due to the decreasing dimensions of the overall transistor structure, other related leakage currents still dominate.

Designing a CMOS circuit above deep sub-micron levels involves a trade-off between chip area, performance, and dynamic power dissipation. Deep sub-micron levels circuit design brings new problems related to short-channel MOSFET, leading to innovative techniques since the planning structure to device fabrication, see Figure 9.



Device or circuit parameter	Scaling factor
Device dimension tox, L, W	$1/\kappa$
Doping concentration Na	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\varepsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

Figure 9: Traditional scaling-down factors on MOSFET parameters (Bohr & Young, 2017).

$$P_{Dynamic} = \alpha \cdot C_L \cdot V_{DD}^2 \cdot f_o \quad (2)$$

$$P_{Static} = I_{Leakage} \cdot V_{DD} \quad (3)$$

$P_{Dynamic}$ is the power dissipation when the circuit is in active mode, from the switching activity of the transistor, by charging and discharging the capacitances (Kim et al., 2003a). P_{Static} is the power lost due to leakage current (Kim et al., 2003a). However, resulting from the continuous scaling of the MOSFET, the deep sub-micron channel length contributes to less area and low capacitance effects. This results in the decrement of dynamic power dissipation. Furthermore, P_{Static} is the off-state leakage, a current that leaks through transistors even in the inactive mode (Kim et al., 2003b).

Static power consumption, shown in equation 3, is a crucial feature to be considered in deep sub-micron chips since its dominance increases with shrinking the technology node. Unfortunately,

smaller geometries exacerbate leakage; therefore, static power begins to dominate the power consumption equation in chip design (Kim et al., 2003b).

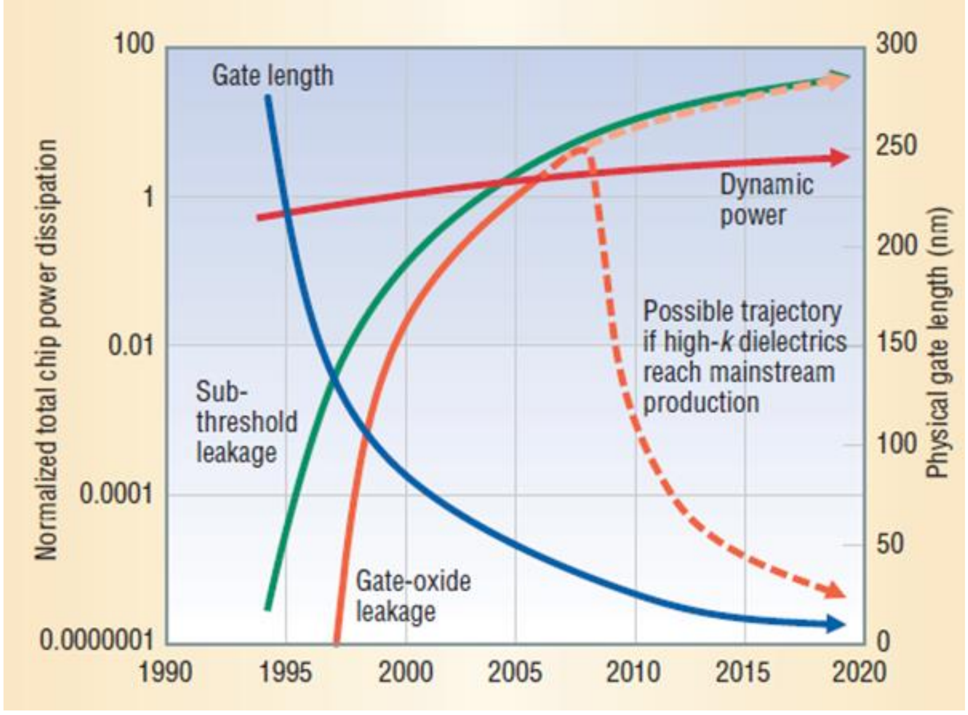


Figure 10: Total chip dynamic and static power dissipation trends based on the International technology Roadmap for Semiconductors. The two power plots for static power represent the 2002 ITRS projections normalized to those for 2001. The dynamic power increase assumes a doubling of on-chip devices every two years (Kim et al., 2003b).

Figure 10 shows exponential increases projected for the two principal components of static power consumption, the subthreshold leakage, and the gate leakage. The subthreshold leakage is related to the weak inversion current across the device. The gate leakage is associated with the tunneling current through the gate oxide insulation. As the CMOS technology evolves, the total power from leakage it is approaching the dynamic power. For technology below 65 nm channel size, the off-state subthreshold leakage exceeds the total dynamic power consumption (Kim et al., 2003a). As leakage current becomes the major contributor to power consumption, the industry must reconsider the power equation that limits system performance, chip size, and cost.

2.5 Short-channel effects

The off-state leakage in long-channel devices is dominated by drain-well and well-substrate reverse-bias PN junctions. The short-channel transistors have the same leakage sources as the long-channel MOSFET. However, with the downscaling of the channel dimension, other leakage mechanisms appear.

Design VLSI with a deep submicrometric transistor is necessary to understand these peculiar leakage sources due to small geometries. In short-channel MOSFETs, the off-state current depends on the threshold voltage, physical channel dimensions, channel/surface doping profile, drain/source junction depth, gate oxide thickness, the voltage supply, the drain voltage, and the gate voltages.

Figure 11 shows the existent leakage currents, I2, I3, I4, and I5 are off-state leakage mechanisms, while I1 and I7 occur in both ON and OFF states. I4 arises in the OFF state but typically appear during the transistor bias states in transition (K Roy et al., 2003).

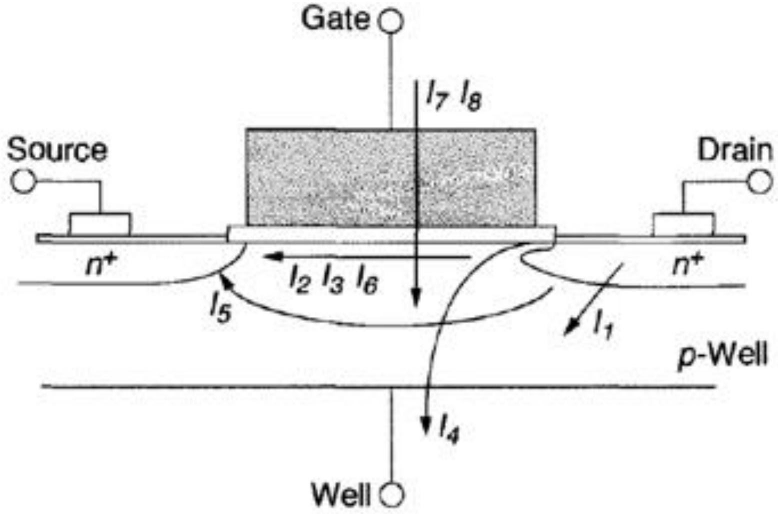


Figure 11: Leakage mechanisms in short-channel transistors (Rahmat bin Sanudin, 2005).

2.5.1 PN Reverse-Bias Current (I1)

When a semiconductor device is reverse biased, it should not conduct any current. Due to the increased barrier potential, the free electrons on the p side are dragged towards the positive terminal. In contrast, holes on the n side are pulled to the negative terminal, producing a current of minority charge carriers. Therefore, its magnitude is very small.

Drain and source to well junctions are typically reverse biased, causing PN junction leakage current (K Roy et al., 2003). Reverse-bias PN junction exists due to minority carriers drift near the depletion region, also, due to electron-hole pair generation in the depletion region of the reverse-bias junction (K Roy et al., 2003), (Kaushik Roy & Prasad, 2000), (Keshavarzi, Roy, & Hawkins, 1997).

2.5.2 Weak Inversion (I2)

Weak inversion or subthreshold conduction current between the source and drain in a MOS transistor occurs when the gate voltage is below the threshold voltage. As shown in Figure 12, the weak inversion is represented as the linear portion of the curve. The carrier virtually does not have an electric field. Therefore, the carriers displace by diffusion along the surface similar to charge transport across the base of bipolar transistors (Keshavarzi et al., 1997). Weak inversion dominates in modern devices off-state leakage due to the downscaling of the threshold voltage (Keshavarzi et al., 1997), (K Roy et al., 2003).

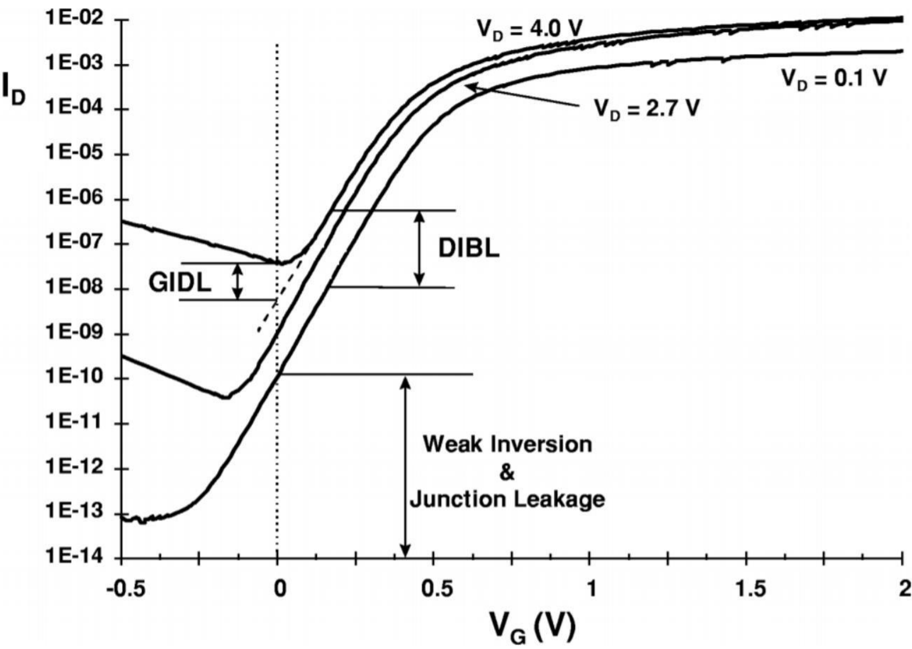


Figure 12: I_D versus V_G NMOS characteristics. Visualization of the different short-channel leakage current, such as GIDL, DIBL, weak inversion and junction leakage (K Roy et al., 2003).

Figure 13 shows the variation of minority carrier concentration along the length of the channel for an NMOS biased in the weak inversion region. Considered that the source of the n-channel MOSFET is grounded, and the $V_{GS}<V_{th}$, and the drain to source voltage $V_{DS}\geq 0.1V$. For such a situation, a weak inversion region is formed, V_{DS} drops almost entirely across the PN reverse-bias junction between the substrate and drain. Therefore, exists a small electrostatic potential variation across the channel, and due to the small number of minority carriers (weak inversion region) and the small electric field. The drift current component, as a result of the charged particle motion in response to an electric field, is negligible (K Roy et al., 2003). Unlike the strong inversion region, which the drift conduction current dominates, in the weak inversion is dominated by diffusion current, which the charged particles tend to spread out or redistribute from areas of high concentration to areas of low concentration (Doolittle, n.d.).

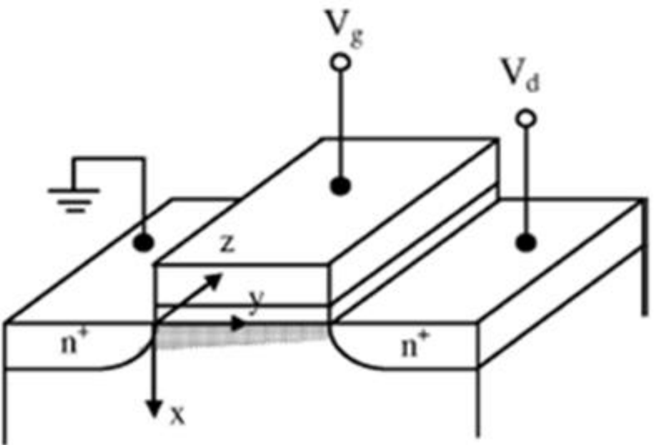


Figure 13: Variation of the depletion region underneath the gate, resulted from the different minority carrier concentration whenever the channel of the MOSFET is biased in weak inversion (K Roy et al., 2003).

2.5.3 Drain-Induced Barrier Lowering (I3)

As the minimum feature size of the MOSFET device reaches the sub-micron level, the DIBL effect is increasingly prominently. Improperly down-scaling of channel length and inefficient channel doping contributes to a significant undesirable field penetration among source and drain.

This unwanted electrostatic interaction leads to a punch-through leakage between the source and the drain. When it occurs, the gate channel loses control of the drain current entirely, being now also influenced by the drain potential. Due to the reduction of the channel's length and the voltage across the drain to source is increased, the drain depletion region moves closer to the source depletion, resulting in field penetration.

As shown in Figure 14, the DIBL is the effect on the output conductance, resulting in a diminishing the potential barrier of the source. It provokes a threshold voltage decrement, increasing the injection of electrons by the source over the minimized potential barrier (Qu, Zhang, Xu, & Qin, 2011).

The DIBL effect causes the threshold variation with drain voltage. The applied drain voltage controls the inversion layer at the drain competing with the gate voltage. With the lowering of the potential barrier due to the increment of drain voltage, a current flow (leakage current) exists. Higher the potential applied to the drain and as the channel length shrinks, the leakage current rises, and the gate can no longer turn OFF the device.

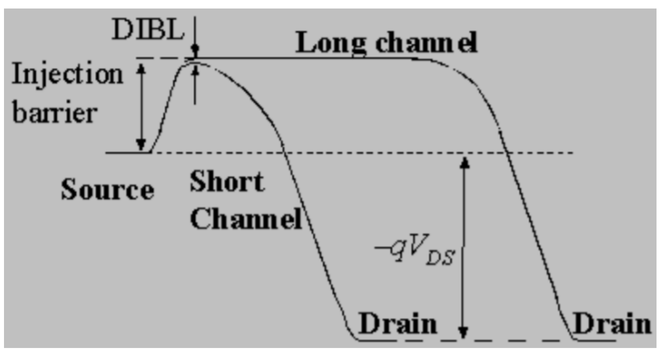


Figure 14: Difference of the potential barrier of the electrons in short and long channel MOSFET, and its influence on the variation of drain potential (Tonk, 2016).

Figure 15 presents the lateral shift of the threshold voltage due to the variation of the drain voltage. The threshold voltage variation is measured as a lateral shift of the transfer curves in the subthreshold region. To overcome this undesirable shift is necessary a proper scale of the depths on the drain and source, and an increased substrate doping density need to be considered.

The height of this barrier is a result of a balance between drift and diffusion current between these two regions. If a high drain voltage is applied, the barrier height decreases, leading to an increment of drain current. This parasitic effect provokes the threshold voltage reduction depending on the drain voltage (Stockinger, 2000).

The result of DIBL is an increase in the residual leakage current in short channel devices as the drain to source voltage is increased. The current increases exponentially with drain bias. The potential barrier between the source and the channel is lowered by the drain bias, for the short channel MOSFET.

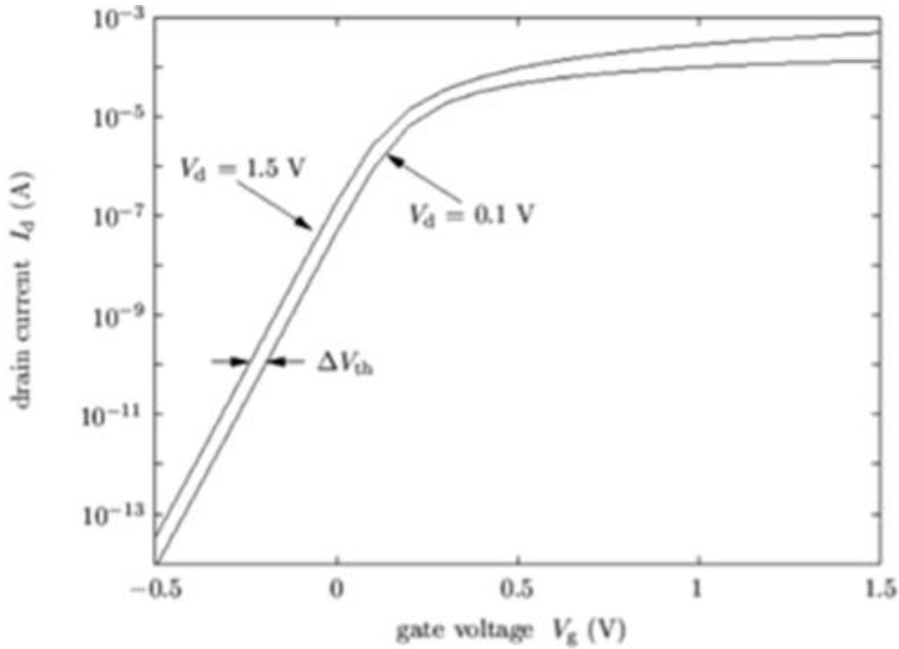


Figure 15: Threshold voltage shift of a MOSFET device for drain voltages of 0.1V and 1.5V in linear and saturation regions (Stockinger, 2000).

2.5.4 Gate Induced Drain Leakage (I4)

In deep-sub-micron MOSFET, doping concentration becomes higher, and the junction profile is more abrupt, causing a high electric field in the devices. This drain leakage current is caused by the gate-induced high electric field in the gate-to-drain overlap region and can dominate the drain leakage current at zero gate bias in thin oxide MOSFET, see Figure 16. A large component of off-stat leakage current is GIDL current. The leakage current is related to the parasitic band-to-band tunneling effect in the electric field present in the drain-subtract junction region underneath the gate (Teherani, 2010), (Chan, Chen, Ko, & Hu, 1987), (X. Yuan et al., 2007). It forces the overlap of substrate energy-band near the interface between the substrate and the gate dielectric. It induces the minority carriers to commute from the valence-band towards the conduction band (Y. K. Choi, Ha, King, & Bokor, 2003).

GIDL is the current that escapes from the thin gate oxide in MOSFET at drain voltages that are extremely small and much less than junction breakdown voltages. It occurs when the V_{DG} potential and band bending are high enough to generate electron/hole pair by valence to conduction band tunneling. The use of doping facilitates the flow of electrons through the MOSFET, the main doping profile is p-type and n-type silicon and the electrons pass through them using tunneling. The electrons escape through band-to-band tunneling due to the very thin gate oxide of the transistor causes the parasitic GIDL current. Concerning Moore's Law (Moore, 2006), the channel length of the transistors and the mass of the dielectric are decreasing. Therefore, band-to-band tunneling increases, causing GIDL to increase as well.

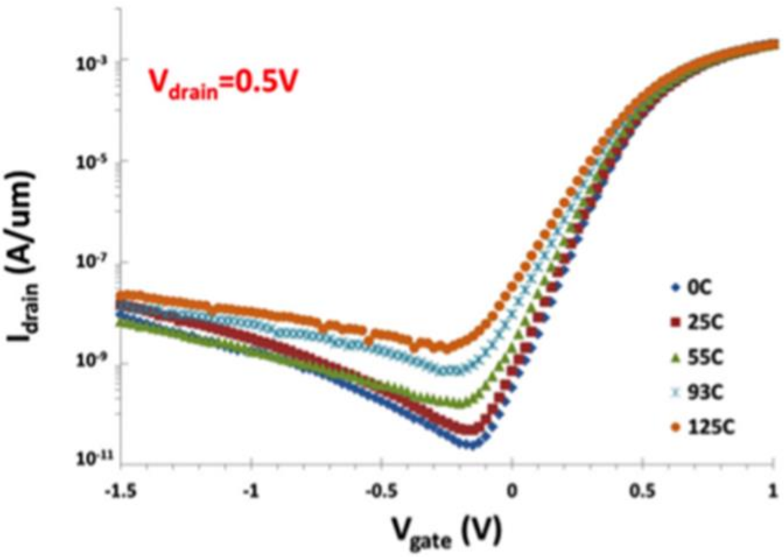


Figure 16: Influence of the electric field from the gate and temperature dependence associated with gate induced drain leakage (Alnuaimi, Nayfeh, & Koldyaev, 2013).

2.5.5 Punch-through (I5)

In short-channel transistors, the proximity of the drain and the source leads to the extension of their depletion region towards the channel. As the existence of downscaling the channel length, the separation between the depletion regions boundaries decrease. An increase in the reverse bias across the junctions with the drain-to-source voltage pushes, even more, the depletion towards each other, establishing a punch-through region that consists of the contact of the depletion boundaries into a single depletion region, see Figure 17(Kaushik Roy & Prasad, 2000),(K Roy et al., 2003). The punch-through phenomenon in a short-channel MOSFET under subthreshold conditions is determined by the DIBL effect, because of the diffusion component is the mainly responsible for punch-through current (Zhu, Martin, & Chen, 1988),(Taylor, 1978).

Any increase in the V_{DS} voltage beyond the punch-through, a lowering of the potential energy barrier occurs. There exists an increment of carriers with enough energy to overcome the potential barrier(Kaushik Roy & Prasad, 2000). Thus, it leads to an increment of subthreshold current. Therefore, the punch-through effect results in an increment of leakage current, derivative on an electric field underneath the gate strongly dependent on the drain-source voltage. Punch-through causes a rapidly increasing current with increasing drain-source voltage (Van Zeghbroeck, 2011). It can be decreased by having higher doping levels either in the substrate or near-source and drain.

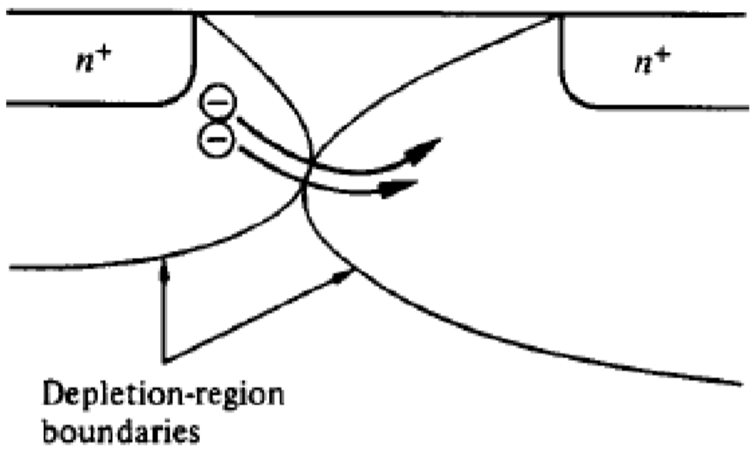


Figure 17: Illustration of depletion region resulted in punch-through leakage current (Tonk, 2016).

2.5.6 Narrow Width Effect (I6)

Similarly, as the channel width becomes narrows, the gate-induced depletion region, which results from the fringing field at the gate oxide edge LOCOS, spreads outside the channel width towards under the isolation. It causes a reduction in depletion layer charge per unit width. This reduction requires high gate voltage to induce a strong inversion layer (channel) at the surface (S. Chen & Shu, 2012). For NMOS transistors, the threshold voltage decreases for effective channel widths under 0.5μm, the narrow width effect in LOCOS isolated devices exhibit an increment of threshold voltage as the channel width decreases (Fung, Chan, & Ko, 1997). On the other side, PMOS transistors have complex behavior, exists a reduction of the threshold voltage till 0.4μm. However, below that channel width value, exists a sharp increase.

2.5.7 Gate Oxide Tunneling (I7)

For conventional CMOS devices, as the continuous down-scaling concerning the transistor size proceeds, the reduction of the gate oxide thickness leads to an increment of the electric field across the oxide (K Roy et al., 2003),(Stockinger, 2000). High electric field coupled with very thin gate oxide, results in tunneling of electrons from the substrate to gate, and vice-versa as subthreshold leakage current. Therefore, for short-channel MOSFET, the gate cannot be considered an ideal insulated electrode anymore (Stockinger, 2000). The leakage current that can flow from the channel to the gate comes into the order of the subthreshold leakage current, and the gate cannot be considered as an ideally insulated electrode anymore. It affects the circuit functionality and contributes significantly to the standby power consumption due to the off-state gate leakage current (C.-H. Choi, Nam, Yu, & Dutton, 2001). For dynamic logic concepts, the gate leakage drastically reduces the maximum clock cycle time (N. Wang, 1989).

2.5.8 Hot Carrier Injection (I8)

Physical degradation on semiconductor devices has a significant impact on the electrical performance of the circuit (Lahbib, Doukkali, Martin, Imbert, & Raoulx, 2015),(Kuphaldt, n.d.). Hot carriers refer to electrons or holes, which due to the rise of the electric field near the Si-SiO_2 interface, gained high kinetic energy enough to overcome the potential barrier, causing reliability problems, damaging Si-SiO_2 interface or oxide trapping (Entner, 2007),(K Roy et al., 2003). The injection from Si to SiO_2 interface is more likely for electrons rather than holes. The electrons have lower effective mass and potential barrier than holes (Khanna, 2016). Due to the high intrinsic energy, hot carriers may migrate into and roam around the forbidden areas of the device, causing degradation of the current drive capability, instability, and eventually failure of the device (Lahbib et al., 2015). These trapped charges shift some performance characteristics of the device itself, such as threshold voltage, transconductance, and drain current (Lahbib et al., 2015).

The hot electron effect can be decreased with the minimization of the electric field across the drain-channel junction. Therefore, the doping concentration at the reverse-biased drain-channel junction needs to be reduced. The Lightly Doped Drain uses two doping levels, with light doping in the source and drain region adjacent to the channel and heavy doping in the most source and drain areas. This process increases the depletion width, reducing the electric field and the hot carrier injection into the oxide (Faculty of NPTEL, n.d.).

2.6 Leakage current reduction techniques

Low power consumption in high-performance VLSI circuits is a highly desirable aspect as it directly relates to battery life, reliability, packaging, and heat removal costs. Nowadays, the leakage current is a great component of the total power consumption in CMOS circuits. The voltage supply needed to be scaled to overcome the dynamic power and reliability issues. To maintain an acceptable level of circuit performance, the threshold voltage also needs to be scaled. This reduction resulted in an exponential rise in the subthreshold current to a certain level that now it is comparable to the dynamic power consumption (Lahbib et al., 2015).(Patel & Patel, 2014). Scaling the voltage supply reduces the dynamic power consumption, but also degrades the performance of the circuit. Therefore, it is necessary to understand some existent approaches to minimize and estimate this undesirable current in both active and standby modes of operation (Amit Agarwal, Kim, Mukhopadhyay, & Roy, 2004).

Standby-leakage reduction techniques put the entire system in low-leakage mode whenever the system is not active. Active-leakage reduction techniques slow down the system by dynamically changing the threshold voltage to reduce the leakage current (A Agarwal, Mukhopadhyay, Raychowdhury, Roy, & Kim, 2006). Many techniques have been proposed to achieve leakage power reduction. Design time requires the modification of process technology. It achieves leakage power reduction within the fabrication/design stage (Duarte, Tsai, Vijaykrishnan, & Irwin, 2002). The other is called run-time technique; it is based on circuit-level optimization schemes that require structural support, and sometimes, technology support.

2.6.1 Multi-threshold voltage designs

Multi-Threshold CMOS technologies, which provide both high- and low-threshold transistors in a single chip, can be used to minimize the subthreshold leakage current. The high-threshold transistors can suppress the subthreshold leakage current, while the low-threshold transistors are used to achieve high-performance (K Roy et al., 2003).

Varying different parameters at the time of fabrication process can achieve different values for threshold voltage, such as channel doping profile, increasing channel length, changing the body bias, thicker gate oxide, as possible to visualize in Figure 18 (a), (b), and (c), respectively.

The goal of using a dual-threshold technique is to achieve higher performance while decreasing the leakage current, during both standby and active modes, without additional circuits, delay, and area overhead. The high V_{th} transistors are used on non-critical paths to decrease the amount of leakage

current, while the performance maintenance is reached with low-V_{th} CMOS circuits in critical paths of the circuitry.

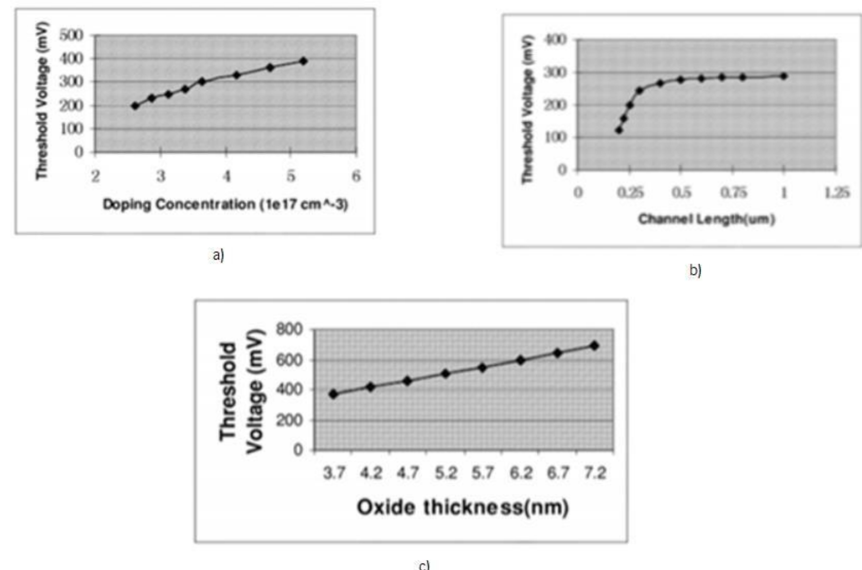


Figure 18: Parameters in the fabrication process that influence the threshold voltage, (a) different channel doping profiles, (b) variation on channel length, (c) oxide thickness (K Roy et al., 2003).

2.6.2 Voltage Supply Scalling

Voltage supply scaling was originally developed for dynamic power reduction. It is an effective method due to the quadratic dependence of the switching power on the voltage supply. Also, voltage supply scaling provides leakage power savings; scaling this parameter helps to reduce the subthreshold leakage current since the DIBL decreases with down-scaling of the voltage supply.

2.6.3 Transistor Stacking

Series connected devices, or stacked devices, have lower leakage than the sum of the leakage for each device taken in isolation. In a stack with two transistors, a slight reverse bias between the gate and source occurs in the pull-up transistor when both transistors are turned off (Butzen & Ribas, 2007). This approach presents some disadvantages, such as performance degradation and higher dynamic power consumption (K Roy et al., 2003),(Patel & Patel, 2014).

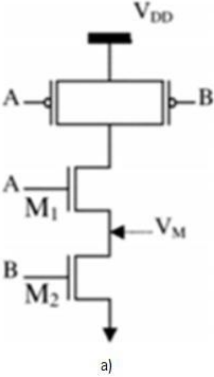


Figure 19: Transistor stack effect, (a) Stacking effect in two-input NAND gate (K Roy et al., 2003), (b) Subthreshold leakage current in different stacks of off-transistors (Dilip, Prasad, & Bhavani, 2012).

Subthreshold leakage current flowing through a stack of series-connected transistors reduces when more than one transistor in the stack is turned off (Butzen & Ribas, 2007). The leakage of a two-transistor stack in order of magnitude less than the leakage in a single transistor, see Figure 19 (b). As shown in the Figure 19 (a), if the NMOS M_1 and M_2 are OFF, the voltage V_M will be slightly positive due the ON state of the A, B PMOS transistors and a small current flowing through the drain. This positive source potential created by the transistor stacking not only will turn the potential between the gate and source negative. Nevertheless, also, the body to source potential will become negative, and therefore the threshold voltage will raise. Last but, not least, the drain to source potential will decrease, which provokes less DIBL and therefore an increment on the threshold voltage. All these aspects related to the transistor stacking lead to a decrement of the subthreshold current (K Roy et al., 2003).

2.7 Reference Circuit

Voltage and current reference circuits are essential building blocks for analog, digital, and mixed-signal circuit systems. Many circuits or electronic devices, from MOSFET to operational amplifiers, depend on a DC operating point to properly function. This operation point is normally established and maintained through a reference circuit. DC biasing is an important feature since some individual blocks require a stable operational point.

As analog circuits are the interface for digital systems, the use of current and voltage references is essential for their proper behavior. It can set a bias point directly or can also be used to compare signals with a known value. With the need to achieve progressively lower power consumption, these low-power CMOS circuits are trying to follow these electronic demands. Within a VLSI, which is the case of the power management circuit, achieving low power to maximize efficiency is necessary, and those low-power circuits can be polarized with current references.

In different research related to this field, there has been a focus on understanding the PVT conditions that do the references deviate. Although many novel references almost do not have temperature variations. However, as we approach the down-scaling limit of the MOSFET, power consumption has another heavy component related to the leakage current in the subthreshold region that can violate the behavior of the CMOS device. These new reference circuits achieve the constant voltage or current depending on the intrinsic characteristics of the MOSFET device. It combines the intrinsic characteristics dependent on temperature to achieve the maximum accuracy to properly bias electronic circuits.

In CMOS technology, several performance parameters, such as stability, and reliability change continuously within a transistor under different PVT conditions. Therefore, the following research attempts to understand these problems, to develop reference circuits, such as current and voltage accurate under different PVT conditions.

The following subsection will focus on a better perception of the state-of-art of those circuits, from the basic towards the most recent. Understanding their behavior and how they achieve their results is crucial to develop a new reference circuit. As some of the restrictions set by this research project are low power consumption and low area, some of the state-of-art research does not fit these requirements. With the emergence of subthreshold leakage current, the researchers focus even more on how to use this leakage current, as shown in Figure 10, the leakage power is overcoming the dynamic power. Therefore, it is essential to change the point of view relative to this type of current, and not see them as leakage but as the main operational current to turn-up devices.

2.7.1 Voltage Reference

A voltage reference with a low-power operation and a small area is required to achieve the desirable milestones of the research project. Therefore, modified voltage reference circuits without bipolar transistors and resistors are required. In CMOS process, there exists a difficulty to fabricate resistors with controlled values or with a reasonable physical size, and modern CMOS processes can only guarantee accuracy on-chip resistors to only with ±25% (N, B P, Anjum, & K A, 2014),(Fayed & Ismail, 2006). Figure 20 shows a layout example during the thesis work and the CMOS area comparison between the CMOS resistor and CMOS transistors.

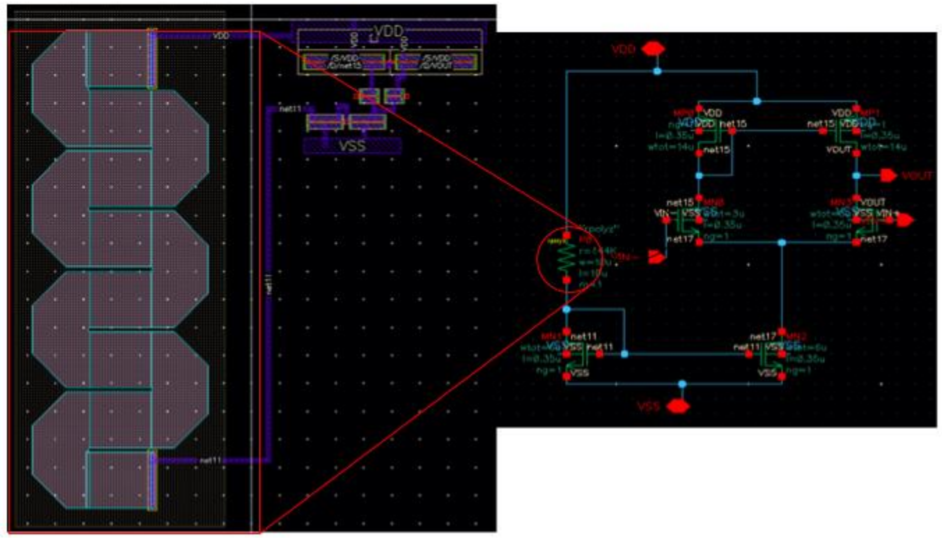


Figure 20: CMOS schematic and layout, in the layout view, the component with the red rectangle is the CMOS resistor. It is possible to observe the difference of occupied area between the CMOS resistor and transistors.

Since VLSI chips require voltage reference circuits to provide precise and stable voltage signals, the traditional BGR is the most commonly used, due to their high accuracy. These circuits have been implemented in standard CMOS technology exploiting parasitic vertical BJT. Their use relies on the negative TC of the bipolar device to neutralize the positive TC of the voltage difference between NPN junction (C. Chen & Wu, 2016). The BGR circuit generates a temperature-independent reference voltage of 1.2V with a voltage supply higher than 1.4V. To keep up the power demands, the voltage supply must be reduced, and in some applications, the required voltage supply is below the forward-biased PN junction voltage of the bipolar device. Therefore, the traditional bipolar bandgap reference and the BJT itself are no longer suitable for the new power demands (C. Chen & Wu, 2016),(B. Do Yang, 2014). Table 4 gives an overview of the characteristics of this device. A possible technique to overcome this problem is to rely on NMOS transistor biased in the subthreshold region since this region exhibits an exponential I-V behavior

resembling the BJT characteristics. Therefore, to achieve low-power voltage reference circuits, their operation consists in strong inversion and subthreshold regions of MOSFET.

2.7.1.1 Voltage reference operating in strong inversion MOSFETs

The proposed circuit by (De Vita, Iannaccone, & Andreani, 2006), as shown in Figure 21, consists of a voltage reference generation with strong inversion MOSFET (M3-M8) and subthreshold MOSFET (M1, M2). The M1-M4 transistors form a close loop that generates a bias current I_o.

The bias current is produced through a current mirror between M6 and the upmost MOSFET in the active load stage receives the current. The MOSFETs M7-M10 generates the output reference voltage. In this circuit, the gate-source voltages for the MOSFET that generates the reference voltage form a closed loop. Therefore, the generated output reference voltage is shown in equation 4.

The temperature independence can be achieved by adjusting the size of the involved transistors because the threshold voltage presents a positive temperature coefficient and the thermal voltage a negative TC (De Vita et al., 2006). To achieve an optimal TC, most of the bias current must flow through M7 and M8 rather than M9 and M10.

$$V_{Ref} = V_{th} + \left[\frac{1}{\sqrt{k_8}}\left(1 + \sqrt{\frac{\frac{W_{10}}{L_{10}}}{\frac{W_9}{L_9}}}\right) - \frac{1}{\sqrt{k_7}}\right]\sqrt{2I_o} \qquad 4$$

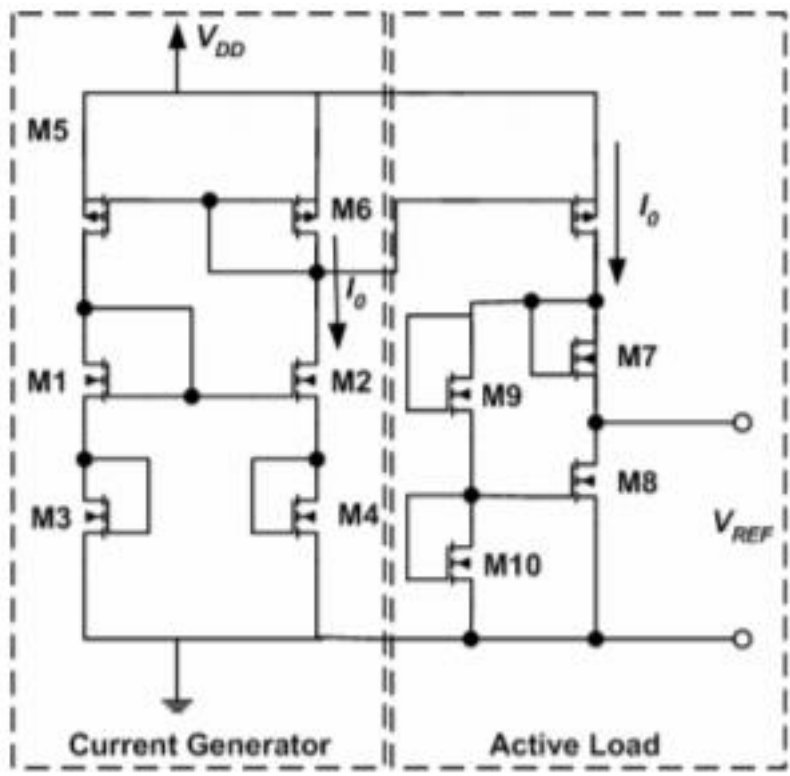


Figure 21: Voltage reference consisting of M_3-M_8 operating in strong inversion region, and M_1 and M_2 operating in subthreshold region (De Vita et al., 2006).

2.7.1.2 Voltage reference operating in subthreshold inversion MOSFETs

The voltage reference circuit proposed by (De Vita & Iannaccone, 2007), consists of using two different threshold voltage devices, as is possible to observe in Figure 22. The transistors M_1 and M_3 are high V_{th} devices operating in the subthreshold region, and M_2 and M_4 operating in a strong inversion region.

This technique of using two different threshold voltage is one technique to decrease the subthreshold leakage current in the short channel. As mentioned in Section 2.6.1, higher threshold MOSFETs can suppress more the leakage current during the standby and active modes. While the lower threshold MOSFETs are designed to achieve higher performance. The core of this circuit is that the two different threshold voltage devices share the same V_{GS}, and the basis for expressing the current generated relies on this statement.

The current generated, through a current mirror between M_8 and M_9, flows to the active load. The transistor M_{10} receives the mirrored current and produces a constant output voltage, that can be given by equation 5.

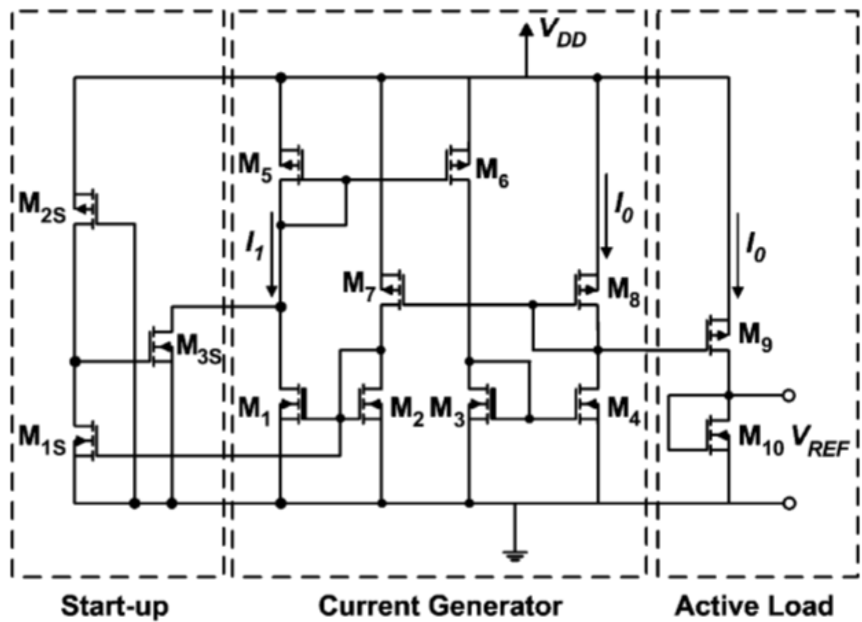


Figure 22: Voltage reference circuit operated in the strong inversion and subthreshold regions using high- V_{th} devices (De Vita & Iannaccone, 2007)

$$V_{ref} = V_{th} + \sqrt{\frac{2I_2}{k_{10}\beta}} = V_{th} + \eta V_T ln\,(\frac{K_3}{K_1})\frac{\sqrt{K_4/K_{10}}}{\sqrt{K_4/K_2} - 1} \quad 5$$

Relative to the temperature dependence, equation 5, represents some parameters that are influenced by the temperature, such as, the threshold voltage (V_{th}), and the thermal voltage (V_T). As these two temperature-dependent parameters have different TC, the V_{th} has a negative TC, and V_T has a positive TC. Therefore, to reach output voltage independent from the temperature, it is necessary to adjust the size of the transistors (De Vita & Iannaccone, 2007).

2.7.1.3 Voltage reference consisting of subthreshold inversion MOSFETs

Figure 23 shows a voltage reference circuit proposed by (Ken Ueno, Hirose, Asai, & Amemiya, 2009). The current source sub circuits consist of a modified ß multiplier self-biasing circuit using a MOS resistor M_{R1} substituting a normal resistor. All the MOSFET except the MOS resistor operates in the subthreshold region, M_{R1} is operated in the deep-triode region.

The first subcircuit generates a current I_P, and through PMOS current mirrors, it injects the produced current into a bias voltage sub-circuit to produce a reference voltage. The MOSFET M_3- M_7 and M_{R1} form a close loop, as shown in equation 6.

The circuit produces two voltages with opposite TC, where one refers to the threshold voltage and the other to a multiple of thermal voltage, these voltages are merged to produce an output reference voltage with a zero TC (Ken Ueno et al., 2009).

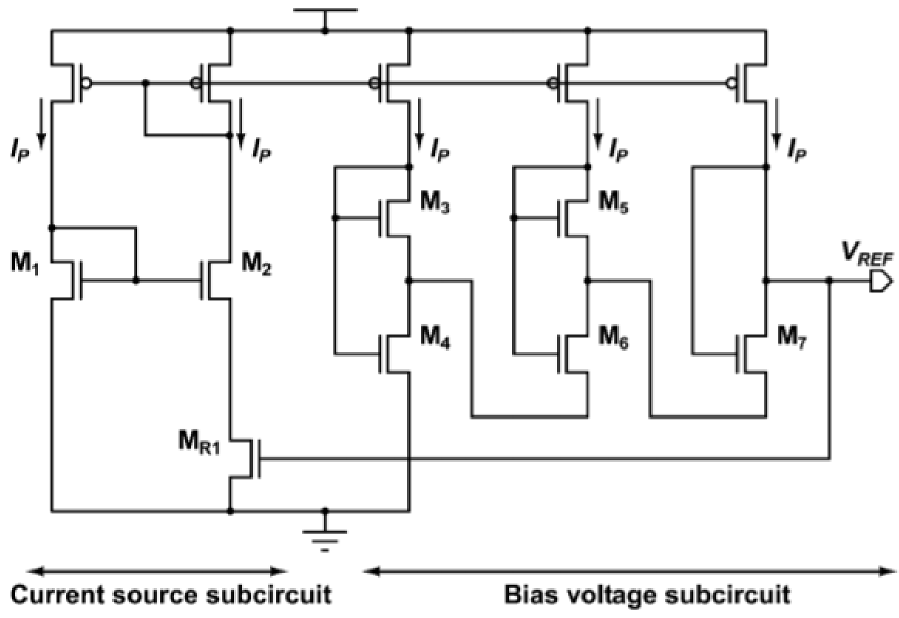


Figure 23: Voltage reference consisting on all MOSFET operated in subthreshold region, except for M_{R1}, which operates in triode region (Ken Ueno et al., 2009).

$$V_{REF} = V_{GS4} - V_{GS3} + V_{GS6} - V_{GS5} + V_{GS7} \quad 6$$

$$V_{REF} = V_{th} + \eta V_T \, ln\left(\frac{3I_P}{K_4 I_o}\right) + \eta V_T \, ln\left(\frac{2K_3K_5}{K_6K_7}\right) \quad 7$$

Equation 7 shows that the voltage reference is expressed as the sum of the gate-source voltage of transistor M_4 and the thermal voltage of the subthreshold transistors that forms a close loop. By adjusting the sizes of the involved transistor, the temperature coefficient is minimized.

2.7.2 Current reference

Current references that produce a nano ampere current is required more than ever in low-power VLSI. The circuit performance must be kept stable and precise because of the bias current influence the power consumption and the performance of other circuits (if current reference gives bias). Therefore, in the following subsection, it is provided with an overview of the state-of-art of nano ampere current reference circuits.

2.7.2.1 Current reference based on self-biasing without resistors

The circuit on Figure 24 consists of a modified ß multiplier self-biasing circuit using a MOS resistor instead of a normal resistance (Oguey & Aebischer, 1997). The gate-source voltage of the MOS resistor M_3 is determined by the diode-connected transistor M_4 operating in saturation region. Therefore, the output current can be expressed by:

$$I_{REF} = \frac{2K_3^2\beta}{K_4}\eta^2 V_T^2 \ln^2(\frac{K_2}{K_1}) \quad 8$$

Applying the partial derivative of current produced w.r.t. temperature (dI_{Ref}/d_T) in equation 8. Two temperature-dependent parameters, such as the thermal voltage and the surface mobility of electrons in the channel are shown. These thermal characteristics do not have opposite temperature behavior. Therefore, the TC of the current will never be zero.

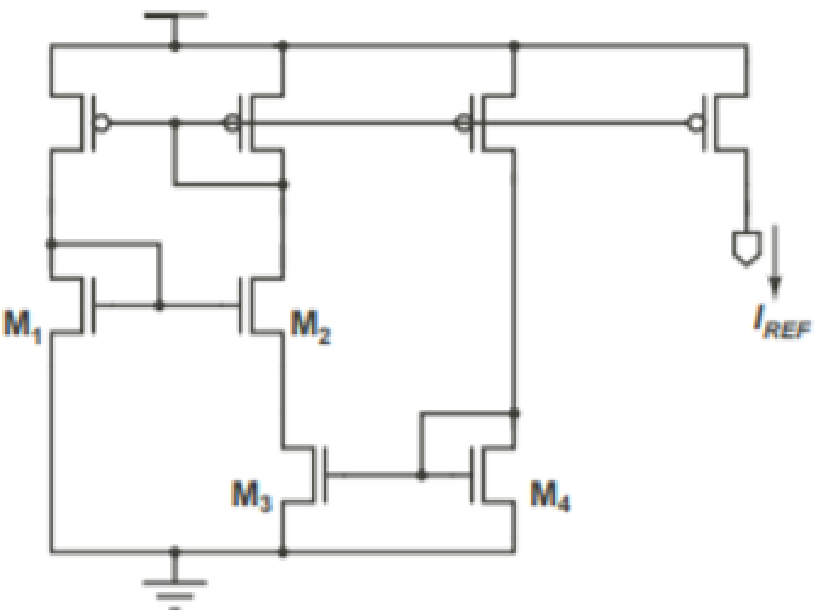


Figure 24: Modified ß multiplier self-biasing circuit without resistors. Transistor M_1 and M_2 operates in subthreshold region, M_3 operates in triode region, and M_4 operates in saturation region (Oguey & Aebischer, 1997).

2.7.2.2 Current Reference consisting of subthreshold MOSFETs

Figure 25 presents a current reference circuit proposed by (K. Ueno, Asai, & Amemiya, 2015) consisting of a bias-voltage sub circuit and a current source sub circuit. Similar to the circuit presented in Section 2.7.2.1, the voltage-source of the MOS resistor M_3 is generated by a diode-connected transistor M_3. The current I_B that flows within bias-voltage sub circuit is determined by the size ration between M_1 and M_2 and the MOS resistor M_3.

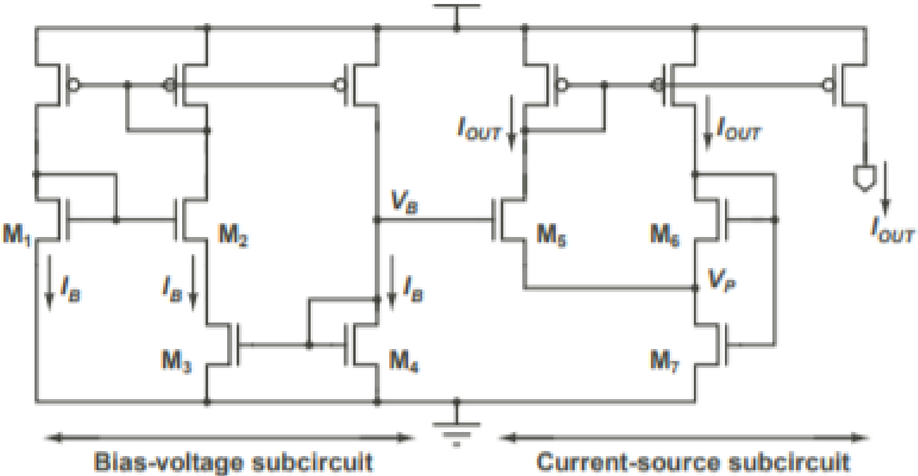


Figure 25: Schematic of a current reference consisting in subthreshold MOSFET, except M_3 which is a MOS resistor, operating in triode region, and M_4 which is a diode-connected transistor, operating in saturation region (K. Ueno et al., 2015).

As the MOS resistor, M_3 and transistor M_4 share the same gate and source, the current that flows through these devices are the same. Therefore, is possible to calculate the parameter V_B, that corresponds to the gate voltage of M_5, equation 9, crucial to calculate the reference current, as possible to observe in equation 10, being ΔV_{th} the difference between the threshold voltages of M_7 and M_6 with M5 and M4, and $I_o = \mu C_{ox} (\eta - 1) V_T^2$ a process-dependent parameter.

$$V_B = V_{th} + \frac{2K_3}{K_4}\eta V_T \ln\left(\frac{K_2}{K_1}\right) \qquad 9$$

$$V_{REF} = V_{th} + \eta V_T\, ln\left(\frac{3I_P}{K_4 I_o}\right) + \eta V_T\, ln\left(\frac{2K_3K_5}{K_6K_7}\right) \qquad 10$$

As ΔV_{th} is insensitive to temperature because the difference of the threshold values of the relevant transistor eliminates the dependence on temperature. Therefore, setting an appropriate ΔV_{th} is the pertinent approach to provide independence on temperature. The value of the threshold voltages can be adjusted by changing the involved transistors sizes (K. Ueno et al., 2015).

2.7.3 Summary reference circuits

This section gives an overview of requirements, implemented in the project report, which gives an understanding of the reference circuits implemented in this report.

Decreasing the voltage supply, as shown in equations 2 and 3 are one of the direct approaches to reduce power consumption. However, along with this drastic reduction, the reduction of the threshold voltage of the CMOS transistors was not very effective. Therefore, it brought a significant challenge to the design of analog circuits under low voltage (C. Chen & Wu, 2016).

As mentioned in Section 2.7.1, the traditional approach is the bandgap voltage reference circuits, but the usage of a BJT is no longer suitable for the new power demands. Therefore, one of the strategies to develop these reference circuits was to substitute it with a diode-connected MOSFET biased in the subthreshold region. The motivation of this choice is the exponential I-V behavior resembling the BJT characteristics. However, an important aspect to keep in mind is although the electrical properties are similar, the subthreshold MOSFET presents other parameters that are dependent on the temperature. Therefore, the literature review of circuits in Sections 2.7.1 and 2.7.2 gives an overview related to the state-of-art of potential approaches that can be implemented.

Resistorless CMOS voltage proposed in (Magnelli, Crupi, Corsonello, Pace, & Iannaccone, 2011),(De Vita & Iannaccone, 2007),(P. Yuan, Wang, Li, Wang, & Liu, 2011),(Cordova et al., 2017) enables nano-watt power operation while saving silicon area. However, this solution uses MOS transistors with different threshold voltages or zero-V_{th} transistors. These different typologies require additional fabrication masks, which are usually not available, and creates extra manufacturing costs (Liu, Zhan, & Wang, 2018).

2.8 Oscillator

The escalating demand for portable devices has highlighted the importance of low-power consumption to enable long time operations for those circuits (Lin, Kaiser, & Pottie, 2004). The increased capabilities of these CMOS devices have led to successfully design and implement RF transceiver building blocks such as LNA, power amplifiers, and local oscillators (Karim, 2013). These local oscillators are used for a wide range of applications varying from keeping track of real-time, setting clock frequency for digital data transmission, and clocking of logic circuits (Van Beek & Puers, 2012).

The goal of the research project is to develop a local oscillator capable of setting a clock time to a digital system to burst the energy accumulated from the energy harvester. For consumer applications, two types of oscillators are distinguished, such as mechanical and electrical oscillators.

Mechanical oscillators consist of a frequency-selective element which is a mechanical resonator made from quartz (Frerking, 1996). Electrical oscillators, the frequency-selective element is integrated on the chip and covers many types of an oscillator such as harmonic and relaxation oscillators. The harmonic oscillators, such as RC, and LC oscillators, the energy flows from the active components to the passive components, and a feedback path pronounces the frequency of output signal.

In the relaxation oscillators, the energy is exchanged between active and passive components; the frequency of the output signal is settled by charging and discharging time-constants. In the case of the implemented oscillator, VCO, the output frequency is controlled by the input voltage. VCO can be implemented in both harmonic and relaxation oscillators, depending on the output form. In the following sections, it will be clarified the reason to choose this type of oscillator.

2.8.1 Important oscillator properties

2.8.1.1 Non-deterministic frequency stability

Ideally, the frequency spectrum of an oscillator should only contain one frequency (J. D. Van Der Tang, 2003). However, any oscillator suffers from short-term frequency fluctuations, expanding the frequency spectrum. This spectrum broadening results in phase-noise or jitter. The short-term fluctuations are induced by non-deterministic noise sources, such as flicker, thermal, and shot noise (Lance, Seal, & Labaar, 1984), (Fundamentals, 2006). These noise sources effect both amplitude and phase of the oscillator (Lance et al., 1984), amplitude fluctuations maybe restoring to the initial state, but phase fluctuations persist indefinitely.

In the developed current starved voltage-controlled oscillator, these sources of noise influence the performance of the periodic signal in long-term stability.

2.8.1.2 Power dissipation

Any oscillator should consume minimum power possible. Nevertheless, the power supply to bias an oscillator is required to achieve enough gain to sustain the oscillation. The signal power of the oscillation needs to be sufficiently high to have a large signal-to-noise ratio, and consequently, a low jitter and phase noise.

The reason to choose the developed oscillator was to decrease even more the power consumption, eliminating the influence of the power supply to bias the oscillator structure. The purpose of the power supply on the developed oscillator is to charge or discharge the output capacitance, defining its amplitude. However, in terms of frequency, the power supply has no influence, because the bias voltage provided by the voltage reference is the circuit which defines the current that flows through the oscillator circuit.

2.8.1.3 Deterministic frequency stability and accuracy

The frequency of the output oscillator signal should be stable or with a low range of frequency variation under different surrounding conditions, such as temperature and voltage supply, or even, fabrication process (Lance et al., 1984). However, this last parameter should be tested upon the finalization of the fabricated chip.

Along with the frequency stability, the frequency also needs to be accurate with a predefined output frequency. The accuracy of a frequency can be limited by manufacturing tolerances.

2.8.1.4 System integration and miniaturization

With advancements in CMOS processes, the possibility to integrate MEMS in CMOS devices, are becoming more and more a viable option. The integration of MEMS mechanical resonators into CMOS processes are becoming a trend, due to their high accuracy and long-term stability, as well as, a better noise ratio compared to electrical oscillators. The components incorporated within these systems should be small and compatible with other high levels of system integration. Moreover, more importantly, it should be viable to integrate with other components aboard.

However, the purpose of this research is to build an oscillator and not develop an oscillator in MEMS technology. Also, the occupied area of a MEMS resonator and an electrical CMOS oscillator is

entirely different, as possible to observe in Table 5. Therefore, due to the reason mention above, an electrical oscillator is chosen to be designed.

2.8.2 Electrical Oscillators

An emerging class of mechanical oscillators is based on MEMS technology. The potential to develop small-sized, high level of integration, and low-cost devices in MEMS open exceptional possibilities for creating miniature-scale precision oscillators. It is expected in terms of performance that mechanical oscillators are superior to electrical oscillators since this type of oscillator results from a mechanical resonance with high-quality Q-factor (Zuo, Van der Spiegel, & Piazza, 2010). However, these promising technologies are crucial to achieving higher system integration as well as better performance. It still lacks compatibility with CMOS technology, increasing its complexity and structure of electronic circuits (Van Beek & Puers, 2012).

It is expected that these two different technologies (MEMS and CMOS) could be compatible since the processes and materials are often CMOS compatible as well as the manufacturing infrastructure. MEMS oscillators will fulfil the gap between high-performance from the non-CMOS compatible oscillators and low-performance CMOS compatible oscillators (Van Beek & Puers, 2012).

Although electrical oscillators cannot meet the electrical performance of mechanical oscillators, the conventional mechanical oscillator is still bulky and cannot be integrated into CMOS technology, without increasing complexity of manufacture cost. These disadvantages make it impossible to be used in any application.

In contrast, the use of electrical oscillators is limited depending on the requirement of the application, their overall performance can be improved attaching them to a mechanical oscillator, but that led to the problem described above. In Table 5, it shows the advantages and disadvantages of both types of oscillators.

Table 5: Advantages (green) and disadvantages (red) of electrical and mechanical oscillators.

Oscillator technology	Accuracy df/f_o (ppm)	Noise	Size $L \times W \times H$ (mm)	Integration level
Mechanical	< 10	~ 130	$> 1.6 \times 1.2 \times 0.35$	Require bulky hermetic packaging Non-CMOS compatible
Electrical	> 100	~ 90	$< 0.5 \times 0.5 \times 0$	Plastic package CMOS design

2.8.2.1 LC Harmonic Oscillator

LC oscillators are arranged using an inductor and a capacitor preserving the energy during the oscillation period. There exist different topologies depending on the arrangement (series or parallel) that the frequency selector and capacitor have in LC oscillators. The resonance frequency of a pure parallel LC resonator is expressed in equation 11.

$$f_{osc} = \frac{1}{2\pi\sqrt{L_S C_S}} \tag{11}$$

As is very rare to find a pure resonator circuit, in practice, the inductor is less effective than the capacitor. It is desirable to achieve a high value of the quality factor. Therefore, in schematics, the inductor L_S is represented with a resistor R_s in series.

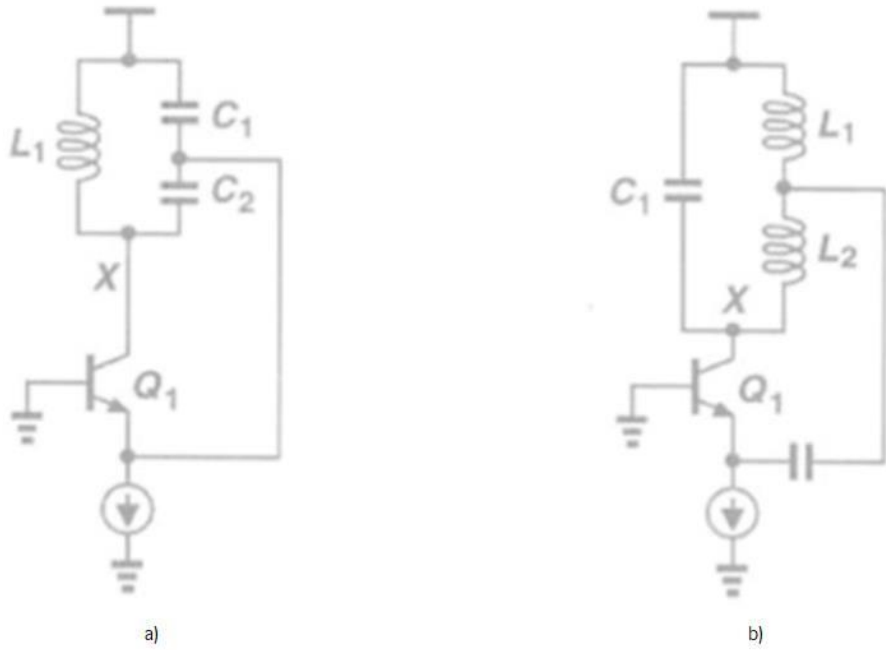


Figure 26: LC-Oscillator configuration, (a) Colpitts, (b) Hartley.

The resonant circuit has three different behaviors depending on the deviation of the oscillation frequency with the resonance frequency. At the resonance frequency, the LC circuit behaves like a resistor and the phase difference between voltage and current drops to zero. When the frequency is less than the resonant frequency, the LC-tank performs as an inductor and a capacitive to higher frequencies that the resonant. The oscillation signal of an LC tank is damped due to the presence of lossy elements. Therefore, to overcome this problem, an active element is added to the circuit.

The two most common LC circuit configurations are the Colpitts and Hartley, see Figure 26 (a) and (b), respectively. These configurations use a transistor as an active device. As shown in Table 3, the common emitter amplifier achieves zero-phase shift between the current and the voltage. The zero-phase shift is reached due to the amplifier configuration that sets a 180° out of phase. The two capacitors in series and parallel with the inductor provide the additional 180° necessary to oscillate. Due to the feedback signal in Hartley configuration, the inductor has a very low Q than the capacitor, occupying a large area in the chip. Therefore, Colpitts is preferred over Hartley.

2.8.2.2 RC Harmonic Oscillator

The usage of the resistor instead of an inductor as the component that controls the frequency does not preserve the energy during the oscillation period, leading to poor spectral purity (J. van der Tang, Kasperkovitz, & Roermund, 2003). Therefore, the RC oscillator has less noise performance compared to

LC oscillators. However, for special high-frequency applications, this type of oscillator can be used due to their easy integration and large tuning range.

Varying the capacitor or the resistor in the RC network varies the resonance frequency produced. If all the passive components in the phase shift network, see Figure 27, are equal. Then, the RC oscillator output frequency is given by equation 12.

$$f_{osc} = \frac{1}{2\pi RC\sqrt{2N}} \tag{12}$$

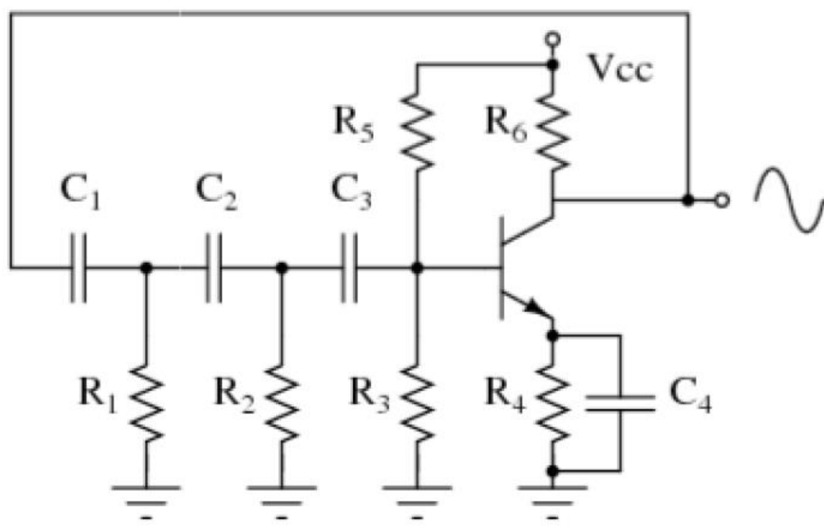


Figure 27: RC oscillator feedback network using a BJT to sustain the circuit (Arim, Lam, & Ordin, 2014).

These oscillators present some limitations, and their usage is limited to low-frequency applications since the phase noise increases with the increment of the number of stages (Odyniec, 2006).

2.8.3 Electrical Relaxation Oscillator

The relaxation oscillator's strength is its natural wide tuning range with a fundamentally linear frequency-control characteristic (Gierkink & Tuij, 2002). The relaxation oscillator presented in Figure 28 consists of a sawtooth output signal waveform with a frequency determined by the charging and discharging of the capacitor. This circuit consists of a comparator with hysteresis, known as Schmitt trigger comparator. It is responsible for sending a signal to a logic block to change the switches. The storage capacitor accumulates energy from the power supply or discharging towards the ground. The accumulated potential is compared with the lower and higher threshold voltages of the Schmitt trigger. Finally, the switches are responsible for charging the capacitor if it is connected to the power supply or discharge if connected to the ground.

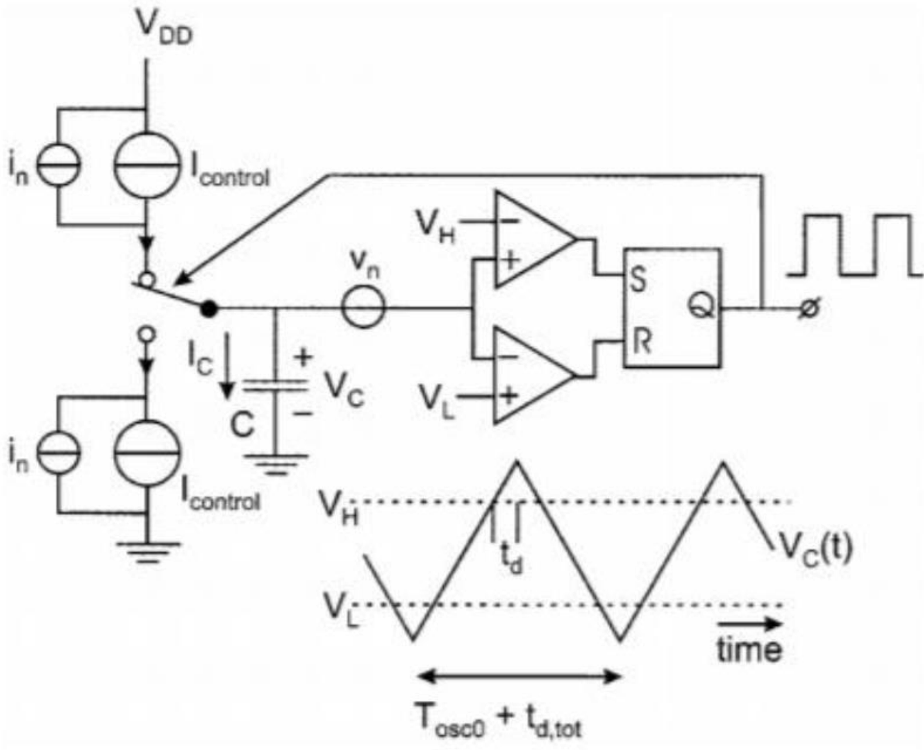


Figure 28: Circuit schematic of a conventional relaxation oscillator and its output waveform (Gierkink & Tuij, 2002).

A VCO is also considered a relaxation oscillator depending on the way they propagate the periodic signal. The circuit implemented in the project report consists of a current-starved VCO. The definition of current-starved results from the restrict current that flows through the delay-stages is dependent on the voltage reference. The voltage reference bias the MOSFET that defines the current through the different delay stages. The reason for the selection and further explanation of this circuit is explained in the following section.

The two notable approaches are LC-tank VCO (LC-VCO), and ring VCO. The LC-VCO is hardly considered because of its fabrication complexity and large area overhead. Also, the non-linearity of LC-VCO to the frequency gain is one of the concerns, degrading the local oscillator performance. The phase noise, as well as its performance, are strongly dependent on the quality factor of the employed inductor. On-chip realization of spiral inductors results in metal conductance losses, skin, and proximity effects. Several techniques were engaged in increasing their quality factor, such as bond-wire inductors, MEMS inductors. Nevertheless, although promising, it brought CMOS process unreliability or high manufacturing costs, along with a large die area (Kumar, Mehra, & Islam, 2019).

On the other hand, Ring VCO has features that surmount the disadvantages related to LC-VCO. It possesses a better integration and a wide tuning-range without using passive elements. Its topology

consists of multiple output phases, where each stage sets a time delay producing a periodic signal due to feedback between the last and first stage.

CHAPTER 3 DEVELOPMENT

According to the specification mentioned in the State of the art, referencing circuits are developed, such as current and voltage reference as well as a current-starved VCO, which uses an original voltage reference to set an output periodic signal.

All the circuits were simulated in Cadence software with proprietary SMIC 130nm CMOS technology. All the necessary steps to perform an ASIC were implemented and shown. It comprises a circuit schematic optimization and simulation, physical layout design, parasitic extraction, validation of the physical layout, integrated circuit fabrication. Further testing and analysis are still an ongoing process.

Extensive research has been done, with all the efforts, focusing on the power consumption reduction and output stability. The focal point was the investigation of deep triode and subthreshold MOSFET, as well as the study of the parameters dependent on temperature. The final layout design was fabricated, the future work of this project comprises the production testing of an integrated circuit, using a 130nm CMOS technology process. The testing part is to show the integrated circuit functionality in real-world applications, as well as the comparison with the simulated results.

3.1 Voltage reference

The development of the voltage reference comprises the knowledge acquired during this research work. Related research work mentioned in Section 2.7.1 gave an understanding of all the involved parameters necessary to perform a voltage reference. Such reference needs to be suitable to bias circuits on the power management circuit chip for energy harvesting applications. The developed circuit generates an appropriate bias voltage to set a correct operation on the circuit which is integrated, such as the voltage peak-detector and the current-starved voltage-controlled oscillator.

This section will explain all the adjacent theories involved in the design of the circuit and the assumption involved to perform a constant output voltage reference, as well as, the discussion of the results.

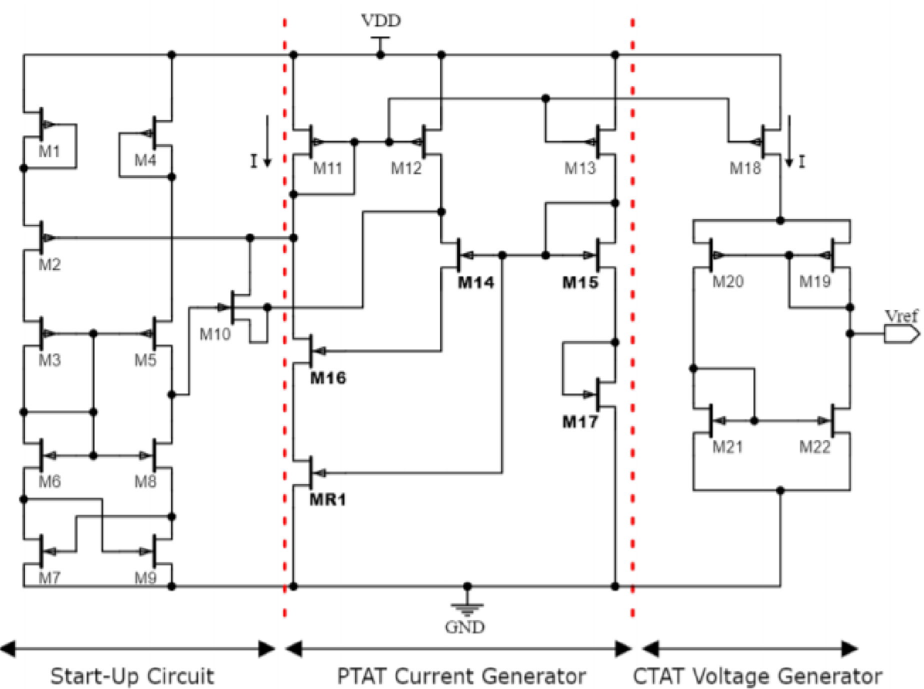


Figure 29: Resistorless voltage reference circuit schematics. Composed by a start-up circuit, a PTAT current generator, and a CTAT voltage generator.

Based on the features projected to the realization of the research work. A voltage reference was designed without the use of passive devices, such as resistors and capacitors. These passive devices unnecessarily increase the chip area, power consumption, and unreliability of the system. Also, it is planned to only use standard MOSFET, without any special implementation, such as using MOSFET with different threshold voltages.

3.1.1.1 Subthreshold Operation of MOSFETs

Subthreshold conduction occurs when the gate-source voltage is below the threshold voltage of the MOSFET. In this operating region, the depletion region underneath the gate is barely formed. As the concentration of minority carriers accumulated under the gate is small. The applied potential on the drain is not enough to force the electron to overcome the potential barrier from the source. Therefore, the current flows in this region are mainly through diffusion, contrarily to other operating regions in which the current flows by drift.

The subthreshold region is essential to achieve low-power circuits. With the continuous development regarding CMOS technology, the dynamic power, which is the main operational source to perform the circuits, is decreasing. On the other hand, as we enter in short-channel MOSFET, the static power, resulted from the subthreshold leakage current, is now comparable to the dynamic power. Therefore, it is necessary to set new strategies to start implementing that leakage current as of the main operational current. To understand it, we need to have a deeper understanding of the equation involved in this region, see equation 13.

$$I_D = \mu \cdot C_{ox} \cdot (\eta - 1) \cdot \frac{W}{L} \cdot V_T^2 e^{\frac{V_{GS} - V_{th}}{\eta \cdot V_T}} \tag{13}$$

Where W/L is the aspect ratio of the MOSFET device, μ is the carrier mobility, and η the subthreshold slope. V_T is the thermal voltage and V_{th} is the threshold voltage.

The resembling electrical characteristics between the subthreshold MOSFET and the BJT, allow the possibility to substitute these devices. Implementing subthreshold MOSFET within CMOS circuits, those circuits can operate in lower voltage supplies. That is due to the potential barrier of a diode-connected subthreshold MOSFET has a turn-on voltage much lesser than a p-n junction diode of BJT.

Although in terms of electrical performance, both devices are similar, both show an exponential behavior between the gate-source voltage and the drain current. However, relatively to thermal proprieties, both devices show some discrepancies. The subthreshold MOSFET presents parameters that are influenced by temperature, such as thermal voltage, threshold voltage, and surface mobility of electrons in channel, their temperature influence is shown in equations 14, 15, and 16, respectively.

$$V_T = \frac{k_B \cdot T}{q} \tag{14}$$

$$V_{th} = V_{tho} - k \cdot T \quad (15)$$

$$\mu = \mu_o \cdot \left(\frac{T}{T_o}\right)^{-m} \quad (16)$$

μ_o the mobility at the reference temperature T_o and m is the mobility temperature exponent. In this design, we assumed the value of m to be 1.5, the same value in standard CMOS technologies (Ken Ueno et al., 2009).

The output currents and voltages in circuits using subthreshold MOSFET devices have two different temperature behaviors, a PTAT, which the current or voltage increases with the increment of temperature, and a CTAT, which the current and voltage produced decreases with the reduction of temperature.

As possible to observe, μ is the only parameter that does not have a linear relationship with temperature. The temperature properties of the thermal voltage as well as the threshold voltage, due to their temperature linearity with contradictory behaviors, offer an appealing technique to compensate their dependence to reach temperature independence. Differently, the non-linearity dependency of μ makes it more difficult to compensate via this parameter.

3.1.1.2 Deep-triode region MOSFETs

As mentioned in this report, the usage of standard resistors in CMOS technology is not a viable approach to implement. Along with their unreliability, its extensive CMOS area is also a precise feature to avoid their use. Therefore, it is necessary to find another reliable approach to this problem. That was one of the motivations for avoiding traditional bandgap voltage reference, due to their requirement on using resistors to create a bias current.

It is important to understand how is possible to substitute this unsuitable component with a more appropriate one. Table 4 presents an overview comparison between MOSFET and BJT technologies. An interesting feature, which was implemented during the design phase, is the resistor-like behavior of the MOSFETs.

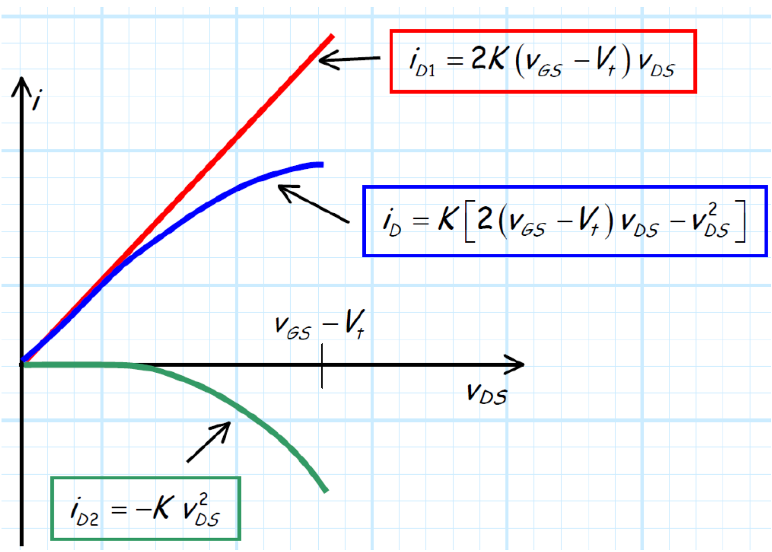


Figure 30: I-V behavior of a MOSFET in triode region. Presence of two different behaviors that complemented results in the MOSFET triode region.

$$I_D = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot [(V_{GS} - V_{th}) \cdot V_{DS} - \frac{1}{2} \cdot V_{DS}^2] \qquad 17$$

Equation 17, shows the current relationship in the triode region of the MOSFET. According to Figure 30, two behaviors are shown, the first portion of the equation 17 presents a linear relationship with V_{DS}, which represents the i_{D1} in the complemented figure. While the second portion, represented by the i_{D2}, demonstrates a quadratic relationship, which is responsible for giving the slight curvature towards the saturation region.

Observing the relationship of the produced current from the two different behaviors, for smaller V_{DS}, the portion with a quadratic relationship is considered negligible. Therefore, towards the deep-triode region, the drain current has a linear dependency with the drain-source voltage, having a resistor-like behavior. This linear relationship is expressed in equation 18.

$$I_D = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot [(V_{GS} - V_{th}) \cdot V_{DS}] \qquad 18$$

3.1.2 Circuit Topology

Resistorless voltage reference circuit provides a stable constant voltage based on the drop voltage through subthreshold and deep triode MOSFET. All the transistors are operating in saturation and subthreshold region unless M_{R1} which operates in the deep triode region.

According to Figure 29, the voltage reference circuit is comprised in three different stages, a Start-up circuit, PTAT current generator, and a CTAT output voltage stage to contradict the behavior of the generated current. Respective critical transistor sizes of the voltage reference circuit are shown in

Table 6. Important to refer that the final value of the transistor sizes was a multi-iterative process. From each iteration, a process of recognition of the voltage reference circuit behavior was conducted until the final schematic was made.

Table 6: Aspect ration of the critical transistors of the voltage reference circuit.

Transistor	**Width (μm)**	**Length (μm)**
$\boldsymbol{M_{11}, M_{12}, M_{13}}$	0.15	2.5
$\boldsymbol{M_{18}}$	0.15	7.5
$\boldsymbol{M_{14}}$	0.5	5
$\boldsymbol{M_{15}}$	0.3	2
$\boldsymbol{M_{16}}$	0.35	5
$\boldsymbol{M_{17}}$	4	2.8
$\boldsymbol{M_{R1}}$	0.18	4

3.1.2.1 Start-up Circuit

Any voltage reference possesses two optimal states, one when every MOSFET is OFF, and another that is considered the desirable state, which produces a constant voltage. The goal of the start-up circuit, presented in Figure 31 is to give the initial bias to turn-on by itself, after reaching the desired bias point, the MOSFET M_{10} turn-off, and the start-up circuit does not influence the rest of the circuit stages anymore.

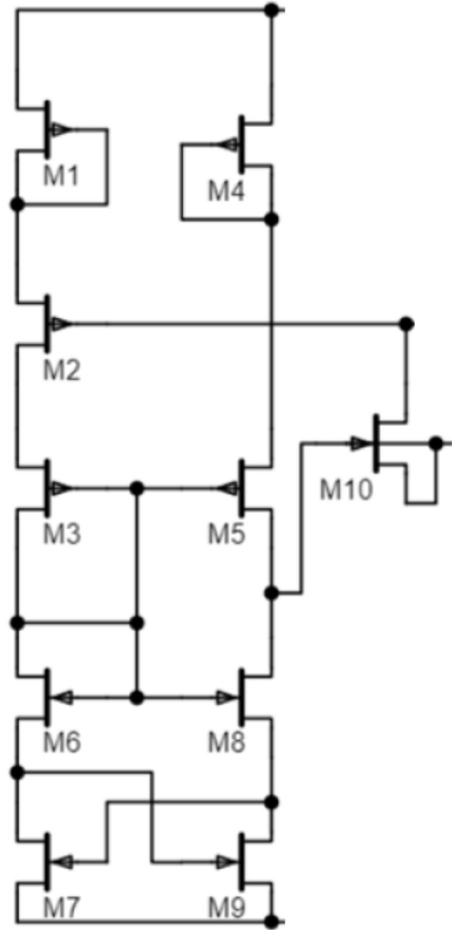


Figure 31: Schematic of the Start-up circuit. This circuit ensures the bias to the voltage reference optimal point.

3.1.2.2 PTAT current generator circuit

The generated current with PTAT characteristics can be solved based on the conservation of energy around the closed-circuit path using KVL. Similar to traditional bandgap reference, the deep triode MOSFET M_{R1} behaves as a resistor to determine the amount of current that flows through the circuit.

Therefore, the closed-loop is established by M_{R1} operating in the deep-triode region and M_{14}-M_{17} transistors operating in the subthreshold region.

The transistors M_{14}-M_{17} are essential to calculate the drop drain-source voltage in MOS resistor. Then, the working operation region of MOS resistor is a deep-triode region, as shown in Section 3.1.1.2, the drain-source voltage is directly proportional to the current that flows through the circuit. Therefore, equation 19, represent the KVL circuit path to calculate the drain-to-source drop voltage.

$$V_{DS_{MR1}} = V_{GS_{15}} + V_{GS_{17}} - V_{GS_{16}} - V_{GS_{14}} \quad 19$$

Rewriting the subthreshold equation described in 13 in terms of V_{GS}. Assuming that the intrinsic characteristics of the involved MOSFET are equal. The V_{DS_MR1} can be written as described in equation 20.

$$V_{DS_{MR1}} = \eta \cdot V_T \cdot \ln[\frac{(W/L)_{16} \cdot (W/L)_{14}}{(W/L)_{15} \cdot (W/L)_{17}}] \quad 20$$

From the equation 20, it is possible to observe, that the threshold voltage does not influence the drop drain-source voltage of the MOS resistor. The reason for this elimination was the even number of subthreshold MOSFET involved in the close loop. As observed in equation 19, exists an even number of subthreshold MOSFET which contradicts drop gate-source voltage, making it possible to eliminate this parameter. If the number of involved subthreshold MOSFET were odd, the threshold parameter could not be eliminated, and further elimination of this parameter to increase the efficiency would be harder.

To calculate the amount of current produced, the use of MOS resistor is essential. If a subthreshold or saturation MOSFET were used, the process to calculate the PTAT current would be more extensive, and the parameter influenced would be more complex to further analysis. Therefore, the deep-triode region was chosen. The understanding of this operating region is helpful because it is the region, which for smaller V_{DS} (V_{DS}<0.1V), transistor behaves as a resistor. Also, its implementation was the target point for voltage references explained in Section 2.7.1.

Regarding the deep-triode operation region of transistor M_{R1}, it is possible to apply the ohm's law due to its resistor-like characteristics, as shown in the equation 21. Therefore, the produced PTAT current can be quantified merging the equation 20 and 21, defining the current due to the deep-triode MOSFET as shown in equation 22.

$$I_D = \frac{V_{DS_{MR1}}}{R_{M1}} \quad 21$$

$$I = \mu \cdot C_{ox} \cdot (W/L)_{MR1} \cdot [V_{GS_{MR1}} - V_{th}] \cdot \eta \cdot V_T \cdot \ln[\frac{(W/L)_{16} \cdot (W/L)_{14}}{(W/L)_{15} \cdot (W/L)_{17}}] \quad 22$$

Equation 22 represents the PTAT current produced is determined by the respective sizes of the transistors involved on the close-loop (M_{14} - M_{17} and M_{R1}). It is also important to mention the parameters with temperature dependency, such as, V_{th} and V_T. Based on (Ken Ueno et al., 2009), V_{GSMR1} - V_{th} = (V_{GSMR1} - V_{tho}) + kT≈kT. This approximation is resulted from (V_{GSMR1} - V_{tho}) «kT. Therefore, the resulted PTAT current equation is shown in equation 23.

$$I = \mu \cdot C_{ox} \cdot (W/L)_{MR1} \cdot kT \cdot \eta \cdot V_T \cdot \ln[\frac{(W/L)_{16} \cdot (W/L)_{14}}{(W/L)_{15} \cdot (W/L)_{17}}] \quad 23$$

A concise analysis of the involved parameters in equation 23, reveals much helpful information to figure it out an approach that might be implemented in the following section, to reach voltage supply and temperature independence.

The produced current presents a positive dependence with temperature, resulted from the parameters T, V_T, and μ, which has a temperature dependency. Therefore, an approach must be implemented to eliminate these parameters.

3.1.2.3 CTAT Voltage Generator Stage

The use of MOSFET with high impedance on the current source and in the load, neglects any possible spontaneous changes of power supply, minimizing the line sensitivity, and its independence to the power supply. For theory simplification, as used in Section 2.7.1, let us consider the load stage as a simple diode-connected subthreshold MOSFET, represented by the equation 13, the constant output voltage is represented as shown in equation 24.

$$V_{Ref} = V_{GS} = \eta \cdot V_T \cdot \ln\left(\frac{I_D}{\mu \cdot C_{ox} \cdot (\eta - 1) \cdot W/L \cdot V_T^2}\right) + V_{th} \tag{24}$$

The PTAT current produced is mirrored to the output stage. Therefore, the reference voltage is shown in equation 25.

$$V_{Ref} = \eta \cdot V_T \cdot \ln\left(\frac{(W/L)_{MR1} \cdot kT \cdot \eta \cdot \ln[\frac{(W/L)_{16} \cdot (W/L)_{14}}{(W/L)_{15} \cdot (W/L)_{17}}]}{(\eta - 1) \cdot W/L \cdot V_T}\right) + V_{th} \tag{25}$$

To calculate the TC of the circuit the derivative equation 26 must be equal to zero. However, it is also necessary to maintain a constant reference voltage from voltage supply inconsistencies. Due to the applied simplifications through the schematic design, the voltage reference circuit still is dependent on temperature, and the modification of the involved transistors can improve the line sensitivity of the voltage reference. However, it degrades their behavior towards the temperature independency. Therefore, it was necessary to establish a trade-off between the performance parameters.

$$\frac{\partial V_{ref}}{\partial T} = -k + \eta \frac{K_B}{q} \ln\left(\frac{\left(\frac{W}{L}\right)_{MR1} \cdot k \cdot \eta \cdot \ln[\frac{\left(\frac{W}{L}\right)_{16} \cdot \left(\frac{W}{L}\right)_{14}}{\left(\frac{W}{L}\right)_{15} \cdot \left(\frac{W}{L}\right)_{17}}]}{(\eta - 1) \cdot \frac{W}{L} \cdot \frac{K_B}{q}}\right) \tag{26}$$

3.1.3 Results and Discussion

The main objectives of the design were to establish an accuracy performance between the temperature and voltage supply independence with a high-power supply rejection ratio.

This section gives an overview of the performance of the voltage reference. The simulation results were developed in Cadence SPICE simulation tools, using a 130nm CMOS technology chosen from a manufacturing company.

Figure 32 shows the minimal variation of the output reference voltage for power supplies within a range of 1V to 3.2V. The average reference voltage at 27◦C, considered temperature room ambient, is 258.38mV. Line sensitivity measures the variation of the output for a voltage supply range, guarantying stability in terms of the voltage supply. In the designed circuit, the line sensitivity was 0.49 %/V, although it is not a very accurate performance metric, it is better compared to other research works.

The range of operation is enough to turn on the voltage reference to produce a reference voltage. This characteristic is viable for this research project because due to the intermittent and unpredictable input signals from the energy green sources, this circuit is suitable to provide a reference voltage for different circuits within the PMC chip.

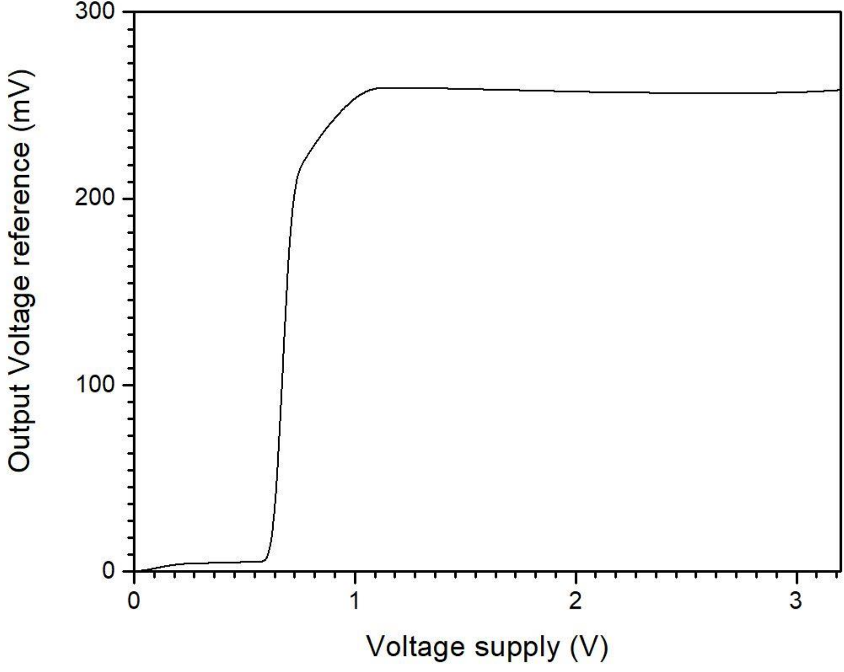


Figure 32: Simulation results about the variation of the output reference voltage with the increment of voltage supply.

During the process of the designed circuit, different approaches were made to simplify the theory of the circuit, such as all the intrinsic characteristics of the relevant MOSFET for the PTAT current generator were equal, and the adoption of a large impedance load, as well as, the implementation of large MOSFET in the current mirror. These different practices improved some performance metrics, such as the line sensitivity and power supply rejection ratio. The circuit turns out to be more robust to voltage supply variations, making it suitable for energy harvesting applications. However, the effectiveness relative to temperature variations worsens, the voltage reference was measured relative to temperature variations

for a range from -10 to 60◦C, considering 27◦C ambient temperature. The results of this simulation are shown in Figure 33, confirming the measures taken upon the circuit design, the existence of disparities concerning the output reference voltage with temperature deviation. The produced voltage suffers a reduction with temperature. This reduction is not convenient, creating potential complications in the precision of the circuit design.

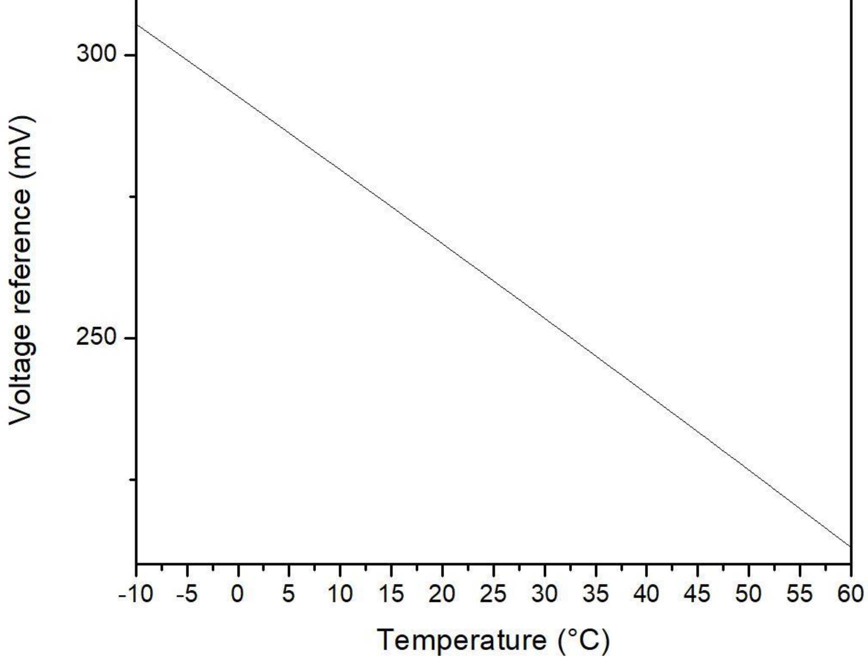


Figure 33: Simulation results about the variation of the output reference voltage with temperature.

The power supply rejection ratio was simulated to elucidate the performance of the voltage reference, see Figure 34, to verify the robustness of the voltage reference to power supply variations. Its simulation comprised an introduction of a filtering capacitor, C=5pF, with a voltage supply of 2V. The rejection ratio is 51.8 dB at 100 Hz and 22dB at 1MHz. This metric confirms the power supply independence.

The adoption of a different strategy for the output stage damaged the temperature coefficient of the circuit, the operation region of the MOSFET involved were not capable of eliminating the parameters dependent on temperature, such as thermal voltage (V_T), and threshold voltage (V_{th}). However, this approach improved other metrics. With high impedance devices, the voltage reference circuit is more robust to voltage supply variation, improving the line sensitivity and power supply rejection ratio. Although, this existent trade-off, the circuit shows referencing capability towards analog, mixed-signal circuits.

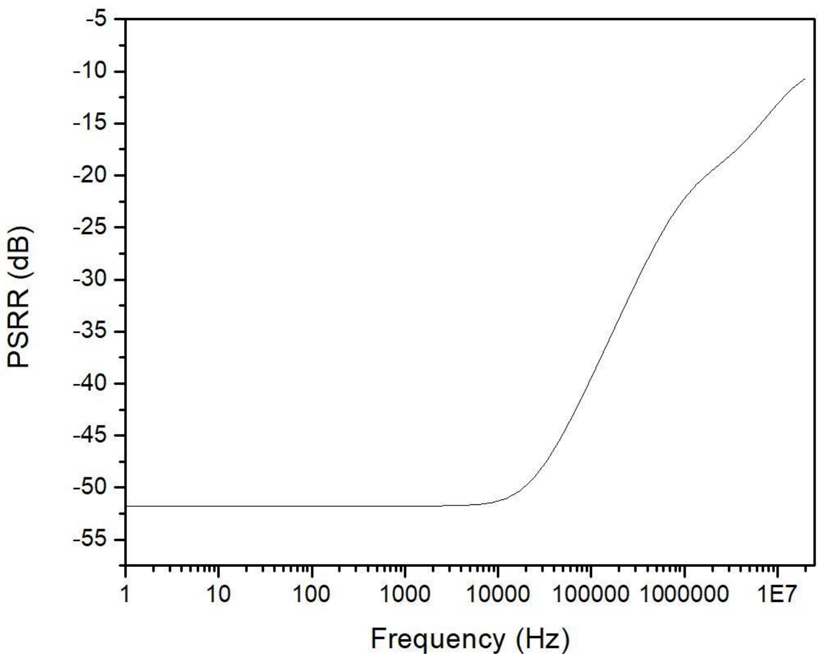


Figure 34: Simulation results of the power supply rejection ratio depending on the frequency at V_{DD}=2V.

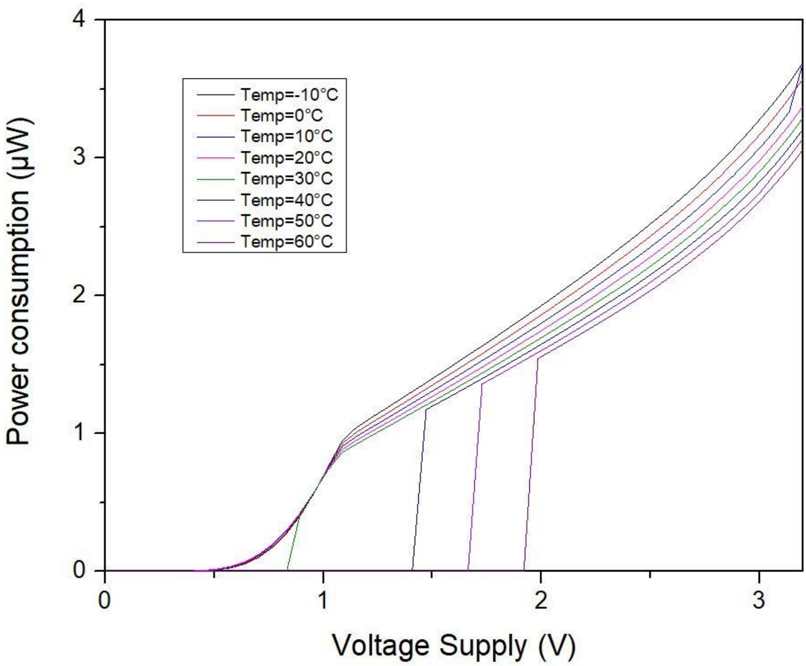


Figure 35: Power consumption of the voltage reference voltage with variation of the voltage supply and increment of temperature.

The adoption of a different strategy for the output stage damaged the temperature coefficient of the circuit, the operation region of the MOSFET involved were not capable of eliminating the parameters dependent on temperature, such as thermal voltage (V_T), and threshold voltage (V_{th}). However, this approach improved other metrics. With high impedance devices, the voltage reference circuit is more

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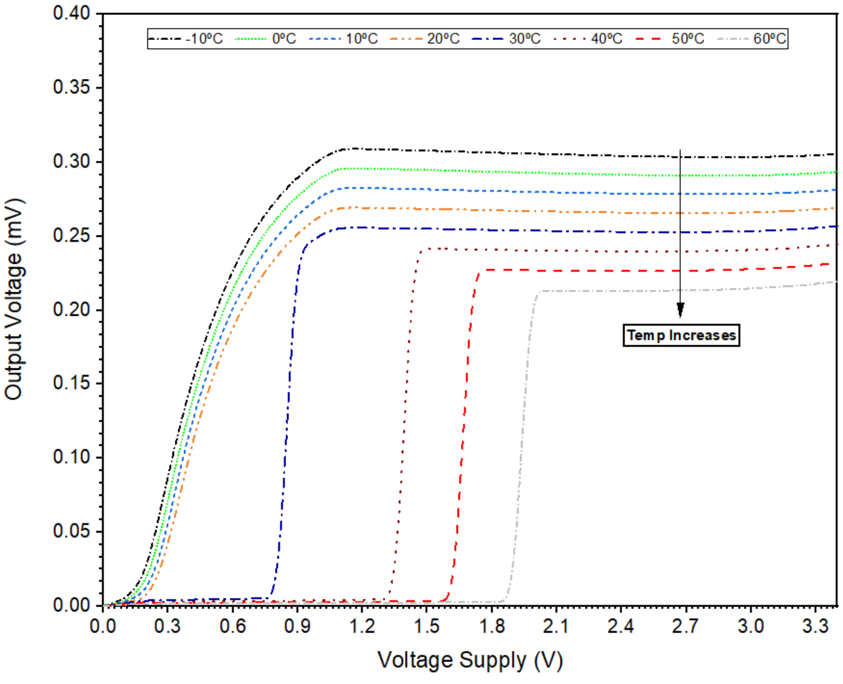

Figure 36: Voltage reference measurements through different voltage supplies and temperatures.

Figure 36 elucidates the behavior of the reference circuit. Although the output voltage decreases due to temperature, the circuit remains robust with a suitable line sensitivity and power consumption towards application that the research project was designed.

3.1.4 Layout Design

Respecting the layout rules imposed by the foundry regarding the CMOS technology processes, the layout was performed. After this process, physical verification was conducted. It is an important step for the IC fabrication, it ensures a correct electric and logic functionalities and manufacturability. It involves the DRC, to verify that layout respects all the CMOS rules imposed by the foundry, the LVS, it checks both layout and schematic designs for any netlist difference. Moreover, finally, ERC that verifies the electrical connections for unconnected inputs or shorted output, as well as precise power and ground connections.

Over time, to meet the improved performance requirements, CMOS process needs to be updated with better processes. This circuit design does not have full compatibility with lower CMOS technologies.

However, respecting the layout rules, few adjustments are necessary to incorporate into newer technologies.

3.1.5 Summary

A robust low-power voltage reference was designed, providing an average voltage bias of 258 mV. Compared to previous researches, Table 7, although the defined characteristics, the circuit performs in a wide voltage supply range.

During Section 3.1.3, simulations have been performed regarding the sensitivity and robustness of the circuit. The designed circuit provides a suitable bias voltage for low-power consumption applications, as well as, for low voltage operation.

The circuit was designed in 130nm CMOS technology, studying the potentialities of subthreshold and deep-triode MOSFET. The final layout was sent for fabrication. Future work comprises testing of the integrated circuit and compares with the results performed during the simulation. Also, to improve the overall sensitivity, further research must be done to improve the temperature coefficient of the reference circuit.

Table 7: Research Comparison

	Designed Circuit	**(Parisi, Finocchiaro, Papotto, & Palmisano, 2018)**	**(Magnelli et al., 2011)**	**(H. Wang & Ye, 2007)**	**(Koushaeian & Skafidas, 2010)**
CMOS technology	0.13-µm	0.13-µm	0.18-µm	0.18-µm	65-nm
Type	Sub.MOS	N/A	Sub.MOS	Sub.MOS	Bandgap
Voltage supply range	1-3.2 V	1.1-2.4 V	0.45 – 2V	0.6-2.3V	1.1-1.3 V
Output voltage (V)	0.258	0.8	0.2635	0.220	0.364
Line sensitivity (%/V)	0.49	2	0.44	2.730	0.75
PSRR (dB)	51.8	36	45	41	60

3.2 Current Staved Voltage Controlled Oscillator

This section presents the study and development for the design of a current starved voltage-controlled oscillator. Figure 37 shows the developed oscillatory circuit. The proposed circuit is responsible for setting a clock-time pulse to a digital system, releasing the stored energy that was extracted by the energy harvester. Therefore, a set of requirements is necessary to fulfill the objective of this circuit, such as low-power consumption, coherent oscillatory signal, and signal frequency stability for a wide voltage supply range, because of the uncertain power that supplies the PMC chip.

The current starved VCO presents characteristics that can solve these problems since its output frequency signal is indirectly dependent on a control voltage. The control voltage provides a reference voltage to bias a MOS device, allowing the production of a current that will be mirrored to all the delay stages, and the process of charging or discharging the output capacitance is dependent on the threshold voltage of the delay stage. Therefore, the voltage reference circuit in Section 3.1 can be integrated to provide a balanced constant voltage to support the oscillator performance.

$$f_{osc} = \frac{I_D}{2 \cdot N \cdot C_{tot} \cdot V_{ctrl}} \quad (27)$$

Equation 27 represents the linear relationship between the properties that influence the oscillation frequency. The C_{tot} is defined as the total capacitance for each delay stage, such as the capacitance of the inverter digital block and the load capacitance. These capacitances increase the node capacitance of the delay stage. Therefore, the delay fluctuations have resulted in the MOSFET drain current, controlled by the voltage reference, and the process of charge and discharge the node capacitances. Factor 2 refers to the topology characteristics of the Current-Starved VCO, which needs to pass twice through the delay stages to complete a single oscillation period. Furthermore, the V_{ctrl} is the control voltage that defines the current that charges and discharges the inverters' stage to propagate the delay signal.

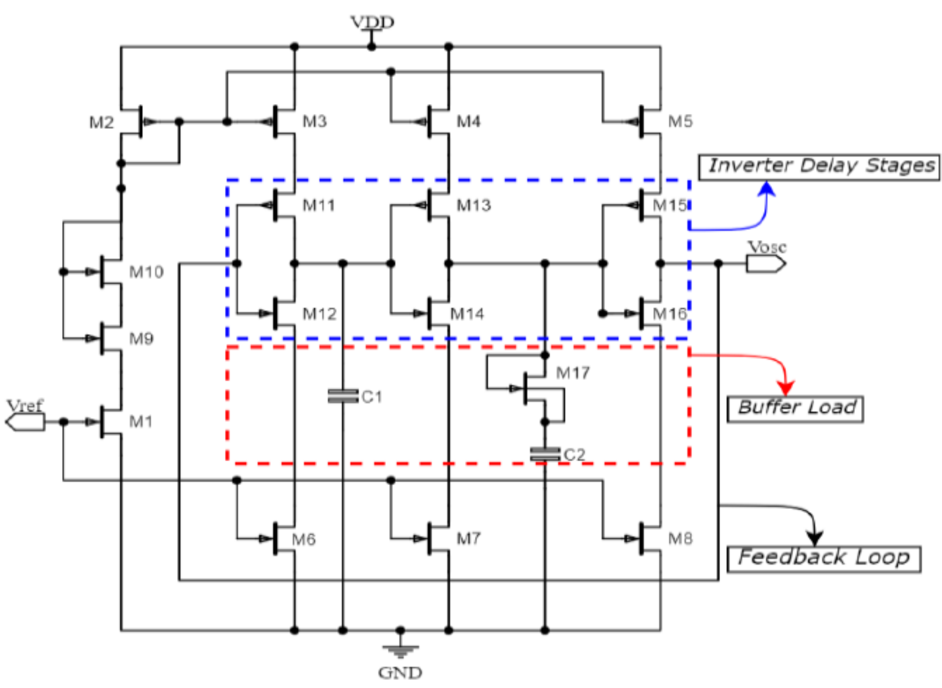

Figure 37: Schematic of the current starved VCO.

Table 8: Specifications of the current starved VCO components.

Component	Specifications
M_1	1/0.13 (μm)
M_{11}, M_{13}, M_{15}	7.5/0.13 (μm)
M_{12}, M_{14}, M_{16}	20/0.13 (μm)
M_3, M_4, M_5	0.15/0.5 (μm)
M_{17}	0.15/10 (μm)
C_1, C_2	983.138 fF

3.2.1 Results and Discussion

Figure 38 A) shows the output voltage waveform of the multi-phase periodic signal. Ideally, the expected waveform should be trapezoid waveforms, where it was easily distinguished from the different operating regions of the MOSFET involved in the delay stage. Figure 38 B), and C) illustrates the charging process through the PMOS in the inverter delay-stage, and discharging process through the NMOS, respectively.

The current flowing through the stages should be homogeneous with small peaks of current, corresponding to the commutation of MOSFET operating region. The process of charging or discharging

the output capacitance corresponds to the PMOS and NMOS devices operating in saturation mode, respectively. Once the output capacitance is charged, the MOSFET commute to the ohmic region, and remain steady until, until the previous delay-stage changes its behavior. In an ideal situation, the saturation, and triode regions of PMOS and NMOS never overlaps, i.e., when the NMOS is in the process of charging the output capacitance, the NMOS is OFF. Differently, the process of discharging the output capacitance, the NMOS is active in the saturation region, while the PMOS is in the cut-off zone. In this design to decrease the output frequency, the node capacitance was increased with the implementation of capacitors and a diode connected MOSFET.

However, due to the presence of leakage current, the ideal behavior becomes distorted, the perfect independent current peaks resulted from the charging process do not exist. The inevitable leakage current is observed at the same time during the operation process of both MOSFET. To complement this statement, in Figure 38, observing the waveform corresponding to the second and third delay stage, it is possible to see that when the NMOS in the second stage reaches the saturation, discharging the output capacitance, also exists at the same time, an opposing current flow through the PMOS of the third stage to charge the output capacitance.

Another feature possible to observe is the Barkhausen condition to sustain oscillation; the feedback signal should be enough to maintain oscillation. As the presented circuit possesses three inverter delay stages, each one will contribute with a phase shift of 60◦ being necessary to pass two times through the circuit to complete a periodic oscillation.

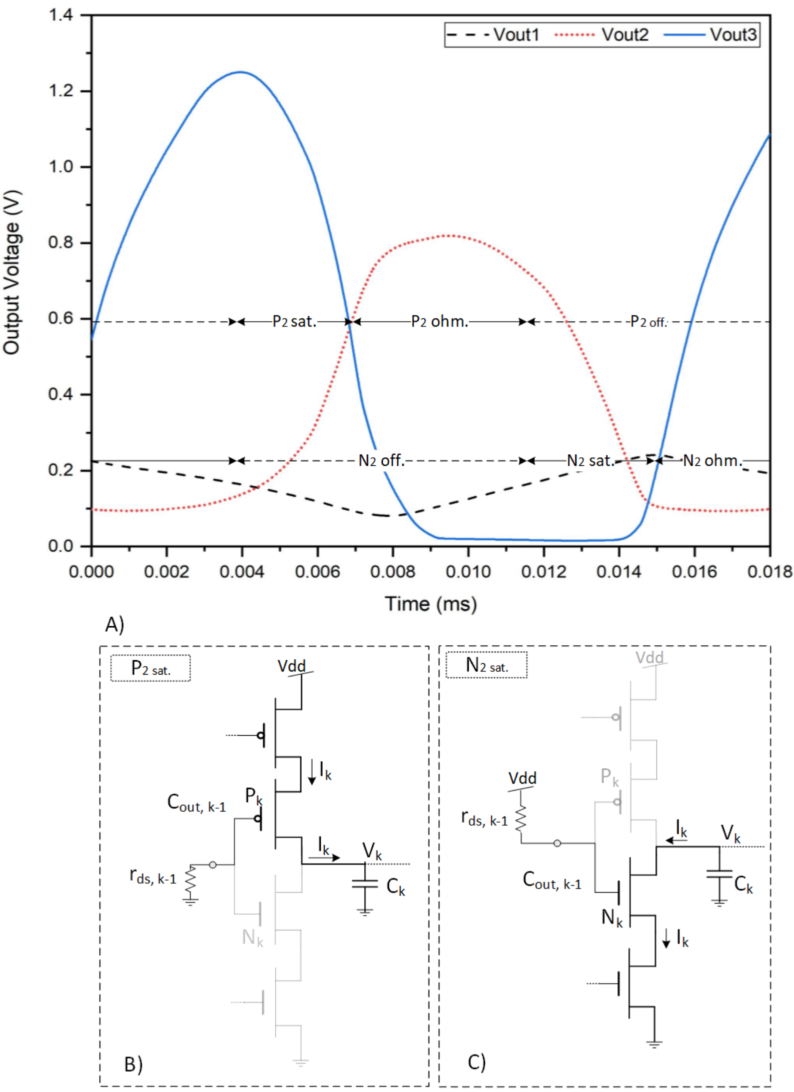

Figure 38: Current Starved VCO output waveform. A) a representation of the behavior of the periodic output voltages of the three implemented delay stages (N=3) of a current starved VCO. The working region of MOS devices are also indicated. B) a representation of the charging process, and C) discharging process.

As mentioned, the voltage control of this circuit is the reference voltage described in Section 3.1. To visualize the variation of the oscillator performance, first, we need to verify the disturbing behavior of the oscillator due to fluctuations of the voltage reference. Figure 39 shows the variation of the periodic signal characteristics, such as frequency and its maximum output voltage. Two different operational zones have been observed—the non-operational zone, which varies between 0-1V of the voltage supply. An unused behavior characterizes this region because the voltage reference was not producing constant voltage, see Figure 32. Therefore, after a simulation in this region, it was observed non-oscillation near the 0V region and non-sinusoidal oscillations near 1V.

In contrast, the oscillation zone produced a suitable sinusoidal oscillation for voltage supplied from 1-3.2 V with an average oscillation frequency of 84.81 kHz.

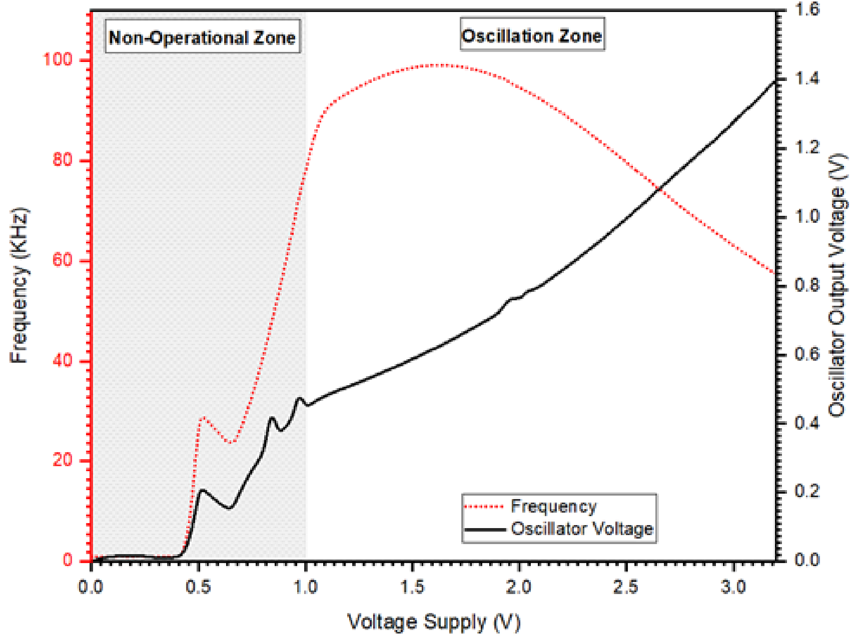

Figure 39: Variation of the oscillator frequency and maximum output voltage through voltage supplies alterations. Categorization of two independent oscillation region, being the oscillation zone the appropriate for circuit purpose.

Since the voltage reference does not have an appropriate TC is important to study the oscillator performance under these circumstances. Therefore, it was performed a transient and parametric analysis to verify the performance of the oscillator. Figure 40 represents the periodic signal frequency influenced by the output reference voltage, as expected, since the voltage reference does not have an appropriate TC, i.e., with further increases of temperature the output reference voltage decreases. If there is less bias gate voltage, the current that flows for each delay stage through the current mirror decreases, and according to equation 27, the frequency of the periodic signal will decrease.

According to Figure 40, the aspect mentioned above is confirmed, exists a decrement of frequency, but, that decrement is not drastic compared to what was expected, the frequency for temperatures between 10◦C to 55◦C have a variation of 10kHz, which does not have a great effect on the performance of the oscillator.

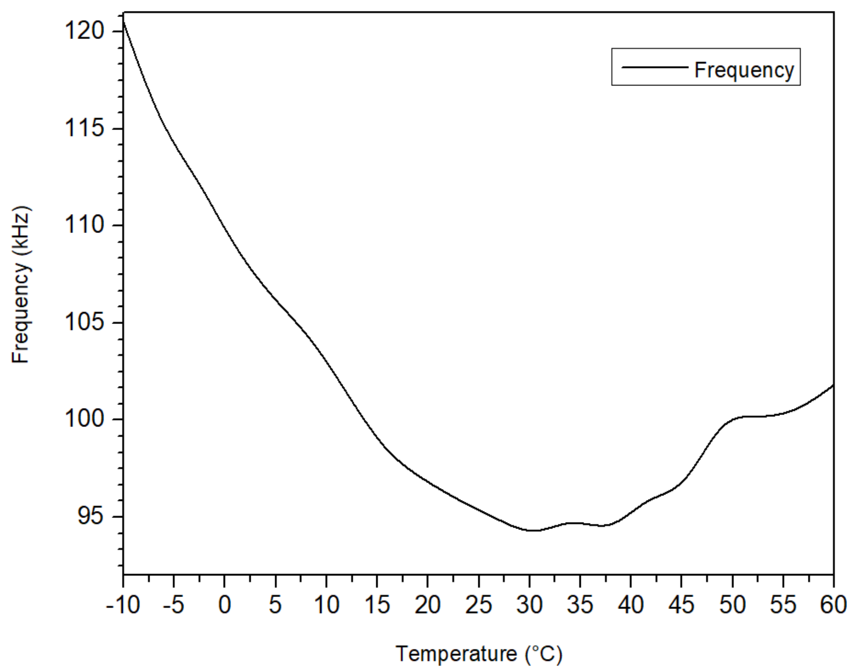

Figure 40: Variation of the oscillatory frequency with the increment of temperature. Verification of the influence of the inappropriate TC of the voltage reference.

Figure 41 shows the power consumption of the designed oscillator circuit. Since, the power consumption one of the biggest concerns on the project research, this circuit consumes less than 4μW at 3V, being suitable to provide low-power periodic sinusoidal signals. Also, this figure confirms what was expected in Figure 39 is possible to observe a voltage reference reduction as the temperature increases. That aspect is possible to observe if a voltage supply is fixed and verify the minimization of power supplies for higher temperatures.

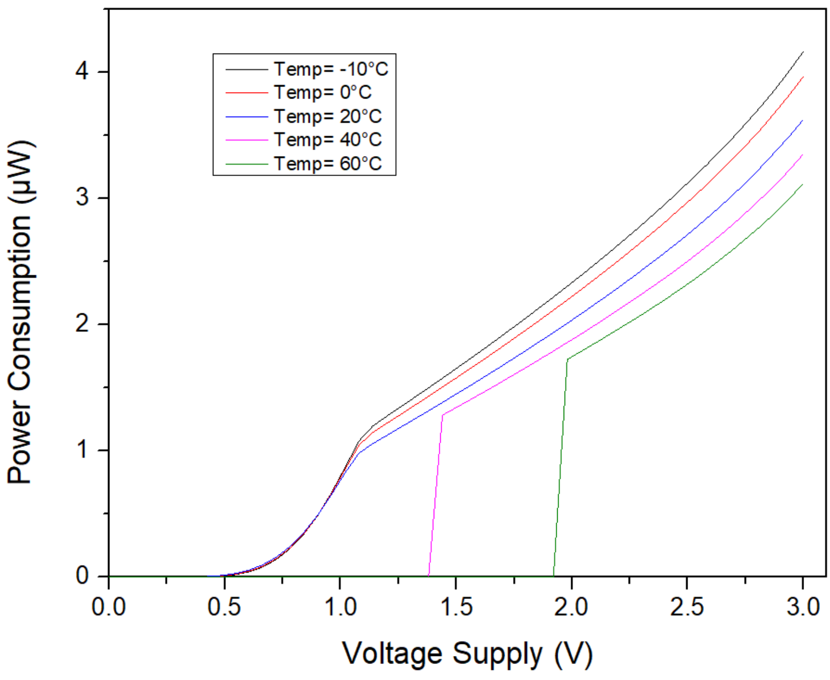

Figure 41: Oscillator power consumption with variation of voltage supply and temperature.

Jitter is a method of describing the stability of an oscillator in the time domain; it combines all the noise sources and exhibits their effects in the time domain. Describing the variations of the signal period, and the time distances from the ideal periodic value.

Figure 42, represents the variation of jitter of the oscillator. Jitter represents the time variation for the ideal time reference, i.e., an oscillator does not always have the same behavior, due to the presence of noise, such as thermal noise, the behavior of the oscillator deviates from the expected ideal oscillation. The implemented circuit is not an exception, for the presented transient time; most of the time deviation is on the scale of ns. Although the jitter is accumulative, i.e., if in one oscillation it suffers a time deviation, that time deviation remains through the next oscillation, it does not affect the performance of the oscillator very much, due to positive and negative time shift in the nanoscale.

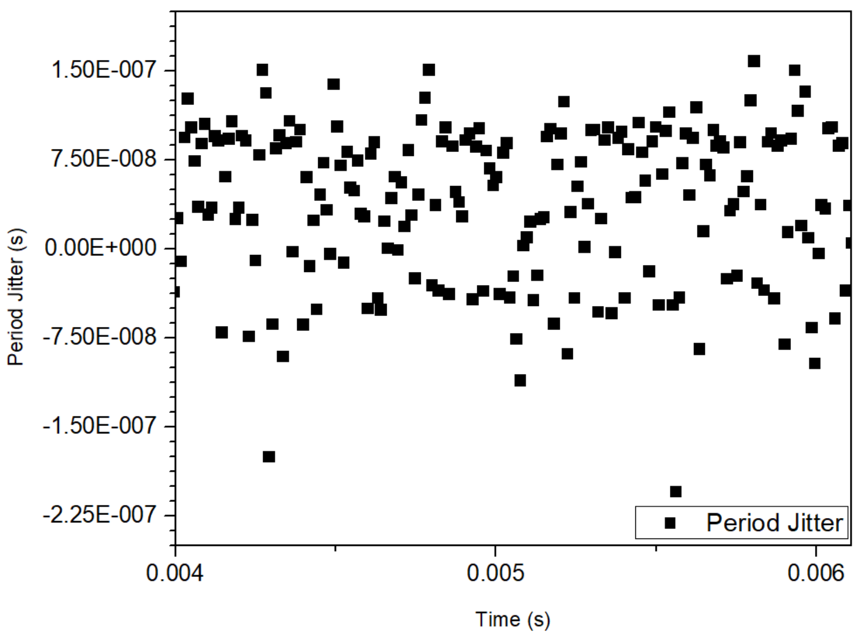

Figure 42: Variation of the period jitter for a specific period of time.

To verify the performance and reliability of the circuit, a 100 number of samples were performed by using the Monte Carlos analysis within the cadence software. This analysis was carried out at V_{DD}=3V, corresponding to an average voltage reference of 257.5mV, at 27°C. Figure 43 shows the statistical analysis of a periodic signal frequency for the stipulated conditions with 100 samples. A standard deviation (σ) of 139.373Hz with a mean value (μ) of 62.8723kHz is observed. The variability presented (σ / μ) as the value of 0.0022. The resulted of this deviation is mainly caused by the process mismatches of the MOSFET.

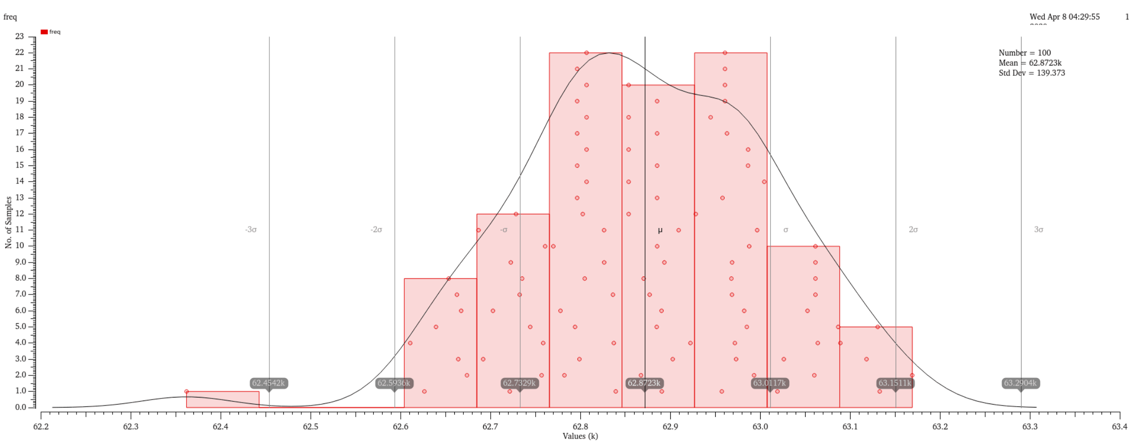

Figure 43: Statistical Monte Carlo Analysis of frequency oscillation deviation for V_{DD}=3V at 27° C. The voltage reference was kept at 257.7mV.

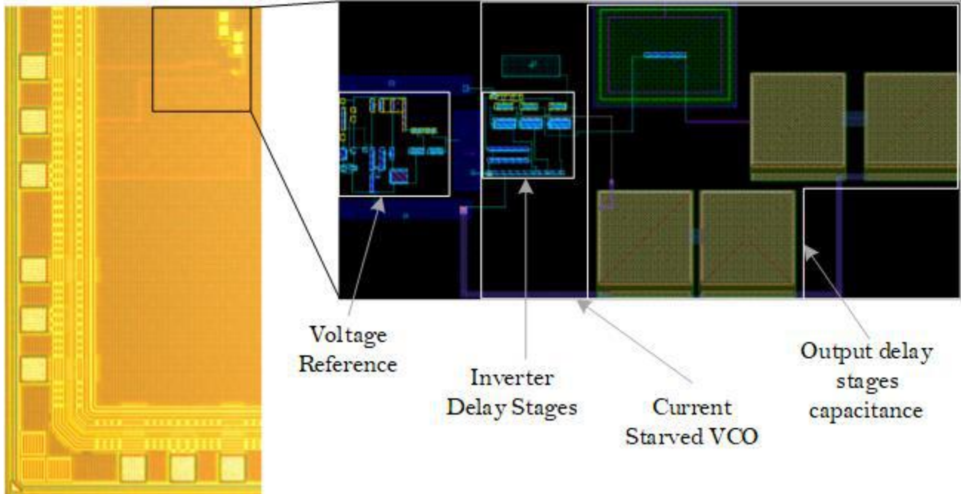

Figure 44: A) Chip micrograph view of the proposed Current Starved VCO. B) Respective layout design and differentiation of sub-circuit blocks.

The designed circuit of a current starved VCO and its voltage reference as the control voltage constitutes a fundamental part of a prototype chip for energy harvesting application. The chip area has 25mm^2 and it was used a 130nm standard CMOS process, with 1-poly layer, 7-metal layers, and 1 top-metal layer with an active area of 0.013mm^2 (=167.32µm × 79.67µm). Figure 44 A) shows a micrograph view of the designed circuit and Figure 44 B) represents the designed layout in Cadence Software (Layout XL) with the sub-circuits involved to provide a periodic signal.

3.3 Current Reference

This section presents a study and discussion of a current reference circuit. A current reference consists on a sum of PTAT current and a CTAT current. As shown in Figure 45, and Figure 46, three sub circuits are required to generate a stable current reference independent from temperature. Depending on the produced current by the PTAT and CTAT sub circuits, a current adder is used to compensate these two current behaviors for cancelling each other.

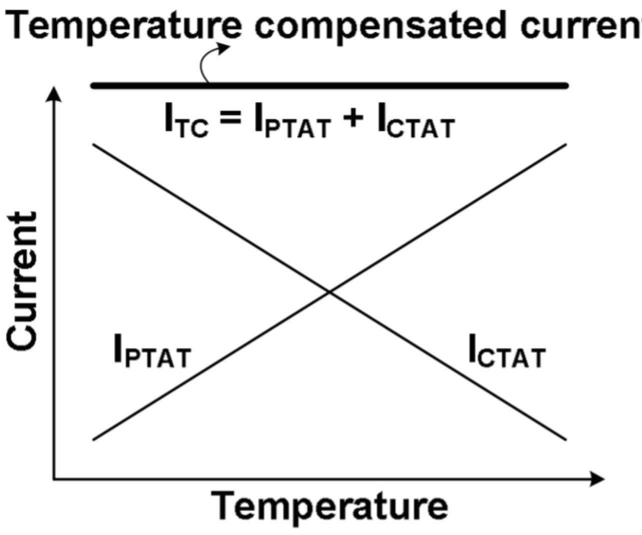

Figure 45: Illustration of the current reference function. It shows how is possible to achieve the temperature compensated current.

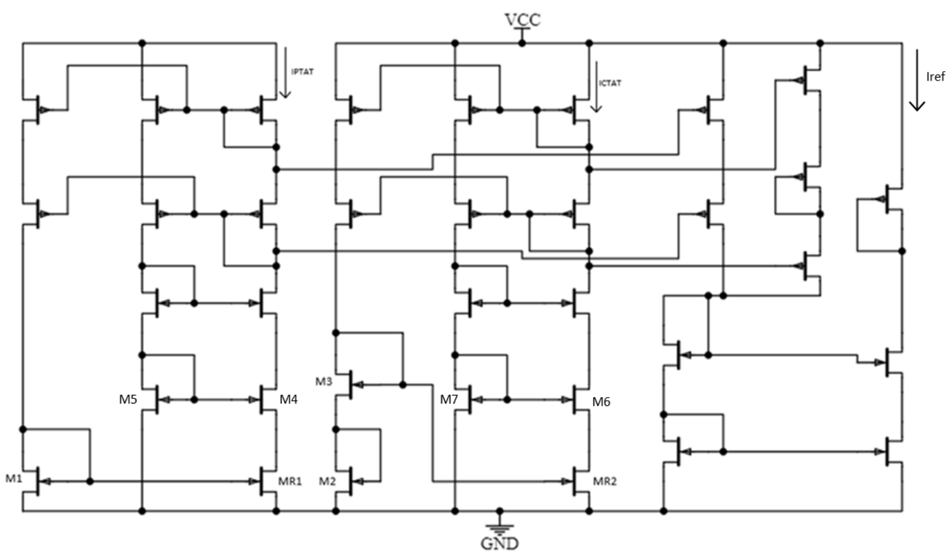

Figure 46: Architecture of a current reference using deep triode (MR1, MR2) and subthreshold MOSFET (M3). This circuit consists in three different sub-circuits, a PTAT current, CTAT, and a current adder.

Figure 46 shows a studied current reference circuit consisting of a beta multiplier self-biasing circuit exploring subthreshold and deep-triode MOSFET. To reach that operation zone, a cascade of MOSFET in saturation are implemented in both PTAT and CTAT sub circuits. The cascade of MOSFET in

saturation mode will minimize the drain-source voltage, till that voltage is almost negligible. The negligible voltage is the first step to put the last cascade layer in the deep-triode region. To have a MOSFET behaving in the last cascade layer in the deep-triode region, a third branch is needed.

Moreover, in this third branch, the operating region of the involved MOSFET will influence the TC of each sub-circuit. For both PTAT and CTAT sub-circuits, a reasonable gate voltage is given for MR1 and MR2. Therefore, according to I-V characteristics of a MOSFET, if the drain-source voltage is very small and the gate-source is high compared to the drain-source voltage, this MOSFET operates in the deep-triode region.

Since both PTAT and CTAT sub circuits have a similar structure to the definition of MR1, and MR2 as operating in the deep-triode region. The difference in the temperature behavior is dependent on the transistor topology responsible for setting a voltage bias to the deep-triode MOSFET.

In the PTAT sub circuit, the diode-connected transistor M1 operates in a strong-inversion region. While in the CTAT sub circuit, the bias voltage is defined by two diode-connected, M2 in the strong-inversion region, and M3 in the subthreshold region. This MOSFET is operating in the subthreshold region because of M2, the V_{GSM3} is nearly zero. Exploiting these two different topologies, it provides two different opposed temperature characteristics. Since the topology of the first sub circuit, the bias voltage provided by M1 can eliminate the threshold voltage with temperature, generating a positive temperature coefficient current IPTAT. While the CTAT sub circuit, since the temperature coefficient of the bias voltage becomes larger than the threshold voltage, the ICTAT has a negative temperature coefficient. The specification of the involved MOSFETs are shown in Table 9

Table 9: Dimension of the critical transistor of the current reference circuit.

Transistor	Width (μm)	Length (μm)
M_1	0.6	0.13
M_2	5	0.13
M_3	1	0.5
M_4	8	0.13
M_5	5	0.13
M_6	2	1.4
M_7	0.6	0.13
M_{R1}	2	0.13
M_{R2}	0.8	0.28

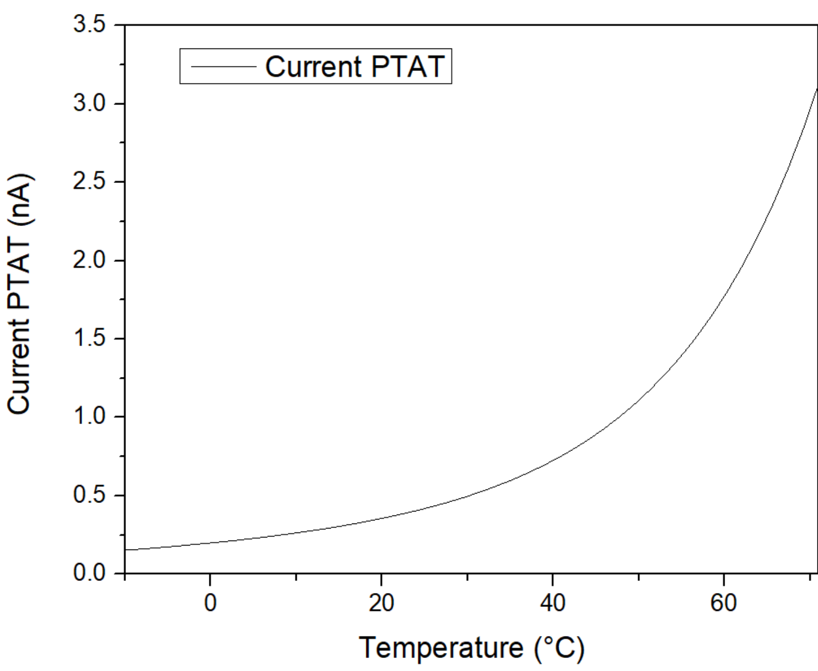

Figure 47: Simulation results about the PTAT behavior of the current reference sub-circuit.

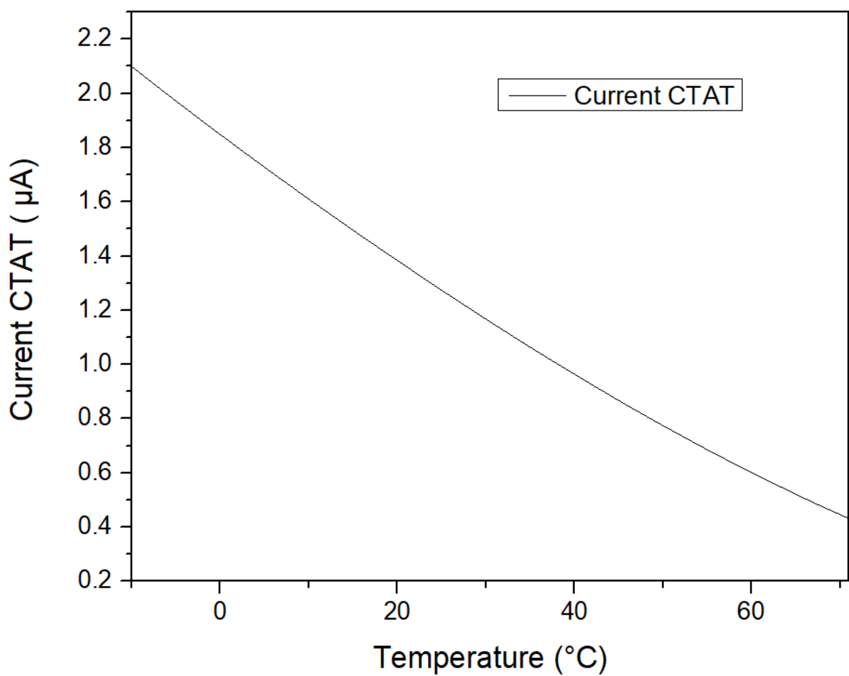

Figure 48: Simulation results concerning the current reference CTAT sub-circuit.

After elucidated the sub circuit behaviors, it is necessary to visualize them to understand the method of amplification that is required in the current adder to achieve a constant current reference. The Figure 47, and Figure 48 shows the simulation results of the PTAT and CTAT behavior of the current reference sub circuit, respectively. As possible to observe these two behaviors have a different order of

magnitude of the produced current. Therefore, in the last stage of the current reference, the current adder, it is needed to establish a mid-term between these two currents to sum and produce a stable constant current. Although the two produced current have different dependencies, the current produced by CTAT is almost ideal, it nearly linearly dependent. The current produced does not show dependency linearly, the temperature behavior exhibits an exponential dependency. This dependency makes cancellation difficult. If the two behavior had the same slope, the cancellation process would be much easy. Since the current produced by the CTAT sub circuit has a higher produced current, this current in the adder stage must be reduced. On the other hand, the current produced by PTAT sub circuit needs to be amplified.

Figure 49 is the result of the output reference current; the circuit starts to produce a measurable average current of 45nA for a minimum voltage of 1.5V. The produced current reference is not stable, which can cause problems to the reliability of further circuits that uses its bias current. An explanation for this behavior is the exponential increment of the PTAT current, which corresponds to the same behavior on the output reference current.

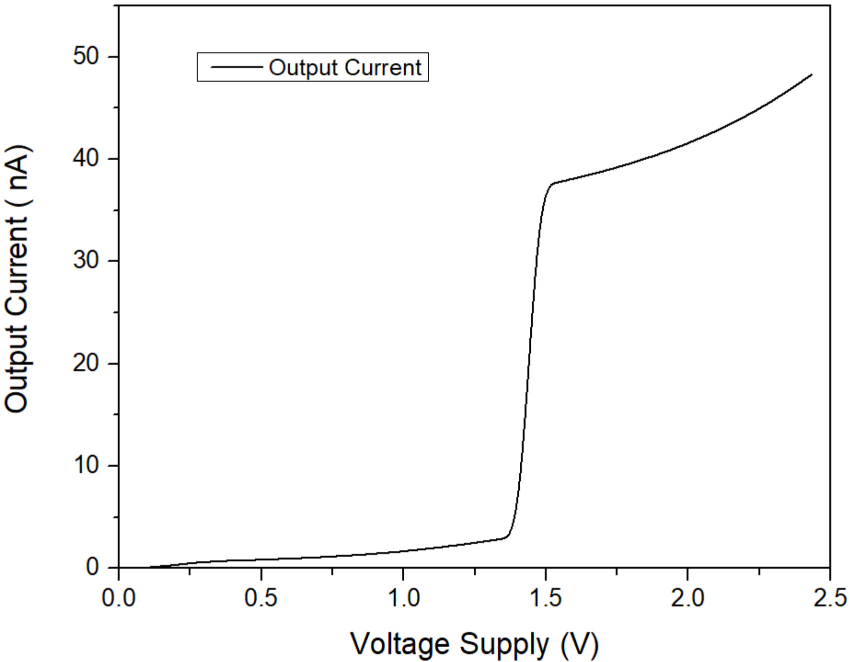

Figure 49: Variation of the output current due to fluctuations of voltage supply.

After visualizing the line sensitivity of the current concerning voltage supply changes, another important aspect is the temperature coefficient. Figure 50 represents the temperature dependency of this circuit, for voltage supplies above 1.9V, the current reference circuit shows satisfactory temperature dependency, but as the voltage supply increases, the range of temperature decreases. This fact happens due to the exponential increase of the PTAT sub-circuit for higher temperatures. It influences the current

reference circuit to adopt the same behavior. For lower temperatures, the reference circuit has a CTAT dependency.

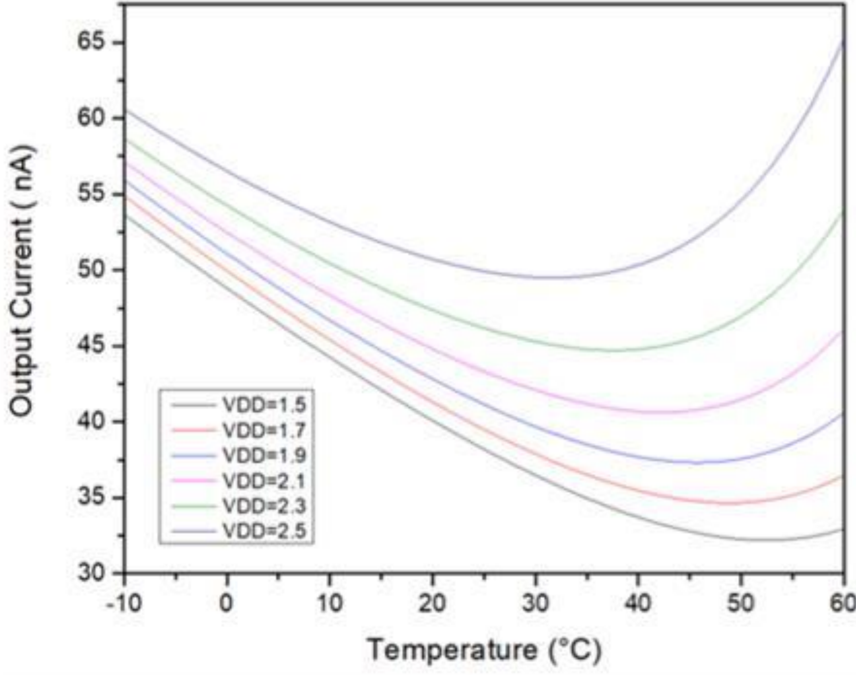

Figure 50: Variation of the output current with variation of temperature and voltage supply.

The main requirement of academic research is low power consumption. Figure 51 shows the power consumption for a wide range of temperature and voltage supplies. As the temperature increases, the power consumption decreases, always remaining under 10μW for the simulated voltages supplies.

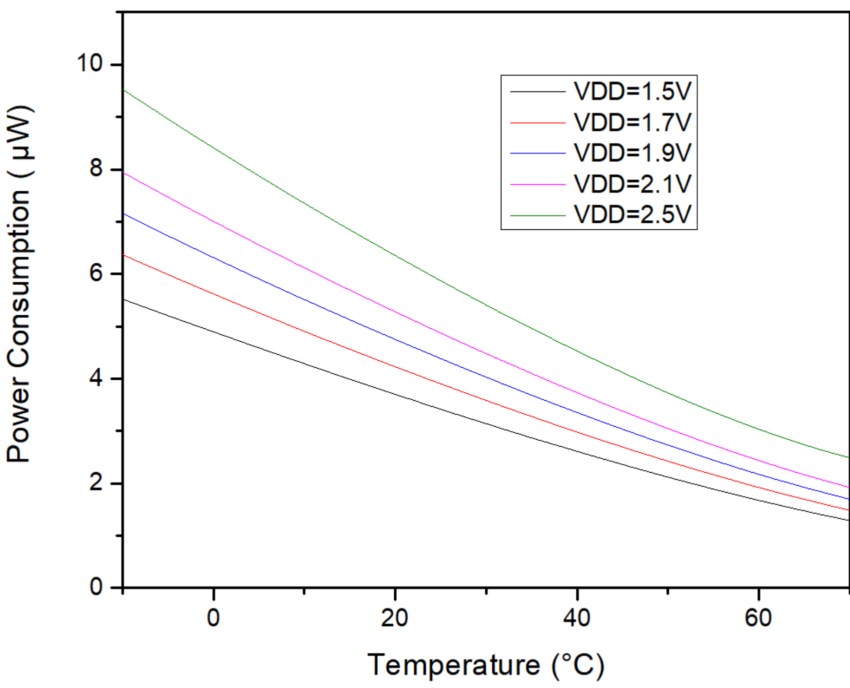

Figure 51: Power consumption of the current reference circuit for different temperatures and voltage supplies.

3.4 Layout

After the schematic and simulation were performed and verifying its performance, the layout design of the intervening circuit was made. Due to the size of the implemented CMOS technology, and external foundry was used to fabricate the chip. All the layout was performed related to the rules and specifications that the external foundry requires. It was used a 130nm CMOS technology, along with 7-metal layers, 1-top-metal, and 1-poly layer. The increased number of metal layers was useful to decrease the layout area because it could be used to pass over the transistor's other layers. The top-metal layer was used to connect the circuits to the pads and the capacitors.

Although the foundry gave the layout design of the pads and the transistors, several approaches were performed to improve the layout, such as the multi-finger approach, the overlap of metal, and VIA layers to decrease the parasitic impedance.

After the layout was performed, several physical verification tests were made to verify the integrity of the circuits. The DRC is a process to confirm the layout of the chip satisfies the number of rules defined by the semiconductor manufacturer. Each semiconductor foundry has its own set of rules to ensure that the variability of the process does not affect chip failure. The second test was LVS. It provides the connectivity comparison between the layout circuits and its schematics. The ERC to verify if the well and substrate areas have proper contacts and space to ensure correct power and ground connections. Also,

verifies the unconnected inputs and short-circuit outputs. The performed layout circuit can be visualized in the Section 5.4.

3.5 Future Biomedical Applications

All the knowledge acquired on this project report can be applied to several applications beyond the focus of the research project, which consists of self-powered WSN to eliminate the use of batteries.

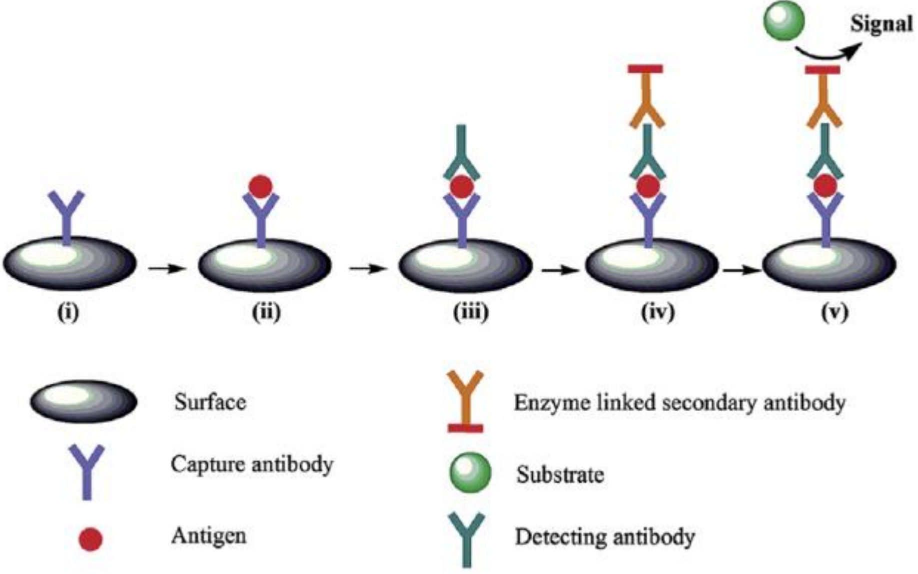

Figure 52: Schematic representation of a sandwich ELISA format, exemplification of a signal detection between a biomarker and substrate (Xuan Chen et al., 2019).

One possible application is their use on biomedical point-of-care devices, more specifically in electrochemical sensors. FET with a functionalized channel gate can detect electrochemical events. Redox reactions in the gate channel release electrons towards the FET channel, enhancing the output current. These fluctuations on voltage-current properties allow the detection of specific biomarkers and concentration, as shown in Figure 52. However, these voltage-current fluctuations are very small. Therefore, to further improve the FET performance, an electronic device needs to be implemented to amplify the signal, see Figure 53. That electronic device, such as a power management circuit, with the knowledge acquired during the project report, is suitable to assist the electrochemical sensor to improve its sensibility.

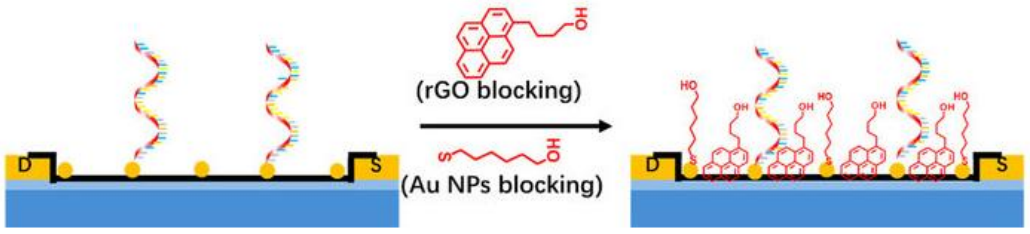

Figure 53: Schematic representation of a redox reaction detection on a functionalized FET gate, which the released electron activates a flowing current through the device. The amount of produced current is proportional to the binding reaction between the aptamer and the biomarker (Xiaoyan Chen et al., 2019).

CHAPTER 4 CONCLUSION

Energy harvester systems, although a very promising technology, it lacks the efficiency to power-up electronic devices without the need for batteries. An implemented solution for this problem consists of an adaptive power management circuit responsible for extracting and storing the scavenged energy efficiently.

The present work presents three main substantial contributions to the research. A robust voltage reference can generate a stable 258.35mV with a line sensitivity of 0.49%/V in response to a 1-3.2V voltage supply. It also presents a very good power supply rejection ratio of 58dB at 100Hz. During the simulation, and analysis to verify its robustness and performance is demonstrated. The designed circuit is suitable to provide bias voltage for low power operation.

A current starved VCO is demonstrated, to ensure and test its stability, the proposed voltage reference was set as a control voltage. It generates an average output signal frequency of 84.81kHz for 1-3.2V of the voltage supply. Although the voltage reference produces a dependent output voltage, the current starved VCO showed being capable of producing a local clock time to release the scavenged energy to an application.

A current reference output an average current of 41.5nA at 2V of power supply, with a 0.19nA/°C over a temperature range of -10 to 60°C. The TC demonstrated seems reasonable; it shows the capability to provide bias current for other circuits within the PMC.

Extensive research was conducted focusing the low power dissipation and output stability. The fabricated IC using a 130nm CMOS technology is ready for testing in a real piezoelectric energy harvester. The results upon the real testing will be compared with the simulated. Also, further improvements on the referencing circuits must be made, although they provide an appropriate bias to other circuits, its stability is a concern that needs to be solved.

The fabricated design has the purpose of being employed as an IC for energy harvesting interface for WSN applications.

The future work projected for this dissertation comprises in the application of the described theory in State of the art, more specifically the introduction of techniques at least in the current starved VCO, such as transistor stacking to decrease even further the leakage current associated to the sub-deep micron MOSFET. Also, the improvement of the referencing circuit, first more studies will be performed to understand even better the reason for the non-stability of the voltage reference related to temperature fluctuations. For the current staved VCO, another different topology could be implemented. Instead of

using the voltage reference to produce the current that limits the performance of the oscillator, a current reference could be used to perform the same purpose. Further chip testing will be performed to verify and test all the sub circuits and compare them to the simulation results.

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CHAPTER 5 SUPPORT MATERIAL

5.1 Fabrication Report (wafer Acceptance test and site report)

Wafer Acceptance Test and Site Report

Wafer ID: #5

VTI_N12_10_D13: 0.3533 V
IDSAT_N12_10_D13: 0.5231 mA/UM
IOFF_N12_10_D13: 137.1 pA/UM
BVDS_N12_10_D13: 3.5 V
VTI_N33_10_D35: 0.5808 V
IDSAT_N33_10_D35: 0.6034 mA/UM
IOFF_N33_10_D35: 0.2179 pA/UM
BVDS_N33_10_D35: 8 V
VTI_P12_10_D13: -0.3168 V
IDSAT_P12_10_D13: -0.2665 mA/UM
IOFF_P12_10_D13: -1840 pA/UM
BVDS_P12_10_D13: -4.3 V
VTI_P33_10_D30: -0.6204 V
IDSAT_P33_10_D30: -0.3025 mA/UM
IOFF_P33_10_D30: -0.6388 pA/UM
BVDS_P33_10_D30: -7.5 V
VBK_N12N1_7K: 10.93 V
VBK_N33N1_7K: 12.04 V
VBG_NB12_50_50: -3.951 V
VBG_NB33_50_50: -8.765 V
RSFV_NP_2_50: 8.277 OHM/SQ
RSFV_NPSAB_2_50: 285.3 OHM/SQ
RSFV_NDF_2_50: 7.613 OHM/SQ
RSFV_NWAA_20_5: 374.9 OHM/SQ
RCFV_NDF_D16_3542: 10.75 OHM/COUNT
RCFV_NP_D16_3542: 11.23 OHM/COUNT
VBK_P12N1_7K: -7.963 V
VBK_P33N1_7K: -9.815 V
VBG_PB12_50_50: 3.827 V
VBG_PB33_50_50: 8.642 V
RSFV_PP_2_50: 8.706 OHM/SQ
RSFV_PPSAB_2_50: 328.6 OHM/SQ
RSFV_PDF_2_50: 8.169 OHM/SQ
RSFV_NWST_20_5: 1133 OHM/SQ
RCFV_PDF_D16_3542: 10.3 OHM/COUNT
RCFV_PP_D16_3542: 10.51 OHM/COUNT
SPAFI_NDF_D21: 11.58 pA
SPAFI_NP_D18: 15 V
CONTI_NP_D13_96154: 5.183 OHM/SQ
VTFM1_N_10_D21: 12 V
SPAFI_PDF_D21: 6.667 V
SPAFI_PP_D18: 15 V
CONTI_PP_D13_96154: 5.926 OHM/SQ
VTFM1_P_10_D21: -12 V
VTI_NHV12_10_D13: 0.45 V
IDSAT_NHV12_10_D13: 0.4199 mA/UM
VTI_PHV12_10_D13: -0.402 V
IDSAT_PHV12_10_D13: -0.208 mA/UM
RCFV_V5_D19_3600: 0.5507 OHM/VIA
RCFV_V6_D19_3600: 0.5593 OHM/VIA
RCFV_V1_D19_3600_B: 0.5728 OHM/VIA
RCFV_V2_D19_3600_B: 0.5621 OHM/VIA
RCFV_V3_D19_3600_B: 0.5405 OHM/VIA
RCFV_V4_D19_3600_B: 0.5316 OHM/VIA
RCFV_V7/TV2D36_720_B: 0.358 OHM/VIA
CONTI_M6_D2_48502: 0.06411 OHM/SQ
SPAFI_M6_D2: 15 V
SPAFI_M7_D2: 15 V
CONTI_M7_D2_48502: 0.06542 OHM/SQ
SPAFI_M2_D2_B: 15 V
SPAFI_M3_D2_B: 15 V
SPAFI_M4_D2_B: 15 V
SPAFI_M5_D2_B: 15 V
SPAFI_M1_D18_B: 15 V
CONTI_M2_D2_48502_B: 0.06255 OHM/SQ
CONTI_M3_D2_48502_B: 0.07224 OHM/SQ
CONTI_M4_D2_48502_B: 0.06893 OHM/SQ
CONTI_M5_D2_48502_B: 0.05876 OHM/SQ
CONTI_M1_D16_72000_B: 0.09703 OHM/SQ
SPAFI_TM2_D46_B: 15 V
VTI_PLV12_10_D13: -0.2342 V
IDSAT_PLV12_10_D13: -0.3284 mA/UM
VTI_NLV12_10_D13: 0.2438 V
IDSAT_NLV12_10_D13: 0.6449 mA/UM

Wafer ID: #6

VTI_N12_10_D13: 0.3533 V
IDSAT_N12_10_D13: 0.5153 mA/UM
IOFF_N12_10_D13: 141.3 pA/UM
BVDS_N12_10_D13: 3.5 V
VTI_N33_10_D35: 0.5808 V
IDSAT_N33_10_D35: 0.5949 mA/UM
IOFF_N33_10_D35: 0.1429 pA/UM
BVDS_N33_10_D35: 8 V
VTI_P12_10_D13: -0.3283 V
IDSAT_P12_10_D13: -0.2613 mA/UM
IOFF_P12_10_D13: -1390 pA/UM
BVDS_P12_10_D13: -4.4 V
VTI_P33_10_D30: -0.6072 V
IDSAT_P33_10_D30: -0.3018 mA/UM
IOFF_P33_10_D30: -0.4851 pA/UM
BVDS_P33_10_D30: -7.5 V
VBK_N12N1_7K: 10.93 V
VBK_N33N1_7K: 12.04 V
VBG_NB12_50_50: -3.951 V
VBG_NB33_50_50: -8.765 V
RSFV_NP_2_50: 8.339 OHM/SQ
RSFV_NPSAB_2_50: 291.7 OHM/SQ
RSFV_NDF_2_50: 7.613 OHM/SQ
RSFV_NWAA_20_5: 375.4 OHM/SQ
RCFV_NDF_D16_3542: 10.75 OHM/COUNT
RCFV_NP_D16_3542: 11.59 OHM/COUNT
VBK_P12N1_7K: -7.963 V
VBK_P33N1_7K: -9.815 V
VBG_PB12_50_50: 3.704 V
VBG_PB33_50_50: 8.642 V
RSFV_PP_2_50: 8.769 OHM/SQ
RSFV_PPSAB_2_50: 331.2 OHM/SQ
RSFV_PDF_2_50: 8.228 OHM/SQ
RSFV_NWST_20_5: 1126 OHM/SQ
RCFV_PDF_D16_3542: 10.21 OHM/COUNT
RCFV_PP_D16_3542: 10.5 OHM/COUNT
SPAFI_NDF_D21: 11.48 pA
SPAFI_NP_D18: 15 V
CONTI_NP_D13_96154: 5.091 OHM/SQ
VTFM1_N_10_D21: 12 V
SPAFI_PDF_D21: 6.667 V
SPAFI_PP_D18: 15 V
CONTI_PP_D13_96154: 5.952 OHM/SQ
VTFM1_P_10_D21: -12 V
VTI_NHV12_10_D13: 0.444 V
IDSAT_NHV12_10_D13: 0.4145 mA/UM
VTI_PHV12_10_D13: -0.414 V
IDSAT_PHV12_10_D13: -0.1986 mA/UM
RCFV_V5_D19_3600: 0.5724 OHM/VIA
RCFV_V6_D19_3600: 0.5497 OHM/VIA
RCFV_V1_D19_3600_B: 0.5912 OHM/VIA
RCFV_V2_D19_3600_B: 0.5588 OHM/VIA
RCFV_V3_D19_3600_B: 0.5621 OHM/VIA
RCFV_V4_D19_3600_B: 0.557 OHM/VIA
RCFV_V7/TV2D36_720_B: 0.3693 OHM/VIA
CONTI_M6_D2_48502: 0.06312 OHM/SQ
SPAFI_M6_D2: 15 V
SPAFI_M7_D2: 15 V
CONTI_M7_D2_48502: 0.0669 OHM/SQ
SPAFI_M2_D2_B: 15 V
SPAFI_M3_D2_B: 15 V
SPAFI_M4_D2_B: 15 V
SPAFI_M5_D2_B: 15 V
SPAFI_M1_D18_B: 15 V
CONTI_M2_D2_48502_B: 0.05992 OHM/SQ
CONTI_M3_D2_48502_B: 0.07062 OHM/SQ
CONTI_M4_D2_48502_B: 0.06834 OHM/SQ
CONTI_M5_D2_48502_B: 0.06033 OHM/SQ

CONTI_M1_D16_72000_B: 0.09589 OHM/SQ
SPAFI_TM2_D46_B: 15 V
VTI_PLV12_10_D13: -0.2554 V
IDSAT_PLV12_10_D13: -0.3159 mA/UM
VTI_NLV12_10_D13: 0.2515 V
IDSAT_NLV12_10_D13: 0.6338 mA/UM

Figure 54: Wafer acceptance test and site report.

5.2 Layers Report

Statistics of Layers

Cadence Layer	Cadence Purpose	Stream Layer	Stream Datatype	Polygon	Rect	Path	Text	TextDisplay	Line	Dot	Arc	Donut	Ellipse	Pathseg
AA	drawing	10	0	26	435	0	0	1	0	0	0	0	0	0
NW	drawing	14	0	9	83	0	2	0	0	0	0	0	0	0
DNW	drawing	19	0	0	3	0	0	0	0	0	0	0	0	0
DNWTR	drawing	19	2	0	3	0	0	0	0	0	0	0	0	0
DG	drawing	29	0	1	7	0	0	0	0	0	0	0	0	0
GT	drawing	30	0	56	589	0	0	1	0	0	0	0	0	40
SN	drawing	40	0	14	165	0	0	0	0	0	0	0	0	0
SP	drawing	43	0	12	151	0	0	0	0	0	0	0	0	0
ESD1	drawing	41	0	0	3	0	0	0	0	0	0	0	0	0
SAB	drawing	48	0	56	0	0	0	0	0	0	0	0	0	0
CT	drawing	50	0	0	58609	0	0	0	0	0	0	0	0	0
MIM	drawing	58	0	0	2	0	0	0	0	0	0	0	0	0
M1	drawing	61	0	82	716	0	26	14	0	0	0	0	0	780
M2	drawing	62	0	69	185	0	5	0	0	0	0	0	0	280
M3	drawing	63	0	64	152	0	7	0	0	0	0	0	0	224
M4	drawing	64	0	30	76	0	43	0	0	0	0	0	0	44
M5	drawing	65	0	30	75	0	43	0	0	0	0	0	0	39
M6	drawing	66	0	30	57	0	43	0	0	0	0	0	0	39
M7	drawing	67	0	30	49	0	43	0	0	0	0	0	0	0
M8	drawing	68	0	28	56	0	43	0	0	0	0	0	0	21
V1	drawing	70	0	0	89128	0	0	0	0	0	0	0	0	0
V2	drawing	71	0	0	85576	0	0	0	0	0	0	0	0	0
V3	drawing	72	0	0	55198	0	0	0	0	0	0	0	0	0
V4	drawing	73	0	0	56068	0	0	0	0	0	0	0	0	0
V5	drawing	74	0	0	59949	0	0	0	0	0	0	0	0	0
V6	drawing	75	0	0	53152	0	0	0	0	0	0	0	0	0
V7	drawing	76	0	0	35914	0	0	0	0	0	0	0	0	0
PA	drawing	80	0	0	4	0	0	0	0	0	0	0	0	0
VSIA	drawing	63	63	0	0	0	323	0	0	0	0	0	0	0
DUMBM	drawing	90	0	0	2	0	0	0	0	0	0	0	0	0
BORDER	drawing	127	0	0	8	0	0	0	0	0	0	0	0	0
SUBD	drawing	131	1	4	28	0	0	0	0	0	0	0	0	0
ESDIO1	drawing	133	0	0	8	0	0	0	0	0	0	0	0	0
DSTR	drawing	138	0	0	2	0	0	0	0	0	0	0	0	0
MIMDMY	drawing	211	0	0	2	0	0	0	0	0	0	0	0	0
NFDMK	drawing	131	5	0	3	0	0	0	0	0	0	0	0	0

Figure 55: Statistics of the number of layers used on the layout the IC.

5.3 Circuit Schematics

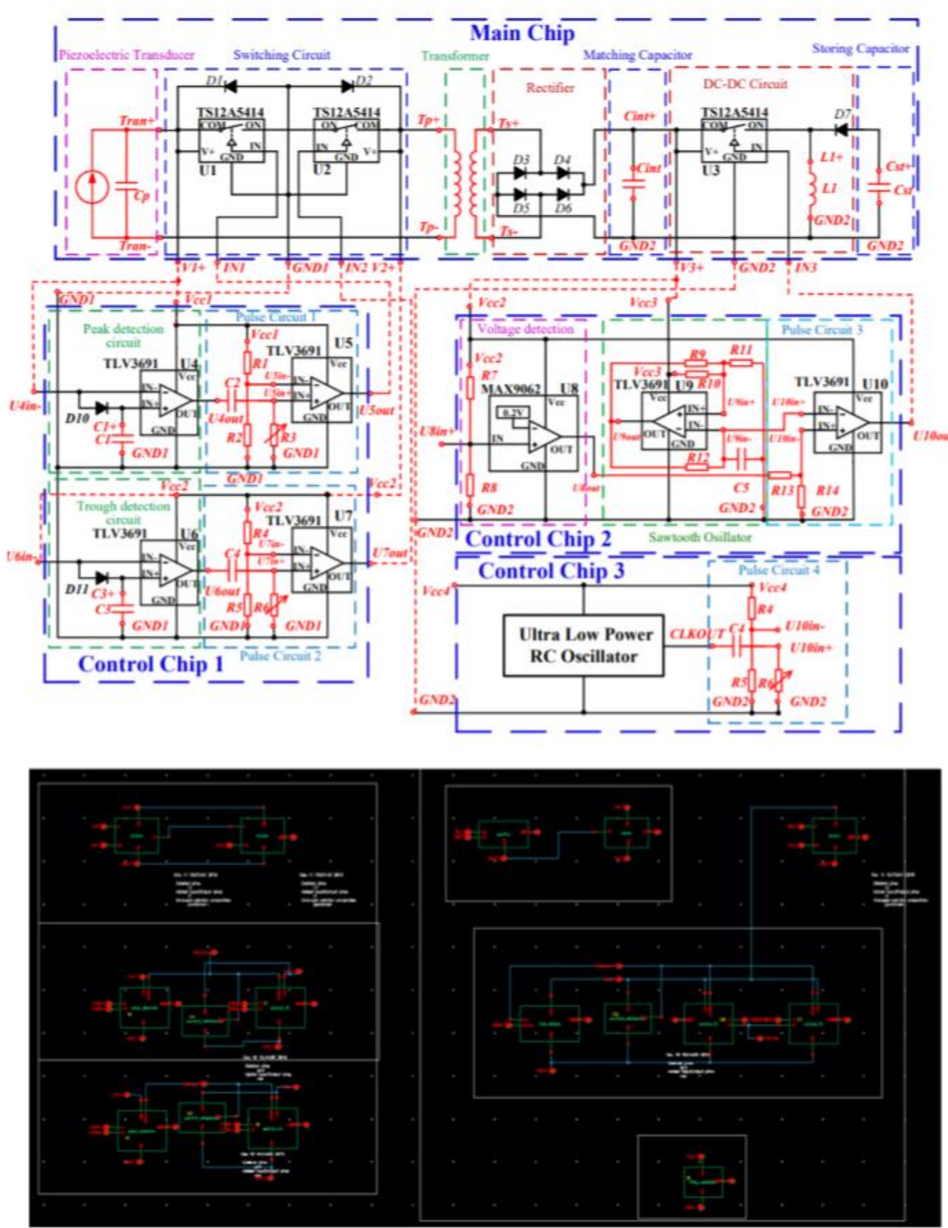

Figure 56: Complete circuit and its schematic in Cadence software.

5.4 Physical Layout

5.4.1 Ring Pads

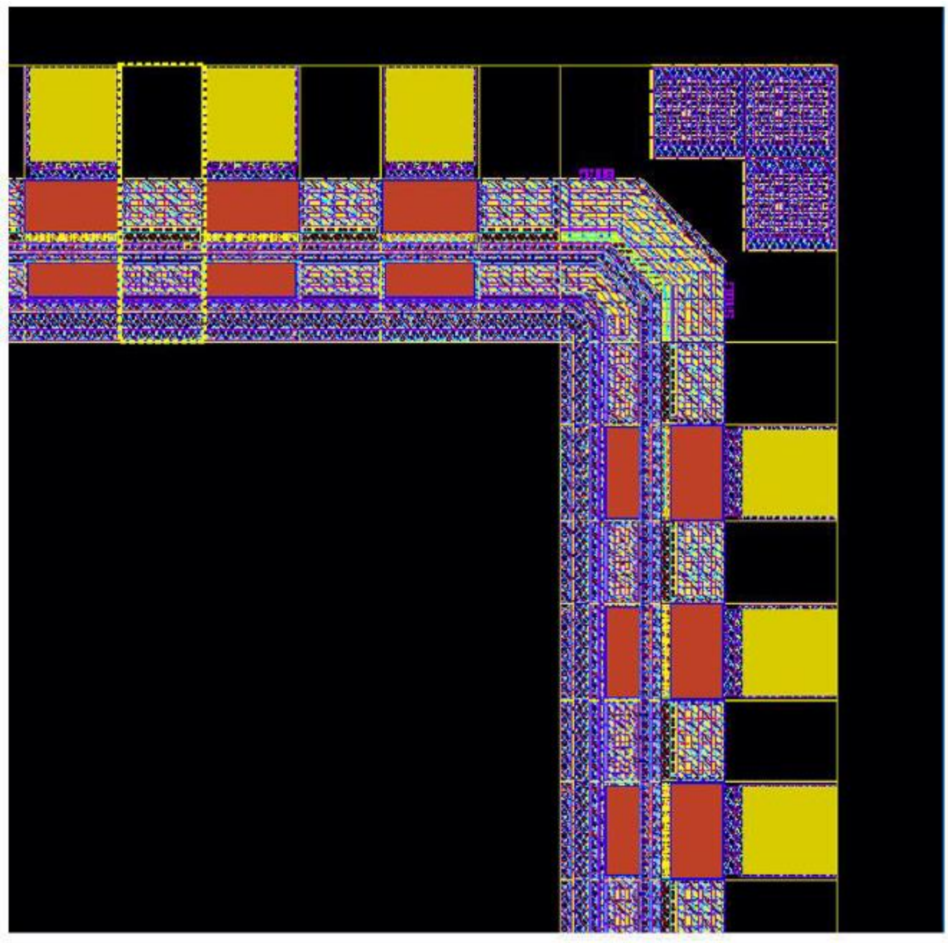

Figure 57: Layout of the ring pads provided by the external foundry.

5.4.2 Voltage Reference

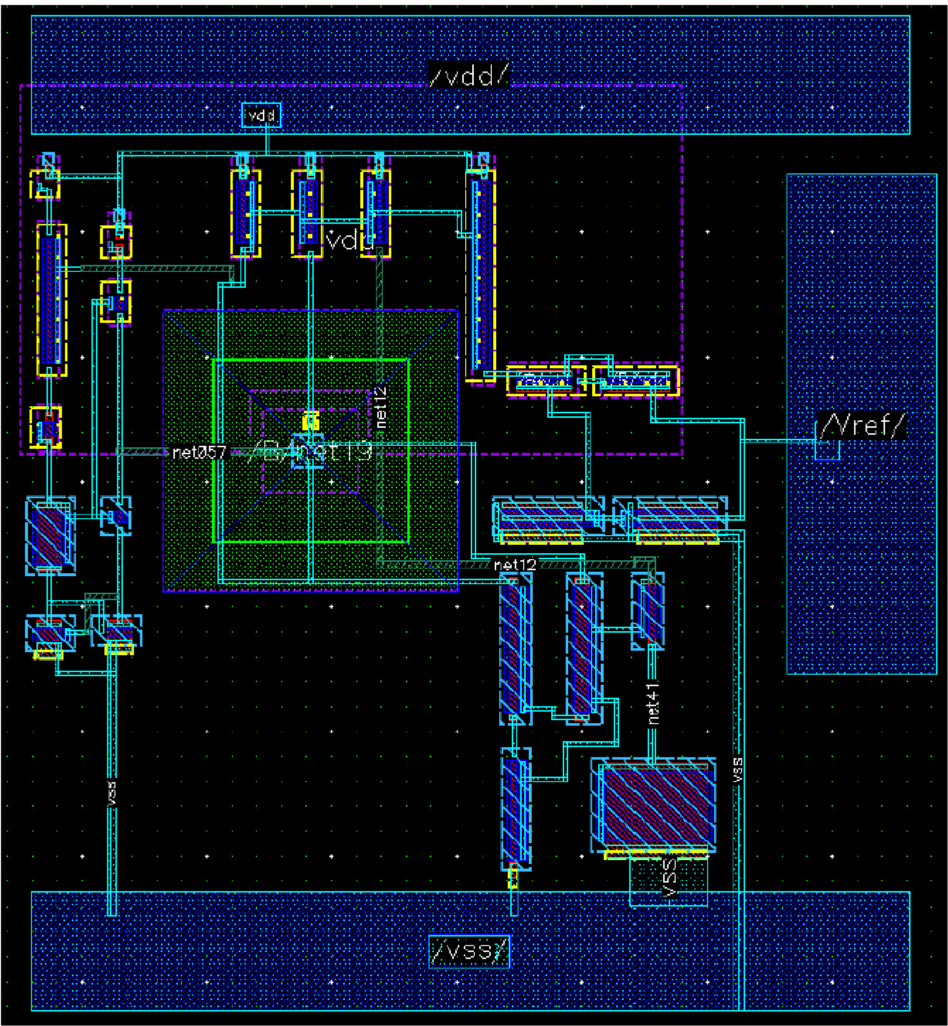

Figure 58: Layout of the developed voltage reference circuit.

5.4.3 Current Reference

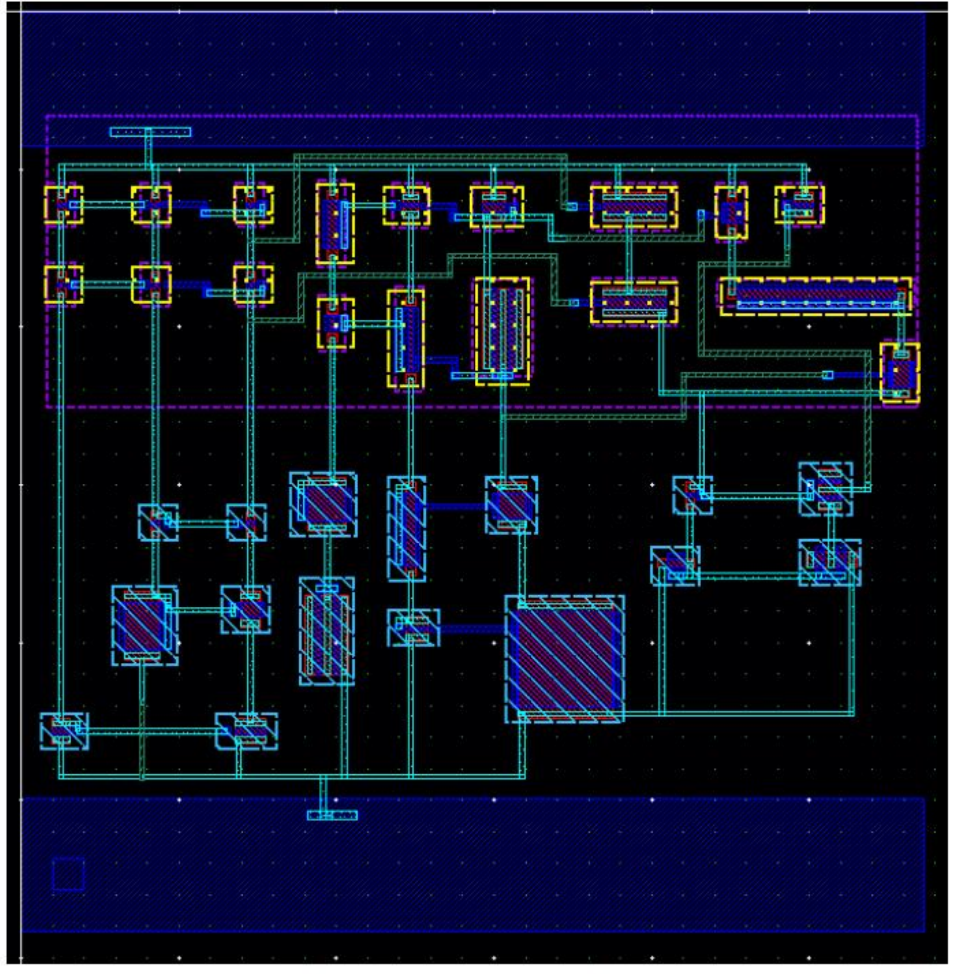

Figure 59: Layout of the developed current reference circuit.

5.4.4 Current Starved VCO

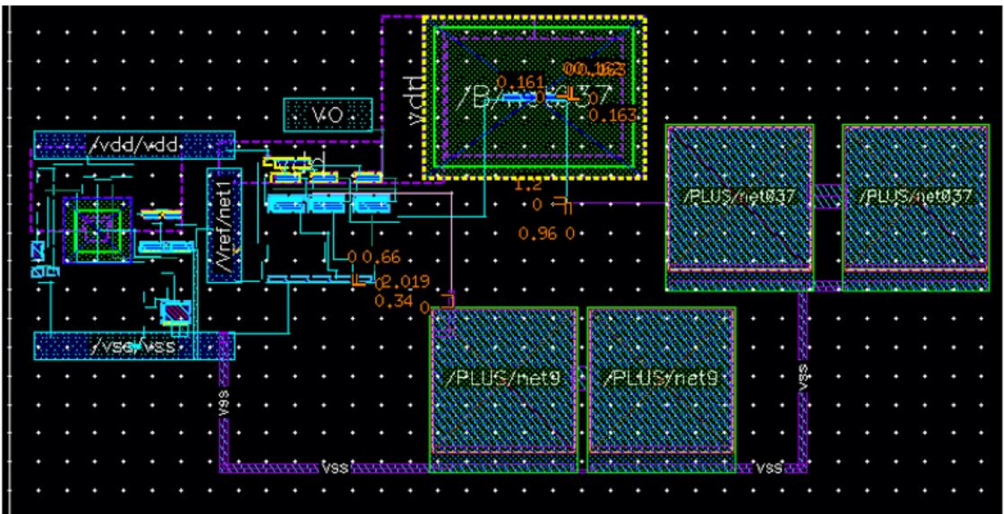

Figure 60: Layout of the developed current starved VCO.

5.5 Chip Photos

5.5.1 Overall Chip

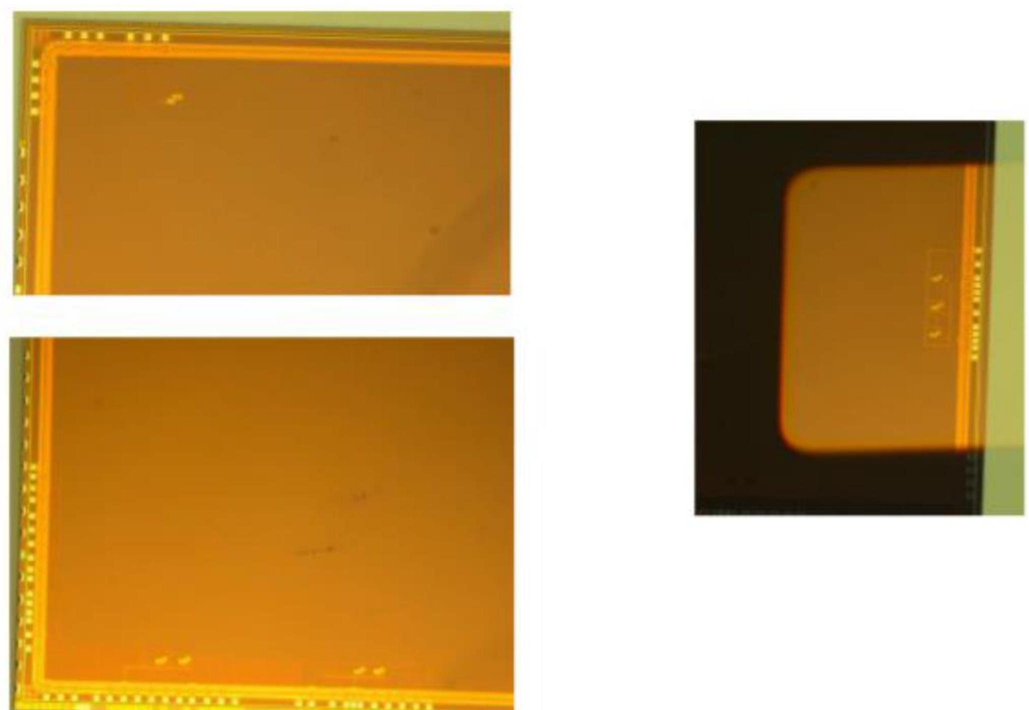

Figure 61: Implemented IC chip, under a microscope view, with 20 × amplification.

5.5.2 Pads and ESD protection

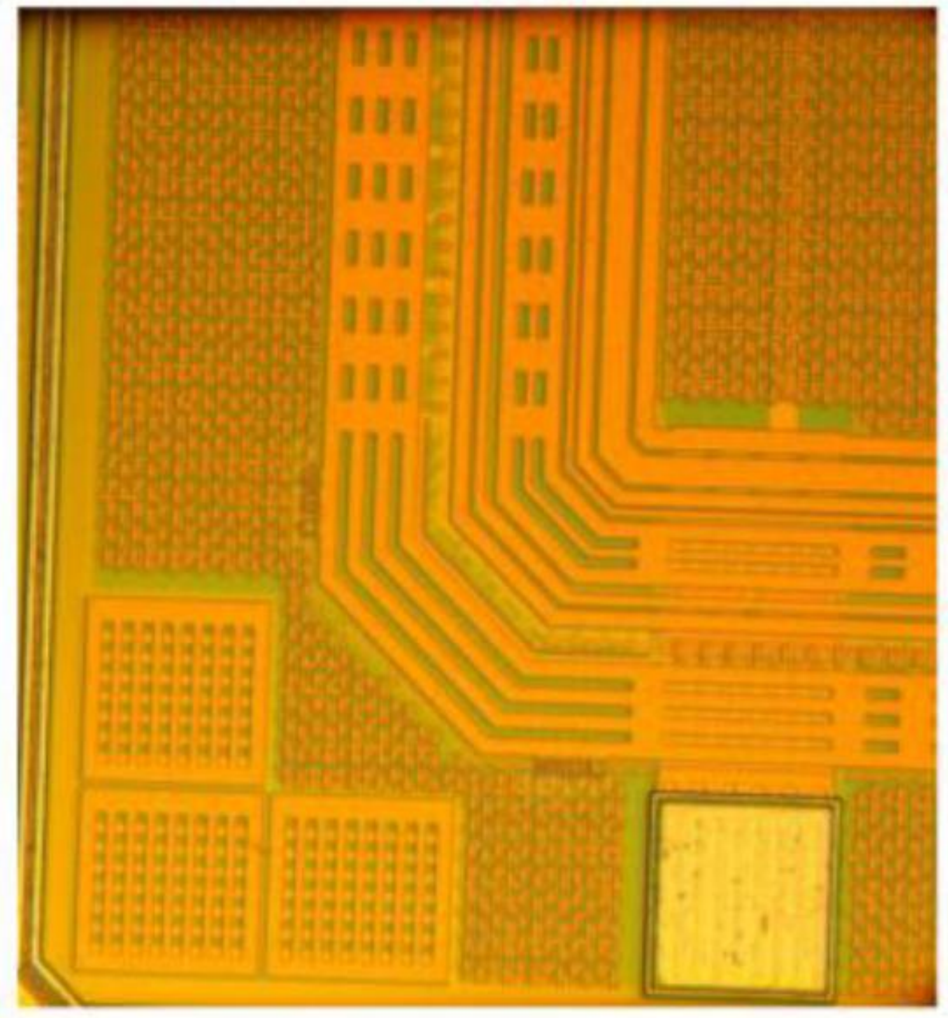

Figure 62: Microscope view of the pads and ESD protection with 100 × amplification.

5.5.3 Comparator Array 2

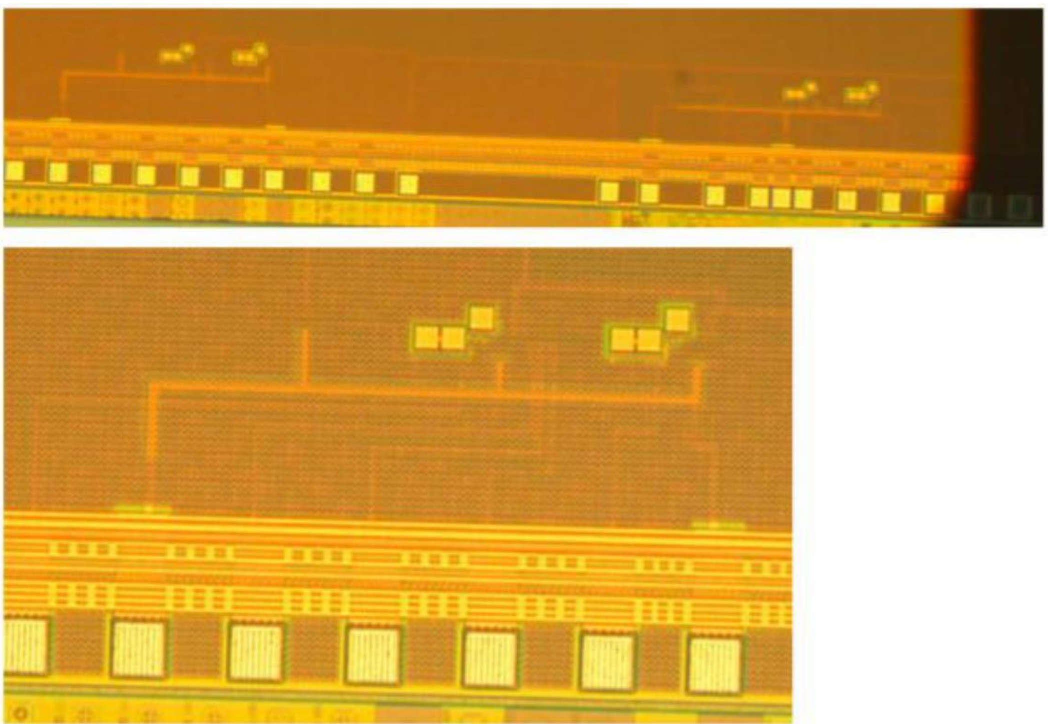

Figure 63: Microscope view of the voltage reference integrated in the negative input of the peak detector with 100 × amplification.

5.5.4 VCO (with Voltage Reference)

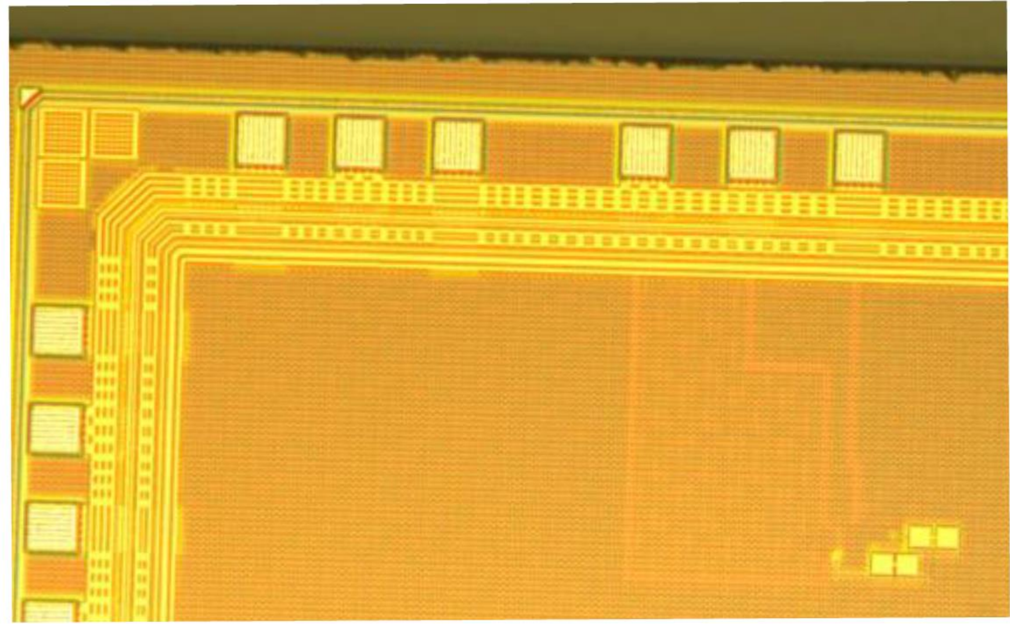

Figure 64: Microscope view with 100 × amplification of the voltage controlled VCO with integrated voltage reference.

CHAPTER 6 PUBLICATIONS

6.1 Paper 1

Goncalo Almeida, Zhaochu Yang, Paulo Mendes, Tao Dong*, CMOS Current Starved VCO for Energy Harvesting Applications, International Conference on Computing, Electronics & Communications Engineering 2020 (iCCECE2020), [Article ID:23]. STATUS: Accepted

6.2 Paper 2

Goncalo Almeida, Zhaochu Yang, Tao Dong*, Paulo Mendes, Yumei Wen, Ping Li, CMOS Current Starved VCO for Energy Harvesting Applications, IEEE Transactions on Electron Devices. STATUS: Under Review