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A Novel Single-Phase Shunt Active Power Filter Based on a Current-Source Converter with Reduced Dc-link

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Abstract. Nowadays, the majority of electronic equipment behave as nonlinear loads, introducing Power Quality (PQ) problems into the Power Grid (PG), namely, current harmonics and low power factor. These PQ problems contribute to the reduction of the efficiency of the transmission and distribution PG, as well as induce the malfunctioning of sensitive loads connected to the PG. Therefore, the development of equipment able to mitigate these PQ problems is extremely important. In this context, this paper presents a novel single-phase Shunt Active Power Filter (SAPF) based on a current-source converter, where the key differencing factor, when compared with the conventional approach, is the reduced dc-link. As the proposed topology requires a reduced dc-link, it represents a relevant advantage, since a typical current-source converter needs an inductor with a high inductance in dc-link, which results in higher losses, costs and component sizing. The proposed SAPF with reduced dc-link is introduced in detail along the paper and a comprehensive comparison with the conventional SAPF is established based on computer simulations. Besides, an experimental validation was carried-out with a developed laboratory prototype, validating the main advantages of the proposed SAPF with reduced dc-link.

Keywords: Current Harmonics, Current Source Converter, Shunt Active Power Filter, Power Quality.

1 Introduction

The shunt active power filter (SAPF) is used for power factor correction, for current harmonics elimination and, in case of three-phase systems, for current unbalances compensation [1][2][3]. In addition, as presented in [4] and [5], to mitigate the power quality (PQ) problems, the SAPF can also be used for interfacing renewable energy sources with the power grid (PG). Moreover, as presented in [6], in [7] and in [8], the functionalities of SAPF can be incorporated in electric vehicle battery chargers, representing a relevant contribution for the future smart grids, where the electric vehicle can be seen as a dynamic controllable load in the PG.

Concerning the structure of the SAPF, depending on the dc-link constitution, it can be classified as a voltage-source or as a current-source [9]. A comparison between both structures for simple applications of SAPF is presented in [10] and for applications of

electric mobility is presented in [11]. Since the focus of this paper is the current-source, a more detailed explanation is provided for this structure.

The current-source SAPF is composed by a coupling *CL* filter with the power grid and by an inductor in the dc-link. The dc-ac power converter is composed by semiconductors totally controlled such as MOSFETs, IGBTs or RB-IGBTs. These devices, in comparison with GTOs and BJTs, can operate with higher switching frequencies, requiring smaller output passive filters, translating into a more compact and cheaper solution. In addition, the input impedance is higher, which results in low power consumption [12]. However, when using IGBTs, it is needed to connect them in series with diodes, in order to ensure reverse-blocking, thus it is avoided that the current flows by the antiparallel-diodes of IGBTs. However, an alternative to this method consists in replace the IGBTs with the diodes in series by RB-IGBTs, which the use of diodes becomes unnecessary [13][14]. The current-source SAPF needs an inductor in dc-link with a huge value of inductance, which is necessary to reduce the ripple of the current for an acceptable value in dc-link.

The aim of this paper is to present a topology that allows the reduction of the inductance value of the inductor in dc-link. Moreover, the operation losses are reduced as well as the dimensions and the costs of the component are diminished. On the other hand, an inductor with reduced inductance value in dc-link allows a faster current control and thus, the average value of current can be minimized. In this context, the main contributions of this paper are: (a) A novel topology for a SAPF based on a current-source power converter with reduced dc-link; (b) A SAPF constituted by RB-IGBTs in the main inverter; (c) An experimental validation of the proposed SAPF.

2 SAPF with Reduced dc-link: Proposed Topology

As described in the introduction, the main contribution of this paper is the reduced dc-link of the SAPF. For this purpose, it is adopted a topology of a current-source inverter with a modified dc-link. This topology consists of a hybrid energy storage, composed by one inductor, one capacitor, two diodes and two IGBTs [15]. The conventional topology of a single-phase current-source SAPF based on RB-IGBTs is presented in Fig. 1, while the proposed single-phase current-source SAPF with reduced dc-link is presented in Fig. 2. As shown, the main differentiating factor of the proposed topology is the dc-link, however, also the coupling filter with the power grid is different from the conventional solution of CL filter [16]. Concerning the reduced dc-link, it is shown the dc-dc power converter in series with the single-phase current-source SAPF.

3 Proposed Control Algorithm

Concerning the simulation of the dc-dc converter, the first step consists in calculate the loads active power. By multiplying the load current by the fundamental component of the load voltage obtained through EPLL [17] algorithm it is obtained the instantaneous power, p. Subsequently, using a sliding average algorithm, it is possible to obtain the

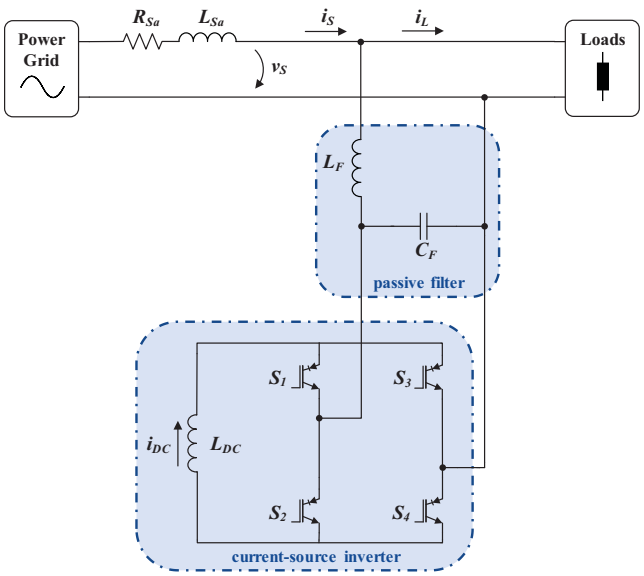


Fig. 1. Electrical schematic of the conventional single-phase SAPF based on a current-source inverter.

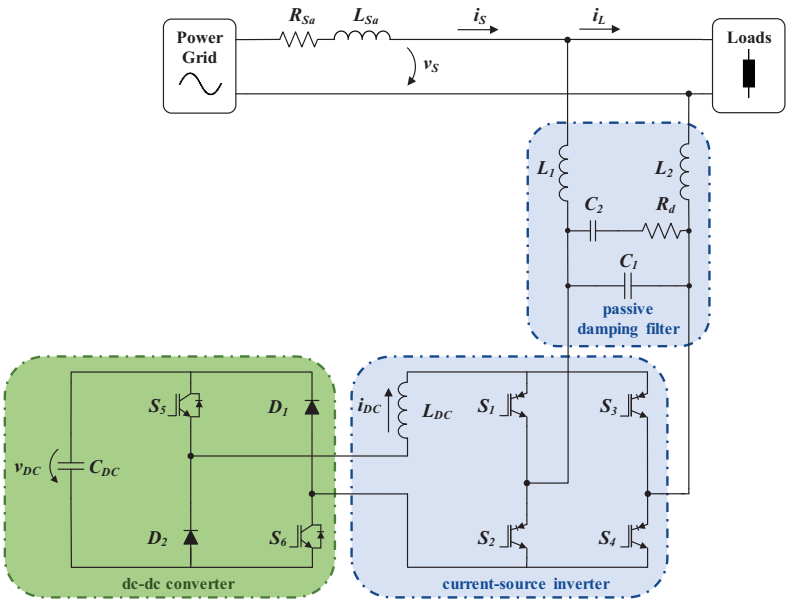


Fig. 2. Electrical schematic of the proposed topology of the single-phase SAPF based on a current-source inverter with reduced dc-link.

average value, $\bar{p}$. Then, the calculation of the oscillating component of the instantaneous power is determined by (1).

$$\tilde{p} = p - \bar{p} \tag{1}$$

After the calculation of the oscillating power, $\tilde{p}$, it is possible to obtain the reference voltage for the dc-dc converter, $v_{out}{}^{*}$, dividing $\tilde{p}$ by the current value measured in inductor of dc-link, i_{DC}, such as represented in (2).

$$v_{out}{}^{*} = \frac{\tilde{p}}{i_{DC}} \tag{2}$$

The modulation of the converter is performed with a fixed frequency of 40 kHz, with three switching states: $+v_{DC}$, 0 and $-v_{DC}$. If the reference voltage, $v_{out}{}^{*}$, is positive, both IGBTs S_5 and S_6 are enabled and the instantaneous voltage, v_{out}, is equal to $+v_{DC}$, whereas if the reference voltage is negative, the IGBTs S_5 and S_6 are disabled and the instantaneous voltage v_{out} is equal to $-v_{DC}$. The instantaneous voltage value, v_{out}, is zero when only one IGBT, S_5 or S_6, is enabled. The operation states of the dc-dc converter are presented in Table 1.

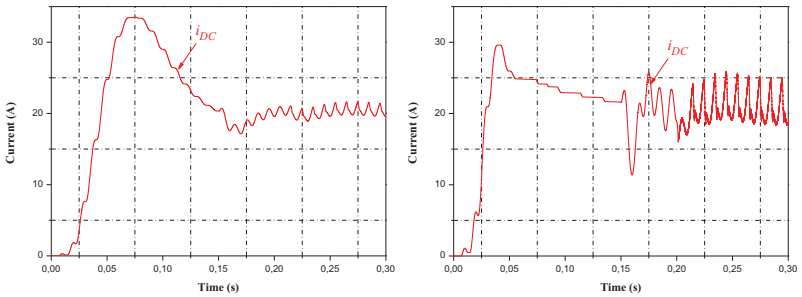
Table 1. Operation states of the dc-dc converter.

State	S_5	S_6	v_{out}
1	1	1	$+v_{DC}$
2	0	0	$-v_{DC}$
3	1	0	0
4	0	1	0

The proposed topology allows to reduce the inductance value of the inductor in dc-link of the inverter, since the dc-dc converter stores most of the energy which was stored exclusively by the inductor [15]. In order to understand the operation principle of the proposed topology, key computer simulation results were obtained for the conventional SAPF and for the proposed SAPF with modified dc-link, where were considered inductors, L_{DC}, of 200 mH and 50 mH, respectively. Fig. 3 shows the current in dc-link in both topologies, whose current regulation was made through a PI controller presented in [18], for a reference of 20 A. It is important to note that the gains of the PI controller influence the overshoot observed in both simulation results. As it can be seen, the current stabilizes for the required reference of current at the instant 0.25 ms.

Fig. 4 shows the voltage, v_{DC}, in the capacitor of dc-dc converter, where it can be observed that since the instant 0.2 s, the dc-dc power converter is activated and the capacitor, C_{DC}, starts storing energy with a maximum voltage of, approximately, 400 V. As part of the energy is stored in the capacitor, the inductor of the inverter does not need a huge inductance value, representing the key advantage of the proposed topology.

Considering both topologies, simulation results were also obtained to analyze the compensation of PQ problems. Therefore, at the time 0.22 s the loads are connected in both simulations. The loads connected are the same for both topologies. Fig. 5 shows the PG voltage, v_S, and the load current, i_L, where it can be observed that the current is delayed in relation to the voltage and presents a Total Harmonic Distortion in relation to the fundamental component, $THD_{\%f}$, of 36.45%.



(a) (b)

Fig. 3. Simulation results of dc-link current, i_{DC}, regulation: (a) Conventional SAPF;(b) SAPF with reduced dc-link.

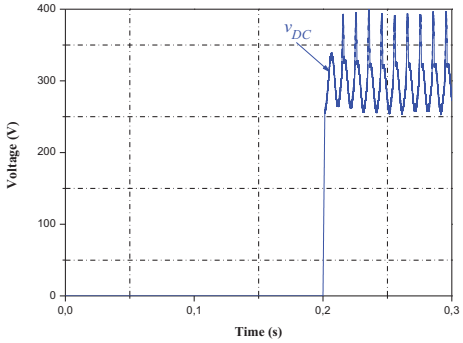


Fig. 4. Simulation result of the dc-link regulation of the proposed dc-dc power converter SAPF with reduced dc-link.

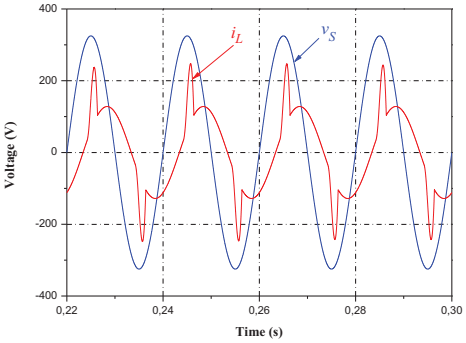


Fig. 5. Simulation results of the power grid voltage, v_S, and the load current, i_L, in both topologies.

As the current consumed by loads introduces current harmonics in the power grid, it is necessary the injection of the compensation current produced by the SAPF, which in this case is obtained through the Fryze theory [19][20].

Fig. 6 (a) shows the compensation current produced by both SAPFs. The behavior of Fryze theory can be proven by subtracting the current consumed by loads, i_L, by the

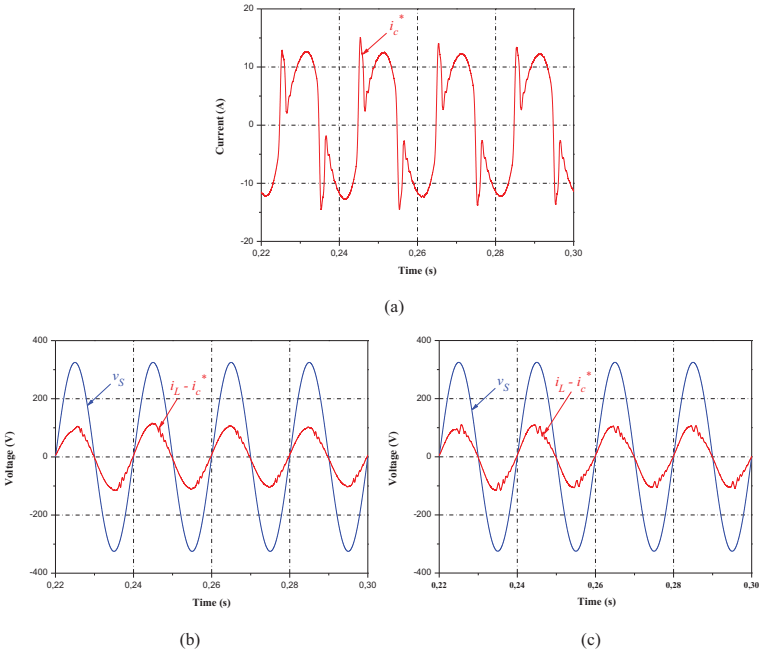


Fig. 6. Simulation results: (a) Reference compensation current produced by the Fryze theory, (b) Theoretical compensation current for the conventional SAPF; (c) Theoretical compensation current for the proposed SAPF with reduced dc-link.

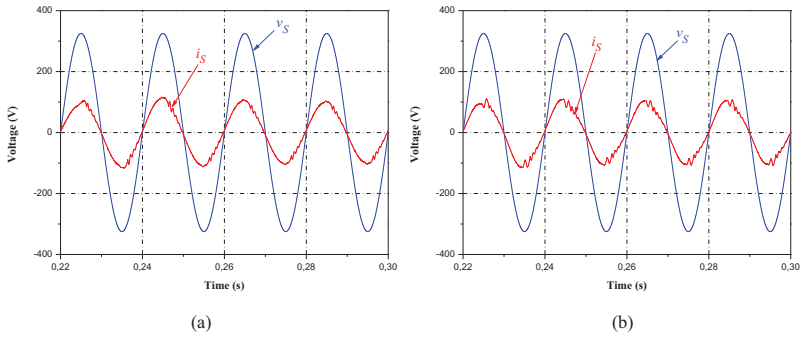


Fig. 7. Simulation results of the power grid voltage, v_S, and power grid current, i_S, after compensation: (a) Conventional SAPF; (b) Proposed SAPF with reduced dc-link.

reference compensation current, i_c^*, resulting in the theoretical current in the source, as it is showed in Fig. 6 (b) and Fig. 6 (c).

Finally, in Fig. 7 (a) are illustrated the voltage, v_S, and the current, i_S, in the grid after compensation for the conventional SAPF, where the $THD_{\%f}$ of current is reduced to 4.25%. On the other hand, as shown in Fig. 7 (b), with the proposed SAPF with reduced dc-link, the source current, i_S, is almost sinusoidal, presenting a $THD_{\%f}$ of 7.78%.

4 Evaluation and Comparison

With the help of the computer simulations, it is possible to compare the two topologies in more detail. In Table 2 are presented the inductance values used in both simulations, the $THD_{\%f}$ and the power factor (PF). As can be observed, the inductance of the inductor in dc-link used in the SAPF with reduced dc-link is four times lower in comparison with the inductor that composes the dc-link of the conventional SAPF. On the other hand, in both simulations, it is obtained a unitary PF. However, the $THD_{\%f}$ is somewhat higher than that obtained in conventional SAPF. Analyzing the simulation results, it can be concluded that the proposed topology has more advantages, once it was proved that it is possible to reduce the inductance value of the inductor in dc-link of the current-source inverter.

Table 2. Comparison between the conventional SAPF and the proposed SAPF with reduced dc-link.

Parameters	Conventional SAPF	SAPF with Reduced Dc-link
Inductance (mH)	200	50
$THD_{\%f}$	4.25	7.78
PF	0.99	0.99

Once validated the principle of operation of the proposed topology, a prototype of the dc-dc converter and the single-phase current-source inverter was developed (Fig. ***8***). Thereafter, are presented the main experimental results obtained for the proposed SAPF with reduced dc-link. The current-source inverter is composed by two legs with two RB-IGBTs (Fuji Electric, model FGW85N60RB) in each leg. In each RB-IGBT is connected a protection circuit against overvoltage. Besides that, in order to ensure the protection of the inverter, are connected varistors in parallel with the RB-IGBTs and with the dc-link, whose actuation voltage is of 510 V. On the other hand, the dc-dc converter consists of two IGBTs (Fairchild Semiconductor, model FGA25N120ANTD). The protection circuit of these semiconductors are similar to the RB-IGBTs of the inverter. In each leg, the IGBTs are connected in series with one diode (IXYS, model DSEP 29-12). For the dc-link voltage, it was defined a nominal voltage of 400 V and nominal capacitance of 100 µF, resulting in a dc-link composed by five capacitors of 20 µF (Vishay, model MKP1848C) in parallel. Moreover, it was developed three driver boards, two of them to actuate the RB-IGBTs and one to actuate the IGBTs of the dc-dc converter. The driver boards used to the current-source inverter generates the overlap-time needed for the correct operation of the inverter.

Fig. 9 shows the PG voltage, v_S, and the signal generated by the EPLL, v_{PLL}. It should be noted that the transient verified, shows that the output signal of the EPLL, v_{PLL}, rapidly reaches the synchronism with the PG voltage. Despite the PG voltage being distorted, the output signal of the EPLL, v_{PLL}, is sinusoidal and in phase with the power grid fundamental voltage, as intended.

To ensure the correct operation of the single-phase current-source inverter, it is necessary to establish an overlap-time between the two command signals. It is important to mention that only one superior semiconductor, S_1 or S_3, and inferior semiconductor,

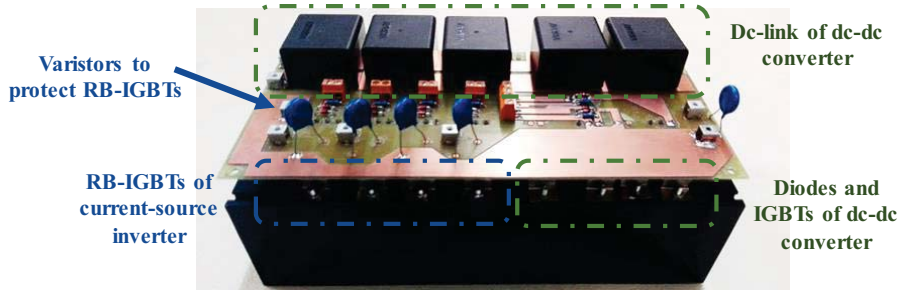


Fig. 8. Final prototype of the dc-dc converter and the single-phase current-source inverter fixed to heatsink.

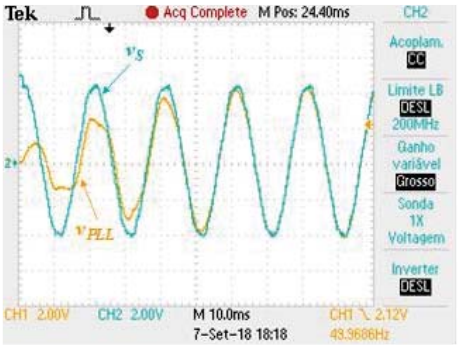
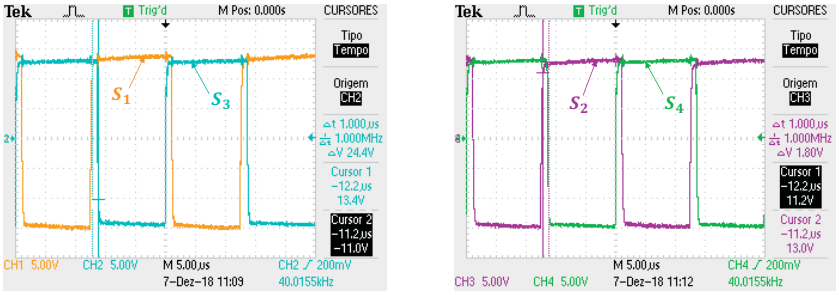


Fig. 9. Experimental results of the proposed SAPF with reduced dc-link: Synchronism of the EPLL, v_{PLL}, with the power grid voltage, v_S.



(a) (b)

Fig. 10. Experimental results of the proposed SAPF with reduced dc-link concerning the overlap-time between the gate signals of the semiconductors: (a) S_1 and S_3; (b) S_2 and S_4.

S_2 or S_4, are connected, except during the overlap-time. Therefore, when one of the superior semiconductors is open, the other superior semiconductor starts conducting, the same happens with the inferior semiconductors. In Fig. 10, it can be observed the overlap-time with duration of 1 µs between the two command signals.

In order to verify the effectiveness of the Fryze theory, it is calculated the theoretical current in the power grid side, subtracting the measured current in load, i_L, from the compensation current, i_c^*. Therefore, the theoretical current in the grid side can be

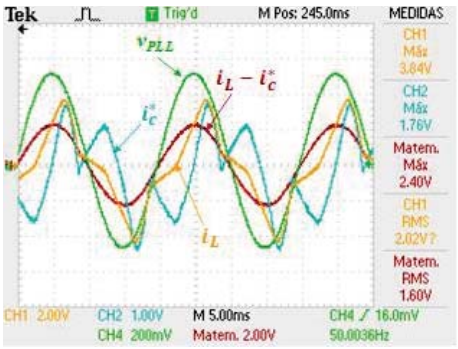


Fig. 11. Experimental results of the proposed SAPF with reduced dc-link concerning the Fryze theory: Load current, i_L; Compensation current, i_c^*; Theoretical current in the grid side, (i_L - i_c^*); Signal generated by the EPLL, v_{PLL}.

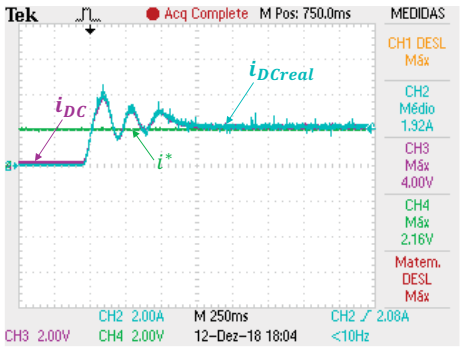


Fig. 12. Experimental results of the proposed SAPF with reduced dc-link during the dc-link current regulation: Reference current, i^*; Dc-link current, i_{DC}.

demonstrated through the MATH functionality available in oscilloscope, *Tektronix* TPS 2024, which allows the calculation previously described. Fig. 11 shows the theoretical current in source, (i_L - i_c^*), the load current, i_L, the compensation current, i_c^*, and the signal generated by EPLL, v_{PLL}.

After that, it was performed the regulation of the current in dc-link of the inverter, applying the PI controller. The performance of the PI control technique is validated for a reference current of 2 A. Fig. 12 illustrates the behavior of the current in dc-link, i_{DC}, where it can be observed that the measured current in dc-link, i_{DC}, after the initial transient, follows perfectly the reference current, i^*. For this reason, it can be concluded that the control technique has a good performance.

5 Conclusions

This paper proposes a novel current-source shunt active power filter (SAPF), aiming to reduce the inductance value, to minimize the costs, the losses and the dimensions of the system. Throughout the paper are described in detail the simulations realized, where it

was proved the possibility of reducing the value of inductance for a considerably low value. Moreover, this paper presents the operation principle of the dc-dc converter that has a crucial role in the proposed topology. Due to the hybrid energy storage strategy, part of the energy is stored by the capacitor of the dc-dc converter, and thus, it is not necessary a huge inductor in the dc-link. On the other hand, it is approached the power theory used for obtaining the compensation current produced by the SAPF. The developed prototype is presented and describe in detail. Finally, are presented the main experimental results, validating the operation of the proposed SAPF with reduced dc-link.

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