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Design, fabrication and integration of 3D micro-structures using self-folding techniques for ultra-miniaturization of smart microsystems

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Tese de Doutoramento em Engenharia Biomédica

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Resumo

Devido aos avanços recentes na área das microtecnologias, são cada vez menores as dimensões dos microdispositivos o que permite a sua utilização em aplicações até aqui impossíveis. Surgem assim, cada vez mais os dispositivos médicos implantáveis com potencial para introduzir benefícios significativos no âmbito do diagnóstico e do tratamento localizado. A integração de tais dispositivos é assim um processo muito complexo pois estes precisam de ser pequenos e biocompatíveis. Para tal, novas tecnologias de integração são atualmente investigadas para conseguir transformar projetos de investigação em produtos que podem ser produzidos em grandes quantidades em centros microfabricação. Na investigação, a integração manual de diferentes dispositivos é muito comum, dificultando muitas vezes o processo fabrico e a própria funcionalidade do dispositivo. Consequentemente, muitos projetos de investigação não avançam para a produção e o dispositivo nunca chega a ser utilizado para o fim que foi desenvolvido. A integração é então, um processo fundamental que afeta não só a funcionalidade do dispositivo mas também o seu processo de fabrico. Para tal, esta integração deve ser considerada desde o início de cada projeto para facilitar a escalabilidade do produto final.

Esta tese foca-se neste problema e teve como objetivo a criação de um processo novo para integrar estruturas 3D com substratos de silício. Utilizando apenas este processo a integração de sensores e atuadores complexos com os seus circuitos de controlo e gestão de energia é uma realidade. Este processo é obtido através da combinação de diferentes técnicas de fabrico de sala limpa. Utilizando técnicas comuns promove-se assim a escalabilidade do processo. Para obter tais estruturas o processo passa por três litografias e três eletrodeposições, seguidas de um processo de self-folding que converte padrões 2D em estruturas 3D. Para prova de conceito, um micro atuador 3D foi desenhado e simulado. A simulação elétrica, mecânica e térmica foi realizada para perceber todo o funcionamento do dispositivo. Após fabricação os resultados simulados são semelhantes aos resultados medidos. O micro atuador fora do plano foi fabricado em cima de um substrato de silício como requerido, permitindo assim que estes dispositivos sejam facilmente integrados com outros sistemas complexos. O objetivo desta tese foi concluído com sucesso e a sua principal contribuição foi a criação de um processo complexo para integrar estruturas 3D em cima de substratos de silício utilizando apenas técnicas padrão de sala limpa.

Palavras-Chave: Integração; Microfabricação; Self-Folding; Estruturas Tri-dimensionais.

Abstract

Recent advances in micro technology, are delivering complex devices that can measure and actuate in places that were thought unreachable. Implantable devices are a reality that will bring forth great, new opportunities in medical field, both in treatment and diagnostics. Such devices are required to be as small as possible, creating the necessity for new complex integration technologies that can be used in the industry. In research, the handmade *ad hoc* integration of different devices and different systems is quite common. When these very small devices need some reproducibility to be implemented at an industrial scale, such methodology does not work properly. Integration has, in fact, an important role in today's creations, because it will affect the device volume, characteristics, performance and its own fabrication process. In this way, the integration process should be considered a part of full devices' development process, since it will ultimately limit the achievable features.

This thesis addresses this problem and creates a new integration process to fabricate and attach 3D structures on silicon wafers. Such fabrication technology allows the integration of complex 3D sensors and actuators with their control circuitry and power management in a single process. The fabrication process gathered a lot of different cleanroom standard techniques that allow the scalability of the process into big fabrication centres. Three lithographies followed by three electrodepositions gave way to the device, and a new technology called self-folding, transforms the 2D patterns in 3D complex structures. For proof of concept, an out-of-plane 3D antennas and a micro actuator were designed and fabricated within this PhD. At last, the 3D actuator electrical, mechanical and thermal simulations were compared with the measurement results, leading to a very good match between them.

After the fabrication process, the micro actuator is out-of-plane on top of a silicon substrate, as intended. With such fabrication process, these devices can be easily tested and used in complex systems. The main objective of this thesis was achieved with success, delivering its main contribution: a complex process to integrate 3D structures on top of silicon substrates using only standard cleanroom techniques.

Keywords: Integration; Microfabriaction; Self-Folding; Three-dimensional Structures.

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List of Abbreviations

2PP	-	Two-Photon Polymerization
a-Si	-	Amorphous Silicon
ASIC	-	Application Specific Integrated Circuits
CAD	-	Computer-aided design
CMOS	-	Complementary Metal-Oxide Semiconductor
CMP	-	Chemical Mechanical Planarization
CNC	-	Computer Numerical Control
CPS	-	Coplanar Strip
CPW	-	Coplanar Waveguide
CVD	-	Chemical Vapour Deposition
DI water	-	De-ionized water
DRIE	-	Deep Reactive Ion Etching
DWL	-	Direct Writing Laser
EDX	-	Energy dispersive X ray Analysis
EFAB	-	Electrochemical Fabrication
FDA	-	Food and Drug Administration
FDM	-	Fused Deposition Modelling
FEM	-	Finite Element Method
FIB	-	Focused Ion Beam
GSG	-	Ground-signal-Ground
HDMS	-	Hexamethyldisilazane
IC	-	Integrated Circuit
INL	-	Iberian Nanotechnology Laboratory
IP	-	Inkjet Printing
IPA	-	Isopropyl alcohol
LCVD	-	Laser Chemical Vapour Deposition
LED	-	Light-emitting diode
LIGA	-	In German: Lithographie, Galvanoformung, Abformung (Lithography, Electrodeposition, Chemical Mechanical Planarization)

MEMS	-	Microelectromechanical system
NEMS	-	Nanoelectromechanical system
NMP	-	N-Methyl-2-pyrrolidone
PDMS	-	Polidimethilsiloxane
PE	-	Polyethylene
PECVD	-	Plasma Enhanced Chemical Vapour Deposition
PEEK	-	Polyether ether ketone
PMMA	-	Poly(methyl methacrylate)
PP	-	Polypropylene
PVD	-	Physical Vapour Deposition
RF	-	Radio Frequency
SEM	-	Scanning Electron Microscopy
SL	-	Stereo Lithography
SLM	-	Selective Laser Melting
SLS	-	Selective Laser Sintering
TMV	-	Through Mold Via
TSV	-	Through Silicon Via
UV	-	Ultra Violet

Chapter 1. Introduction

1.1. Implantable devices

The recent history of implantable devices begun in the 30's, where the first known attempts for the implantation of electrodes were used for muscle and nerve stimulation. In the middle of the XX century, the first telemetry systems, composed by batteries, coil antennas and sensors, formed the first fully autonomous integrated systems that could be implanted to measure simple things like temperature, pH and movements. Even so, these devices were big and hard to miniaturize, being only implantable at the surface of organs or below the skin. With the technological advances, and the appearance of MEMS in the 90's, the devices started becoming smaller at an astonishing pace, and the first microdevices started to appear. The miniaturization of ASICs with the inclusion of this first MEMS devices, brought a new trend in fabricating small devices that could be embedded in the human body. Applications like electrical stimulation of the nervous system and cardiac defibrillators, so called pacemakers, were the first to be implemented on the market. But this was just the beginning for the vast number of applications that the human body still requires from the micro biomedical devices [1].

Complex microdevices to be placed inside the human body need to be designed in a way that the power usage is as low as possible. Future devices will have to make a power management with energy harvesting techniques, but the developments in this field are still not satisfactory for every device. A good example is the work shown in [2], where the device is capable of measuring the vital signs of the human body, such as temperature, heart rate and ECG simultaneously. This device occupies an area of 16 mm^2 and is powered by a battery. This battery of 1.4 V with 3 $\mathrm{mAh/cm}^2$ is enough to power the device. Another good example related with the vascular system is presented in [3], where a full device measures the blood flow rate inside the veins. However, the electronic circuitry included on the ASIC is not fabricated with the sensing device. The consumption of the full device is really low, only 21.6 μW, and the full device occupies a chip area of 2.67 mm^2. This power, generally given by a battery, is enough for the device, but the implantability of the system gets compromised. Furthermore, the integration of both devices is

considered by the authors a big challenge for the future, where the main concern is related with the mechanical properties and the implantation procedure. A lot of complex devices offer solutions of energy harvesting, and wireless power generation with RF coils. The authors in [4] have developed an implantable intraocular pressure monitor that continuously measures and sends data to the outside world. In this device (Figure 1.1) there are three main components: the coil antenna made in a polyamide substrate, the MEMS capacitive sensor, and the stainless steel needle. They are assembled manually at the end of the fabrication, but a system like this would benefit largely if the integration was done in the fabrication process. Another example of wireless sensors is given in [5], where carbon nanotubes are the sensing component of the device and a connection to a wireless system with RFID is used. In the paper, it can be noticed that the size of the sensor is not comparable with the size of the electronic circuit. An integrated way to build these carbon nanotubes on top of an ASIC device should be developed and implemented.

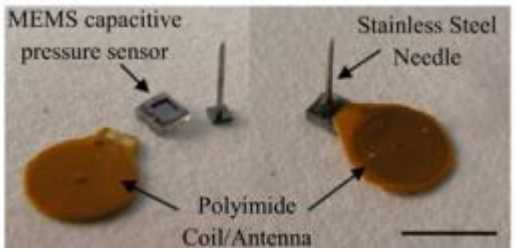


Figure 1.1. IOP measurement system, disassembled and assembled (Adapted from [4]).

These energy restrictions regarding energy harvesting and big power circuitry are a great concern, but when talking about implantable devices this is not the only matter to take into account. Biocompatibility is also an extremely important feature that every encapsulated device has to provide. Sometimes, these devices need to be embedded in the cellular tissue, and the natural reaction from the human body is to reject this strange material and to expel it. In [6], the authors use PDMS encapsulation to create an implantable device to be placed in the eye with drug delivering mechanisms fabricated with MEMS technology. This encapsulation is made with silicon molds to define the PDMS and, in the end, the device is encapsulated with PDMS-to-PDMS bonding. Another example of the use of this material, is in [7], where a probe was created to record neural signals and deliver drugs in the same device. This device, made in silicon technology, was covered with PDMS to ensure biocompatibility with the brain cells. The results achieved with such device are viable and the device works as planned, so it begs the question: “why is this not on the market?” The answer lies in the fact that this device is composed of only the sensor/actuator module. All of

the control electronics are placed in a board that is not small enough to be implanted in the human head. In conclusion, integration and encapsulation of such MEMS with the ASIC would be a fundamental future work for these biomedical devices.

Parylene is a widely used FDA approved biocompatible material for the encapsulation of several devices. A novel fabrication process is shown in [8], where MEMS and parylene are integrated in a flexible device. The junction of such techniques allows the creation of flexible arrays of sensors compatible with the human body and with big potential applications in the medical field. Intraocular devices to measure pressure are also a reality with such material [9]. Parylene presents itself as a great option to encapsulate all these different MEMS and electronics, and turn them into biocompatible machines [9]. In [10], the authors created a device to study the optogenetics of the brain tissue. This device in completely portable and wireless, but its assembly is not perfect and the device occupies a lot of volume. Big academic research can be found on the implantable devices research field, and most of them with high quality results in measurements and actuation, but most of them are not fully integrated and ready for production.

Integration ends up being the “holy grail” in the development of medical microdevices. There are thousands of MEMS ready to measure and actuate over hundreds of different variables that exist in the human body. But in most of them, the problem comes when these MEMS need to be connected to complex electronic circuits. In academia research, the manual apparatus of connecting wires and gluing different devices is a standard, and with that the full devices become unscalable and hard to translate to mass production. With this mindset, the devices can be extraordinary at detecting molecules or controlling electrical signals, but they will never be used in final products because their fabrication processes didn’t include integration techniques with other components.

In conclusion, integration needs to be pursued from the beginning of a project that aims to create stable and scalable miniature devices, allowing them to revolutionize the implantable systems market.

1.2. Thermal modulation microdevices

Recent advances in technology have been paving the way to new medical integrated solutions for the treatment, diagnosis and prevention of diseases, and even for the replacement of human body functions. Such technological advancements, like miniaturization and low power consumption technologies, took research fields to a new level where microdevices are now capable of reaching so-far inaccessible places. Fully-implantable microsystems are becoming a reality and their growing market is expected to reach more than $54 billion in value, until 2025, in developed countries [11]. These implantable devices could have hundreds of different usages, including diagnosis or treatment of various neurological disorders, cardiovascular problems, and ophthalmologic diseases [12]. The nervous system can greatly benefit from this technological progress, where microdevices should be able to measure and actuate on single neurons, treating and providing new information from locations that were previously unreachable [13], [14].

Neuromodulation consists in the control of neural cells' behaviour, and includes every approach that changes the neurons' biochemical process or electric signals. This is achieved by suppressing or facilitating the flow of action potentials to accomplish a specific brain function. In this context, thermal neuromodulation may play a significant role. An earlier work from Baldwin and Frost (1956) [15] reported that cooling the brain to 30°C or below was effective at suppressing electrical discharges on brain cells, and could stop strong electrical signals, such as seizures. Many other studies followed: for example, thermal regulation resorting to cooling, also known as hypothermia, was tested to treat insomnia [16], and is also used on a more regular basis to prevent brain injuries and traumas after strokes [17], or on newborns to prevent serious brain injuries [18]. Overall, epileptic seizure suppression was the main application of brain cooling and will be the main focus of the project were this thesis is inserted.

Epilepsy affects more than 50 million people worldwide, and 30% to 40% of patients are not responsive to antiepileptic medication [19]. Thus, thermal neuromodulation presents itself as an alternative solution for this group of patients, reducing the electrical signals before the seizure intensifies can be a solution to suppress it. This method is already used on site when performing brain surgeries: a cold liquid (0°C) is poured on the brain's surface to suppress epileptic seizures that can randomly start. Cooling the brain is, therefore, one of the quickest and most effective responses available to quickly stop a seizure. Consequently, developing a small device capable of

detecting and suppressing electric signals that can be implanted on the brain is a technological solution of interest for the chronic control of drug-resistant focal seizures. To suppress seizures, a temperature of around 20 to 30°C or less is required [15], [20]. In this way, the device must be able to reduce the tissue's temperature by at least 7 to 17°C, considering that the brain's temperature is around 37°C. In order to be safe, this device has also to maintain temperatures within safety limits of biological tissues, which implies that it shouldn't surpass 43°C and the cooling shouldn't go below 0°C [21], [22]. Going out of this temperature range can lead to irreversible thermal damage. Additionally, cooling for long periods of time can reduce the motor function of the whole body and, in extreme cases, it can also cause pneumonia [23]. In the literature, small systems for thermal modulation in the brain have been reported to produce good results. Rothman and his team were some of the first authors proposing the use of focal cooling to terminate seizures, and have published the evolution of their work based on different devices. However, all of them required water to cool down the system [24]–[26]. In a different kind of device, Ahiska made a complete model of a thermoelectric helmet that can cool down the brain in a non-invasive way. Nevertheless, and much like the previous device, water was required to cool down the hot side of the Peltier modules [27]. In his review, Fisher presented a way of cooling the brain with only a small implanted Peltier module. However, since no proper heatsink was used to cool down the thermoelectric module, after turning off the Peltier module, the heat from the hot side would dissipate in the rat's head, damaging its cells [28]. In 2011, Hou and his research group developed an integrated wireless system to cool down and stop seizures in the brain. This system required no batteries and was powered resorting to wireless power transfer. The paper presents good results in terms of communication between the device and the external source of power, but it is difficult to understand the accomplished brain cooling results. One main conclusion that can be made is that the wirelessly-transmitted power was not enough to stop seizures [29]. Another example comes from Fujji and his fellow researchers, who have developed one of the most advanced systems for brain cooling. Their approach was based on the use of a small Peltier together with water cooling to achieve the desired tissue temperature. Such device was able to cool the brain tissue down to 10°C without causing any damage to the cells. Consequently, seizures below the focal points were completely terminated. The system was tested and placed in rats' brain cortex [30]. Furthermore, there are also examples of devices that do not use Peltier modules to reduce the temperature. Cooke and his research group used PDMS tubes to circulate cold water and cool down the cells. In their research, two types of devices were developed: one to place on the surface of the brain and

another to place in the brain grooves, also known as sulcus [31]. The previously presented studies were focused on the effectiveness of the focal cooling and did not target cheap and small devices that can be used in vivo, as they had large cooling modules with considerable areas that were not portable and were impossible to implant in the brain. To sum up, despite its reported benefits, thermal neuromodulation is not used as much as expected since the available cooling devices are generally too large for practical use [32]. Such devices are far from being suited for permanent use in humans, or for testing with monkeys or rodents.

1.3. Integration and miniaturization technologies

Over the last decade, miniaturization became one of the most dominant areas in the device fabrication research field. Building a device that is small enough to directly interact with micro objects such as cells, and that also has the significant advantages and capabilities of devices in the millimetre scale, presented challenges that were surpassed in the 90's. The Microelectromechanical Systems (MEMS) business is a billion-dollar market that ascends to 17 billion dollars in the whole world [33]. This technology brought us the capability to actuate and sense with complex devices that can be produced in the micro scale. There are uncountable works in this area, proving that MEMS are here to stay and that they will dominate the technology in our life. Unfortunately, when translating these researches to market products, some major complications appear and most of them are related with the integrability of these devices with other technologies. This interconnection between several microdevices is a significant constraint when moving the device prototype to the production scale, if the integration was not well implemented [33]–[35].

Generally, complex microdevices for sensing or actuating require the usage of controllers, energy systems, and other circuitry. These circuitries are fundamental components, and without them, our smartphones, smartwatches, and other devices would not exist. For these integrated circuitry (ICs)' fabrication, the technology followed Moore's Law, which stated that the density of transistors doubled every two years of development. This law was accurate for a long time, but the rate at which the number of transistors increased slowed down in the most recent years. Shrinking down the transistor gate is now more challenging, and unreachable physical limitations in fabrication technologies make it impossible to respect Moore's prediction, as they lead to higher

costs and longer development times. Nevertheless, this law never considered the existence of other components that are not in the ICs' category [36].

The increasing demand for miniaturization and integration of complex devices does not grow at the same rate as transistors, so this gave origin to the "More than Moore" law. This new trend considers the integration not only of transistors but also of complex devices like MEMS. The concept of small complex devices that use different technologies like radio frequency (RF) circuitry, sensors and actuators integrated with IC's, became one of the main themes of discussion and generates billions of dollars every year [36]. This idea created the term Multi-Chip-Module, where different chips are included in the same package. There are already complex devices present in our smartphones and computers, but most of them follow a 2D packaging configuration. This 2D technology inherently results in undesirably big devices, which, in cases like biomedical applications, renders them unusable. The research field is so focused on achieving almost perfect sensing and actuation devices that generally the integration is ignored, and this ends up being fatal on the scaling process of creating new market products.

The encapsulation of a device implies dicing and assembling the obtained die with the remaining components that were fabricated with other techniques [35]. This originates a big impact on the final device characterization and testing, because both reliability and performance can be deeply affected. On the other hand, integration pushes this encapsulation to a more precise junction of different devices. The integrability of complex devices received a lot of visibility and this new emerging research field gained a lot of attention. Following this new trend, the 2.5D and 3D integration technologies became a major topic of discussion. These new technologies consider that the devices can grow in other directions and extending this integration in the z-axis provides a breakthrough in device packaging [33], [34], [37].

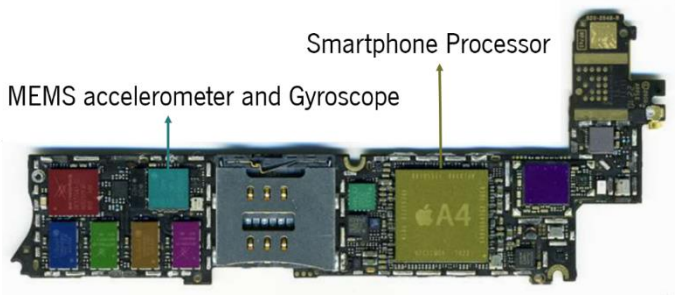


Figure 1.2. Smartphone logic board where different devices can be seen (Adapted from [38]).

In **Error! Reference source not found.** a logic board of a common smartphone is showed here, a MEMS gyroscope and accelerometer (blue square) are fully packaged and integrated with their own ICs. This small device is integrated in a large system and is indispensable for these smart devices that we use every day.

1.3.1. 2D and 2.5D Integration technologies

2D packaging is the most common process to integrate IC's with other circuitry or MEMS. In this method, three special cases can be acknowledged: board-level integration, chip-level integration and wafer-level integration. The board-level method is majorly done when the integration of the MEMS device and the application specific integrated circuits (ASIC), in the process flow was not possible or considered. This is the most common integration method and it can increase the complexity in the devices' testing. As it is shown in Figure 1.3, the MEMS and the IC are not connected between them, being only integrated by a bridge that transfers, controls and connects the signals between them. These bridges can be PCBs or even silicon dies specifically designed for this connection. Another important thing to notice on this method is the possibility of having different interconnection technologies, as shown in Figure 1.3. The IC is connected with flip-chip bonding, where small solder balls are aligned with the substrate, creating an electrical connection [34], [39]. The MEMS device is connected by wire-bonding. After the two are integrated in the same substrate, the devices are generally covered by mold compound. Using flip-chip technologies, the device is ready to be used or integrated with more complex systems.

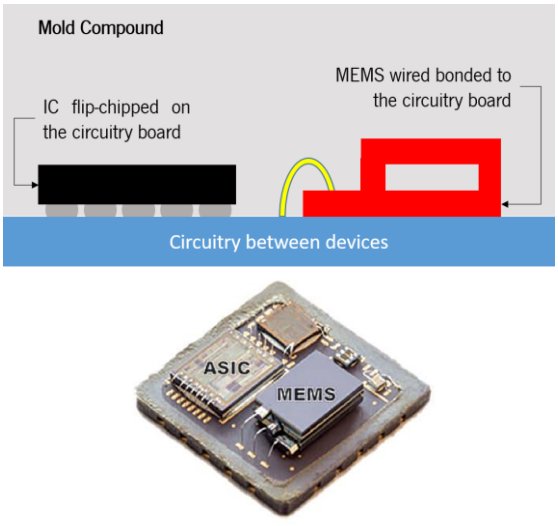


Figure 1.3. 2D Integration of a complex accelerometer developed by: Colibrys Ltd [34].

The chip-level 2D approach is similar to the previously referred one. In this case, the two devices, the MEMS and the IC, are placed next to each other, and wire bonding is used to make the electrical interconnections more reliable and more precise (Figure 1.4). But the integration step has to be considered before processing each one of them in order to get a compatibility between devices without the need of a bridge. The devices are then covered by a mold compound, making them solid to integrate with other devices and chips [34], [39].

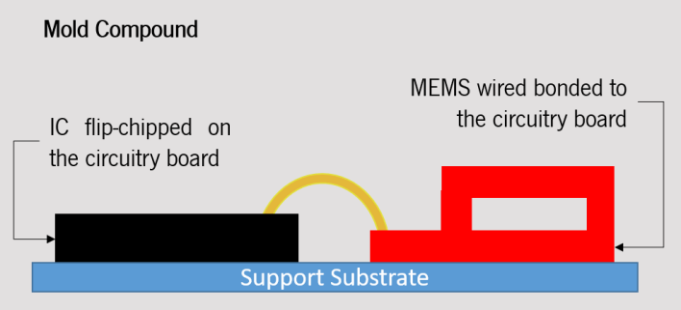


Figure 1.4. 2D Chip level integration of the MEMS and IC [34].

The 2D wafer-level integration is done by fabricating the IC and the MEMS device in the same wafer. In this side-by-side process, the two devices are built at the same time but in different positions. With such process, a high level of integration is achieved. Generally, the layers used in CMOS technologies are not compatible with the layers used in MEMS fabrication, meaning that planning a side-by-side integration is hard and dispendious.

2.5D integration resorts to the same idea of the circuit board approach in 2D, but the connection substrate is made with a silicon interposer. Because this technique uses the z-axis as a direction of integration, it gets called 2.5D integration. In fact, it is quite similar to 3D packaging, but it is done in a way that an interposer allows the connection between the two devices. The interposer generally exists to create the missing compatibility between the IC and the MEMS. In this interposer, Through Silicon Vias (TSV) are used to make the interconnection between the different components of the system, allowing the integration of several devices in a single package. This interposer can be used not only as shown in Figure 1.5, but also between the different stacked elements, providing the pitch mismatch of connections between them [34], [40].

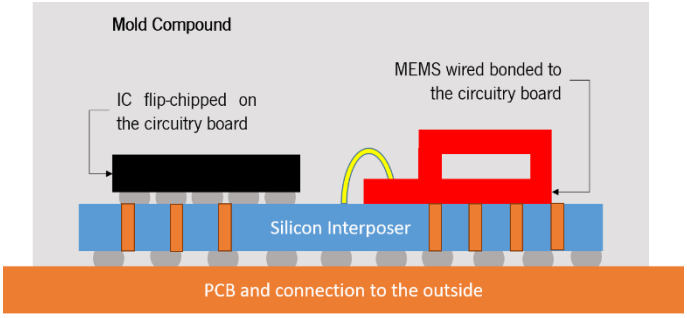


Figure 1.5. 2.5D Integration of a device and an IC with a silicon interposer as described in [40].

1.3.2. 3D Integration technologies

Since integration became a major research field, reliability, reproducibility and precision were increased. 3D stacking of devices became a major integration opportunity to fabricate complex microdevices that have multiple chips interconnected with each other. This method is the one with less electromagnetic noise, because it allows the minimization of the distance between circuits and mechanical elements. Another big advantage of this technique is the miniaturization of devices in the x and y axis. There are two main 3D stacking options that provide fully integrated microdevices: monolithic integration and device bonding [39].

Monolithic integration can be described as wafer-level packaging, since in this technique the same wafer is used to fabricate all of the devices. It can be divided into two types of integration [39]:

- Post-Process integration: The MEMS device is built on top of the IC component;
- Pre-Process integration: The MEMS device is the first to be fabricated and, the IC is fabricated on top of it.

Wafer-level packaging is definitely the most interesting technique when the quality of the device needs to be preserved. The interconnections are the best in all of the processes, creating less noise and presenting good reliability. A good example of post-process integration is described in [41], where the authors make a 3D MEMS structure on top of a CMOS wafer without dicing the wafer in the middle of the process (Figure 1.6).

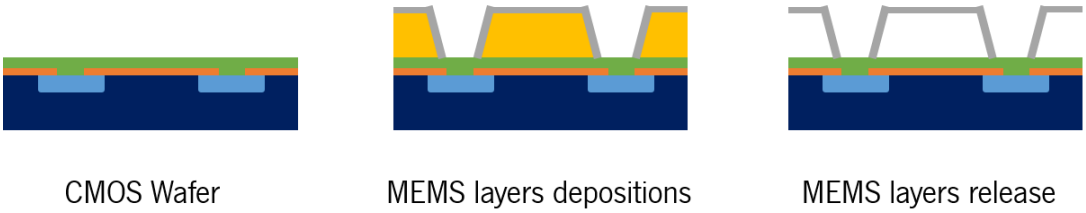


Figure 1.6. 3D Wafer Level Integration of a device and an IC as described in [41].

Device bonding is also a promising technique that can be done at both the wafer-level and the chip-level. Device bonding is based on bonding techniques between different or similar substrates. These techniques make use of two different processes to fabricate two different devices. In the end, the two devices are connected by bonding techniques. The production of different devices can be useful when the same cleanroom cannot produce, for example, the CMOS and the MEMS device. Still, the full process needs to be integrated in the design of the devices, in fact, this is the main concern when 3D stacking integration is required. The full device needs to be thought from the integration perspective before thinking on the other process flow steps. This is one of the first steps because the alignments between the devices is now a critical point whereas, in the 2D and 2.5D integration mechanisms, the alignment was not critical because the devices were integrated with bridges for interconnection.

A good example of wafer to wafer bonding is shown as a full package integration of a MEMS device with a CMOS wafer in [42]. In this work, the authors present a high volume, fully integrated multi-axis gyroscope that can be used in complex devices such as smartphones and smartwatches. In Figure 1.7, the process for this gyroscope fabrication is shown in detail. In the end, the two wafers are permanently bonded to each other by a layer of aluminium and germanium, sealing the main MEMS cavity and encapsulating the full device.

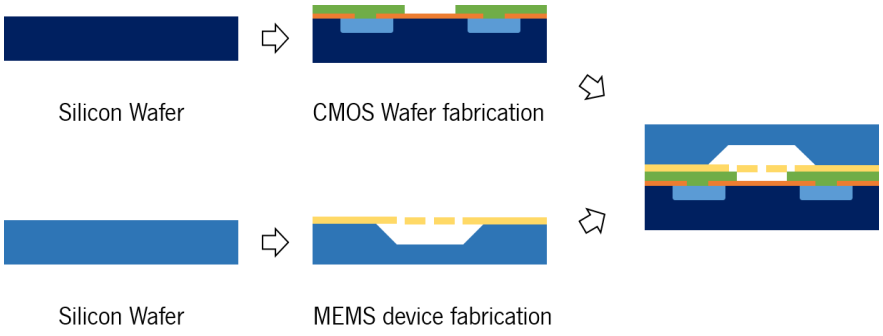


Figure 1.7. 3D Wafer Level Integration of a device and an IC as described in [42].

1.3.3. Multiple integration technologies

All the aforementioned complex integration processes are used in several research projects but, sometimes, more than one integration technique is used in the same device. STMicroelectronics [43] presents a fully integrated accelerometer that includes an ASIC device for control and a MEMS structure that measures acceleration. This integration is a perfect example of a 3D stacking between different processes. In this case, the 3D stack is obtained with the bonding of the MEMS device with an encapsulation, and then this encapsulation is bonded to the ASIC. In the end, the connections are made by wire bonding and the whole structure is prepared for flip-chip bonding with a ball grid array of solder balls (Figure 1.8).

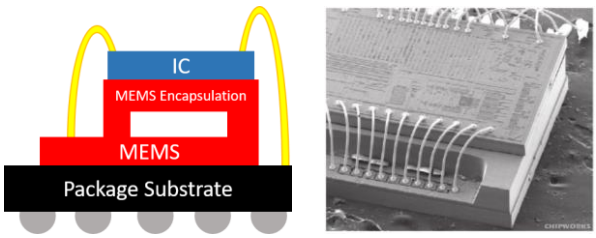


Figure 1.8. STMicroelectronics accelerometer package as described in [34].

Another good example comes from [44]. In this work, the author integrates a MEMS sensor, an ASIC, a wireless communication system, and a power management component, all in a 3D integrated package. This integration process uses 3D chip bonding to attach the MEMS device to the ASIC and both are bonded on a package substrate. This complex process provides an viable and complex solution to measure the pressure inside a tire. This research is extremely important since the focus is in the integration process, which provided a device ready for production (Figure 1.9).

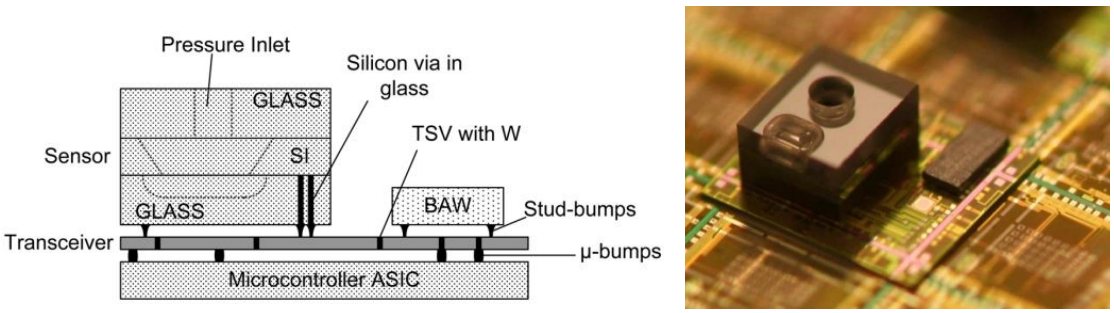


Figure 1.9. Complex autonomous pressure sensor as described in [44].

1.3.4. Non-conventional integration technologies

The usage of standard techniques is not always the way of creating new devices. Some complex integration processes are done in different ways, but not all of them have high reproducibility. In [45] the authors demonstrate a process flow to fabricate different MEMS integrated in the same board. In the end, the device is folded in a pyramid shape in order to obtain these devices integrated in several directions, including gyroscopes and accelerometers (Figure 1.10). For a device like this, the IC integration of the controlling circuitry was not considered but is absolutely necessary. Another big issue is the manual folding that is performed at the end. The mass production process that will produce millions of these devices will not be able to manually fold them, so an improvement for automatic folding is needed. Even so, the level of integration in a structure such as this one is a small approximation of what the future holds. With such devices, the development of micro bots and small autonomous robots becomes a reality.

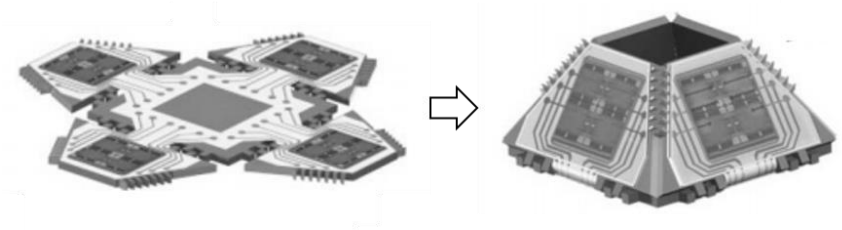


Figure 1.10. Complex integrated device with several MEMS described in [45].

These devices have extraordinary MEMS features, but they are not designed for integration. As a consequence, this integration is custom made, meaning that the encapsulation can be hard to translate to common factories that mass produce these devices [46].

1.4. Objectives and contributions

The creation of fully packaged autonomous devices is a reality, and their miniaturization brings major benefits for the technological advancements, such as lower costs, less power consumption, and high volume integration of different sensors and actuators. The usage of these systems in biomedical applications can enable a great improvement in patient treatment, providing implantable micro devices and self-diagnostic techniques. Systems-on-chip can bring a lot of new and desirable applications that, until now, had unreachable dimension requirements. These new

integrated devices can have sensors and actuators together with control systems, batteries or even energy harvesting circuitry for wireless devices [47].

This work is inserted in a project called "Wireless powered microsystem for thermal neurostimulation on medication-resistant neurological and psychiatric disorders". The objective of this project is the creation of an ultra-small packaged micro-cooler device to control medication-resistance disorders by thermal neuromodulation. The development of this micro-cooler is composed by four main tasks (4 different colours: light blue; Green; Yellow; Dark Blue), as seen in Figure 1.11. The cooling actuation will be performed by a Peltier device, which will lower the temperature of the local brain tissue. To control this Peltier and to handle power management, a small ASIC is required. Since it is this device's objective to be wireless and batteryless, the system requires a small antenna to communicate and receive power in the GHz band.

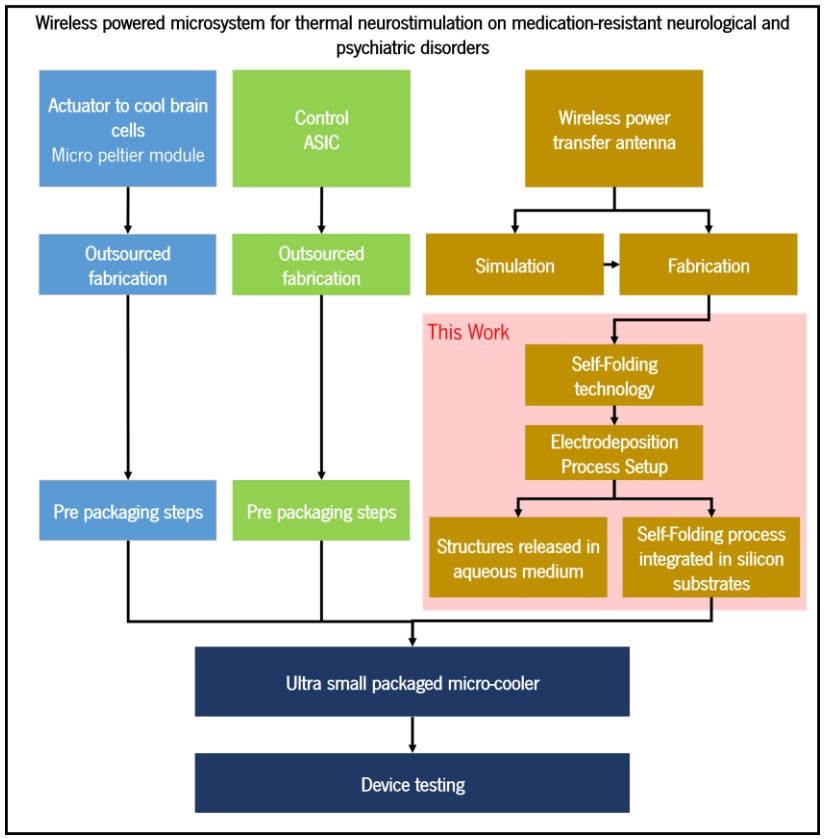


Figure 1.11. Project work flow for building a full integrated microdevice. Highlighted in red, the objectives of this work.

The work of this thesis consists in the development of the integration method of the wireless receiver antenna that is compatible with the remaining components of the micro-cooler device: the Peltier module and ASIC controller. This is achieved with the usage of 3D monolithic wafer level

packaging to integrate the 3D MEMS antenna on top of a silicon substrate. With such process, the fabrication is self-integrated and can provide a novel fabrication technique that will induce the usage of 3D structures on top of a CMOS wafer (Figure 1.12).

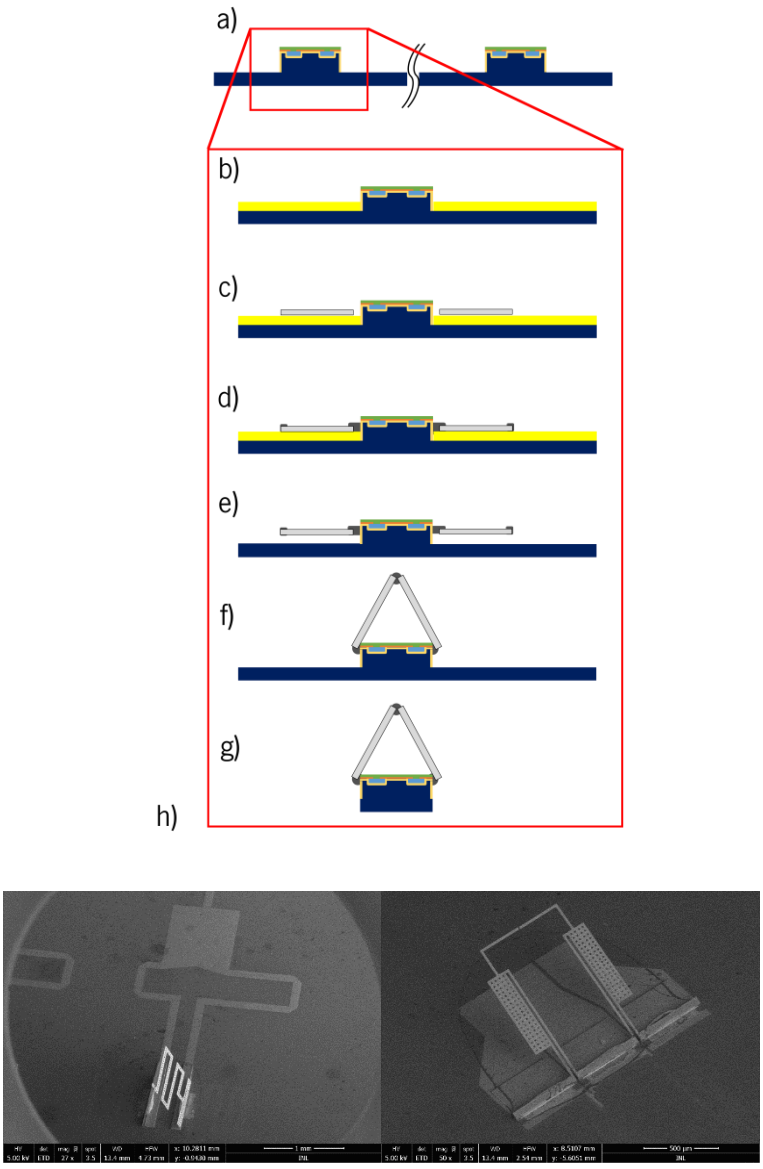


Figure 1.12. Wafer-level packaging: a) CMOS wafer processed in a foundry; b) Deposition of a sacrificial layer; c) Deposition of the main plates of the MEMS device; d) Deposition of the hinges of the MEMS device; e) Removal of the sacrificial layer by etching processes; f) Folded device integrated with the ASIC; g) Dicing of the full wafer, now integrated with the complex device; h) Final devices produced with the proposed wafer-level packaging process.

The wireless power transfer antenna is a 3D metallic structure fabricated with standard cleanroom MEMS technology. The planar antenna structure is patterned over a CMOS substrate, using sacrificial layers, and followed by a folding mechanism to produce the 3D assembly (Figure

1.12). The first developments of the self-folding technology are described in the work by Pedro Anacleto [48]. The work of this thesis within the overall project is highlighted in Figure 1.11. The work is intended to go beyond the state of art and create a process for integrable 3D structures with self-folding, as shown in Figure 1.12, which, besides being able to fabricate 3D microstructures, should also provide a solution to fully package a miniature thermal neuromodulator with control electronics and wireless energy receptors.

1.4.1. List of publications

- **J. Fernandes**; E. Vendramini; A.M. Miranda; C. Silva; H. Dinis; V. Coizet; O. David; P. M. Mendes. "Design and Performance Assessment of a Solid-State Microcooler for Thermal Neuromodulation". Micromachines 2018, 9, 47.
- H. Dinis, **J. Fernandes**, L. Gonçalves, P. M. Mendes, "Implantable thermal neuromodulator with wireless powering and wireless communications and fabrication method", University of Minho, European Patent, EP3263076A1 - 2018
- **J. Fernandes**, P. Anacleto, L. Rocha, J. Gaspar, P. Mendes, "Ultra-Small Packaged Micro-Cooler for Medical Applications" EPTC 2017, Singapore, December 2017.
- **J. Fernandes**; L. Rocha; P. Mendes; J. Gaspar, "Self-folding process for integrated 3D structures in complex microsystems", MNE 2017, Braga
- **J. Fernandes**, H. Dinis, V. Silva, I. Colmiais and P. M. Mendes, "Thermal modeling of an implantable brain focal cooling device," 2017 IEEE 5th Portuguese Meeting on Bioengineering (ENBENG), Coimbra, 2017, pp. 1-4. doi: 10.1109/ENBENG.2017.7889425
- H. Dinis, **J. Fernandes** and P. M. Mendes, "Slot antenna design for a wirelessly powered implantable microcooler for neuronal applications," 2017 11th European Conference on Antennas and Propagation (EUCAP), Paris, 2017, pp. 480-484. doi: 10.23919/EuCAP.2017.7928775
- **J. Fernandes**, H Dinis, LM Gonçalves, PM Mendes, "Microcooling solution development and performance assessment for thermal neuromodulation applications" IFESS 2016 – La Grande Motte, France, 2016

- **J. Fernandes**, H. Dinis, L. M. Gonçalves and P. M. Mendes, "Implantable microdevice with integrated wireless power transfer for thermal neuromodulation applications," 2016 IEEE 18th International Conference on e-Health Networking, Applications and Services (Healthcom), Munich, 2016, pp. 1-6. doi: 10.1109/HealthCom.2016.7749530
- F. Rodrigues, S. Gomes, P. Anacleto, **J. Fernandes** and P. M. Mendes, "RF CMOS wireless implantable microsystem for sacral roots stimulation with on-chip antenna and far-field wireless powering," 2015 European Microwave Conference (EuMC), Paris, 2015, pp. 76-79. doi: 10.1109/EuMC.2015.7345703
- H. Dinis, P. Anacleto, **J. Fernandes** and P. M. Mendes, "Characterization of chip-size electrically-small antennas for smart wireless biomedical devices," 2015 9th European Conference on Antennas and Propagation (EuCAP), Lisbon, 2015, pp. 1-5.
- H. Dinis, M. Zamith, **J. Fernandes**, J. Magalhaes and P. M. Mendes, "On-chip, efficient and small antenna array for millimeter-wave applications," 2015 International Workshop on Antenna Technology (iWAT), Seoul, 2015, pp. 227-228. doi: 10.1109/IWAT.2015.7365337
- **J. Fernandes**, P. M. Mendes and C. Abreu, "Towards long-term intracranial pressure monitoring based on implantable wireless microsystems and wireless sensor networks," 2015 2nd International Conference on Signal Processing and Integrated Networks (SPIN), Noida, 2015, pp. 1031-1034.doi:10.1109
- S. Gomes, **J. Fernandes**, P. Anacleto, P. M. Mendes, E. Gultepe and D. Gracias, "Ultra-small energy harvesting microsystem for biomedical applications," 2014 44th European Microwave Conference, Rome, 2014, pp. 660-663. doi: 10.1109/EuMC.2014.6986520

Chapter 2. Fabrication technologies and processes

2.1. Cleanroom and facilities

A cleanroom is a laboratory where particles in the air are controlled to certain sizes, as the purity of the air is extremely important when dealing with micro and nanodevices. Not only the air, but the pressure and temperature are maintained at the required values twenty-four hours a day. The INL cleanroom is class 1000, meaning that for each cubic meter there are less than 1000 particles in the air in the full cleanroom. Additionally, some rooms of this laboratory have even less than 100 particles per cubic meter of air. The cleanroom is divided in 7 main bays: 1. bio-bay, where biological samples can be used inside the cleanroom; 2. Metrology bay, where most of the metrology tools are located; 3. Etching bay, where the deep reactive ion etching (DRIE) machines are placed; 4. Deposition bay, where the sputtering systems are found; 5. Wet-bay, the room where most of the liquid chemicals are handled; 6. Lithography bay, where the lithography is done, from the coating to the development; 7. SEM and e-beam bay, where these two specific machines are placed. Using these facilities, microdevices can be produced with addiction and subtraction techniques on top of silicon wafers.

For this project, several fabrication techniques were used in the cleanroom. These techniques are described in detail in Appendix 1, and are listed below.

Deposition Techniques: Sputtering (Appendix 1.a); Chemical Vapour Deposition (Appendix 1.b); Electrodeposition (Appendix 1.g); Etching Techniques: Dry Etching (Appendix 1.d); Wet Chemical Etching (Appendix 1.d); Optical Lithography (Appendix 1.c); Metrology tools (Appendix 1.f): SEM; Optical Microscope; EDX; Sheet Resistance; Dicing (Appendix 1.e);

2.2. 3D Structuring technologies – Fabrication and integration

The main objective of this work is focused on the integration of 3D structures, developed with the self-folding technology, on substrates. Following the guidelines of a project where a sub-

millimetre small cubic 3D antenna, with 500 μm of height and width, should be fabricated and integrated to deliver a miniaturized neuromodulator. This device was developed in another work [12]. The main requirements for such a project are:

- High aspect ratio structure: Dimensions with a ratio of 50 between thickness and width/height;
- Wide range of materials: A process that can produce three dimensional samples with different materials, like polymers and metals;
- Resolution up to the sub-micron range: On the 3D structure, the smallest feature can have dimensions bellow 10 μm;
- Integrated process: A process that is done on top of other substrates and devices;
- Scalable process to industrial applications;
- Cleanroom friendly: A process that is compatible with other cleanroom processes.

There are numerous options that are used nowadays to microfabricate 3D objects. The MEMS market has been pursuing these fabrication processes for decades in order to achieve new devices and products that will revolutionize the future. Even so, there is no widely employed major process to fabricate these complex structures. New technologies and new trends are always appearing with different advantages and disadvantages. The industry constantly pushes for a cheap, fast and precise process, and the research field still hasn't found the solution. In this sub-chapter, some well-known techniques will be shown to understand why this project went for the self-folding technique to promote the self-integration of complex microdevices.

2.2.1. Sub-micron 3D printing

The fabrication of 3D objects exploded in the XX century. 3D printers took the research field by storm, and became a major investment for producing prototypes and experimenting new technologies. Fused deposition modelling (FDM) became the main 3D printing technology, and a lot of commercial options are available nowadays. The concept behind this technique is the deposition of a material that changes its phase in the deposition step. A nozzle receives the solid material (generally thermoplastics), melts it, and draws, the 3D object layer by layer. These prototypes could go from a few millimetres, to enormous parts with hundreds of centimetres.

Nevertheless, at the microscale this technology was not so reliable. In [48], the authors use an FDM machine to create 3D printed scaffolds for heart diseases. This technology is quite common to fabricate 3D microfluidic devices, as seen in [49], [50]. The main advantages of such technique rely on the cost and the fast prototyping, but have a lot of limitations regarding minimum feature size and the different materials that can be used.

FDM technology is not the only one resorting to a nozzle to dispense a material and draw a 3D sample. Inkjet printing is another good example of a process that fabricate 3D structures, in principle this structures are not as complex as the one that FDM can build, but they can be smaller and fabricated in different materials. In [51], the authors use inkjet printing (IP) to create a 3D antenna with silver ink (Figure 2.1). This technique is also used in microfluidic applications [52].

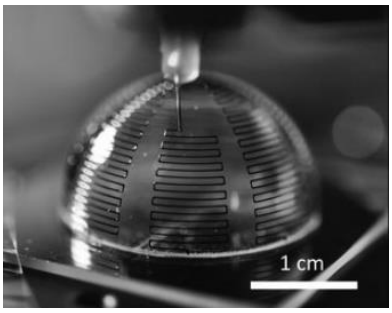


Figure 2.1. Inkjet printing of a 3D antenna (Adapted from [51]).

Stereolithography (SL) is one of the most well implemented technologies, and it is based on the polymerization of a photosensitive resin, layer by layer. A UV laser source is focused on the liquid resin, creating a reaction where the small focus point is solidified. With the changing of the physical properties of the resin, this process can draw in three dimensions, allowing the fabrication of complex 3D structures from the sub-micron scale to the millimetre scale. To draw in 3D, sets of reflective mirrors have the capability of focusing the UV laser beam on any point in 3 dimensions. In the end, the liquid resin is removed with solvents, revealing the polymerized structure.

For 3D structuring with hundreds of micrometres, SL machines are commercially available, with hundreds of companies producing them. The processes are fast, and can create complex 3D samples with polymeric resins. In [53], the authors fabricate small complex 3D samples using a commercial SL printer with PDMS polymer. With it, biocompatible devices can be created in situ with geometries that are not achievable with normal FDM 3D printing. In Figure 2.2, a small pyramid shape made in PDMS polymer is presented, and a blade measuring less than 1 mm is shown. At INL, a Formlabs Form 2 SL printer is available, but it can only print in specific polymeric resins, not

in metals. Additionally, the resolution is highly dependent on the laser beam diameter. In this case, the printer has a resolution of 140 μm in X and Y directions and a resolution of 20 μm in the Z direction.

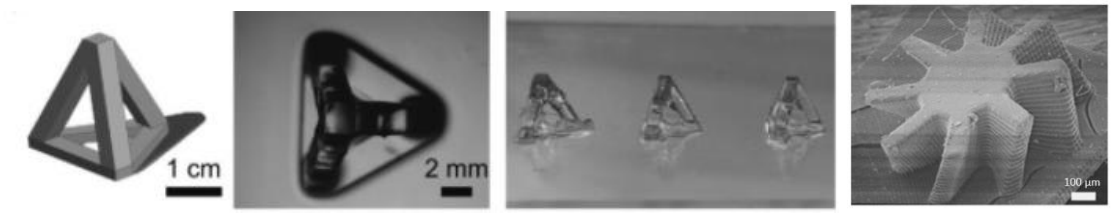


Figure 2.2. 3D structures fabricated with commercially available SL machines (Adapted from [53], [54]).

2.2.2. Micro direct writing laser technologies

Inside the SL field, a new technology called Two-Photon-Polymerization (2PP) emerged in the last decade, where sub-micron patterns can be microfabricated, creating the most complex 3D structures achievable to this day. This technology uses a femtosecond laser that pulses two photons to polymerize the resin, conducting to even higher resolutions on producing microstructures, yielding dots of approximately 100 nm. This other type of SL, on the other hand, cannot produce samples with hundreds of micrometres due to the time consuming and expensive nature of the process, and it is used for polymeric fabrication and not complex metallic structuring. Several works with this process are available, putting the great capability of the technique to use in innovative medical applications or complex MEMS for electronic devices [55]–[58].

Two examples are shown in Figure 2.3: one is a micro grid for bone tissue regeneration, and the other is the fabrication of a micro vase with high detail. In other examples, this technology is used to create polymer conductive microstructures to use in biomedicine, MEMS and microfluidics applications [56], and to create 3D nanoparticles in “gear” shape [57]. There are other SL technologies created by different authors, but the core principle is always the same, the point by point polymerization of resins. At the INL there is a workstation with a Femtosecond laser that works between 690 and 1040 nm that can polymerize different resins to obtain these complex 3D structures. In principle, SL technologies can be done on top of substrates aligned with them, creating an automatic integration between the structure and the substrate.

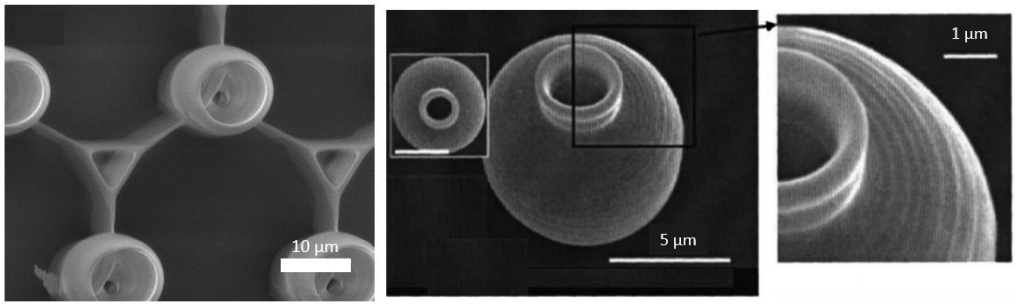


Figure 2.3. 2PP micro structures (Adapted from [55], [58]).

Lasers are not only used to polymerize resins. Another well-known technique, called selective laser sintering (SLS) or selective laser melting (SLM), is used for the creation of complex 3D samples. In this case, the raw material is powder and a high power laser is used to melt and solidify the powder in a focused point, meaning that with sets of mirrors to move the laser, 3D structures can be solidified point by point. In this case, the wavelength is not the important feature, but the power of the laser that heats up the material. The big advantage related with SLS comes with the usage of different materials, like polymers, ceramics, metals, and composites, creating a high range of different applications. The resolution is not as high as the 2PP technique, but it can fabricate small structures with a few micrometres. The process can also be performed on top of substrates, easily integrating these 3D objects with devices and other components [59], [60].

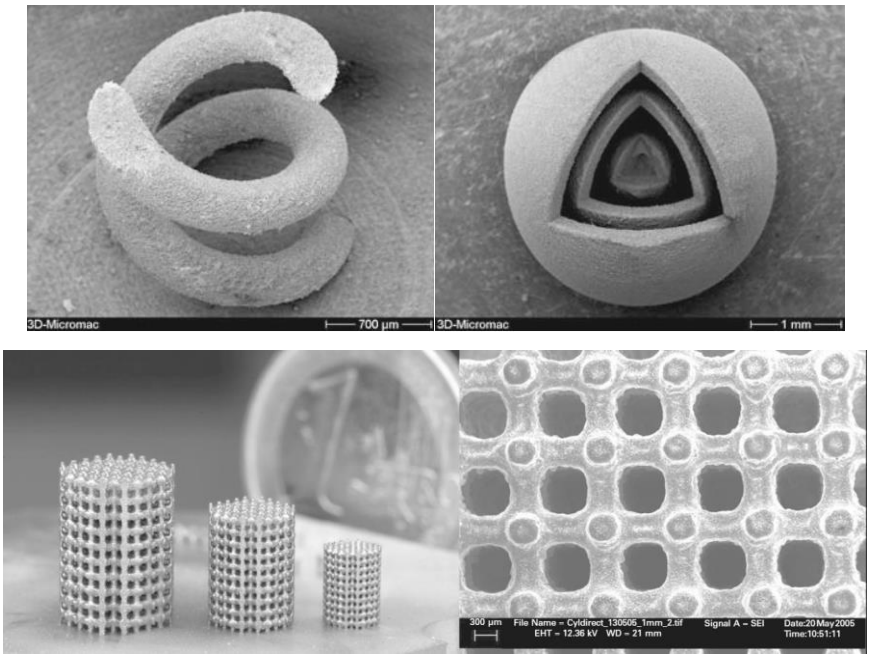


Figure 2.4. Metallic structures fabricated with selective laser sintering (Adapted from [59], [60]).

Laser chemical vapour deposition (LCVD) is a technique similar to the previously mentioned one. The difference comes again in the raw material. In this case, they are in the gas phase and, with a laser, these gases are dissociated on top of the substrate, the reactant gases are removed keeping only the desired material on top of the substrate. The technique can achieve spots of approximately 1 μm, creating interesting 3D structures on top of substrates. Since the laser is focused in one place, the dissociation of the gases only occurs there, promoting the localized deposition of the desired material [54]. Generally, this technique is used for the deposition of ceramics and passivation materials. In [61], the LCVD technique is used to create 3D microcoils to use in low frequency response accelerometers.

Focused ion beam (FIB) is a well know technique to fabricate 3D structures with deposition and etching techniques. Generally, inside a FIB chamber a similar process to the LCVD happens, but instead of a laser, an ion beam generated from a gallium liquid source is used to dissociate gases. Both ion beam and laser sources are controlled and can be focused in the three dimensional space allowing the fabrication 3D objects. With such equipment, the user is able to deposit Platinum alloys and etch different materials, allowing the creation of complex structuring. The resolution is extremely high, and the possibilities are endless, yet the major problem comes with the time that it takes and the power consumption to fabricate such structures. The authors in [62] used FIB to create a grid of complex 3D wiring between different structures (Figure 2.5) and, in [63], this technology was used to fabricate suspended nanowires in order to create novel transistors. The last three shown techniques, SL, FIB and LCVD, are considered direct writing techniques.

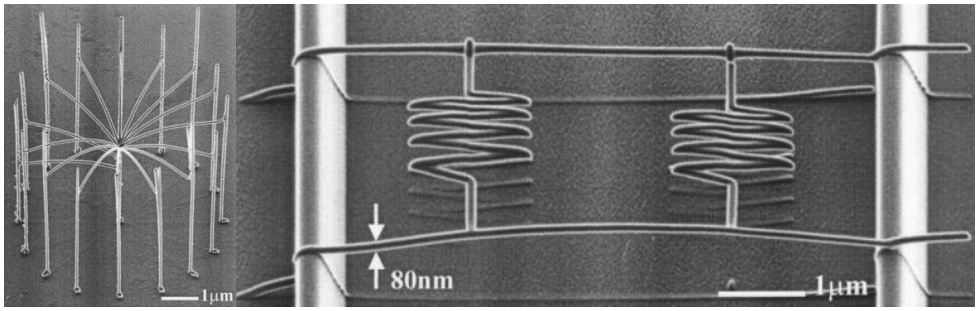


Figure 2.5. 3D FIB structuring of small wires (Adapted from [59], [60]).

2.2.3. Cleanroom technologies

The techniques described in this chapter are related to cleanroom fabrication processes. But inside the cleanroom, there are numerous addictive and subtractive techniques that, when put

together, can promote the creation of 3D objects. One of the most well-known technologies is the LIGA process (German for Lithography, electrodeposition/electroforming and chemical mechanical planarization), where the conjugation of three different processes creates a three dimensional structure on top of a substrate. In principle, the complexity of these structures is reduced because it can only transform a 2D pattern into a 2.5D object, since only one lithography is used. Even so, this is a way of creating 3D objects like the one presented in Figure 2.6, where the structure was used for nuclear power applications. In this case, the 3D structure is produced on top of a sacrificial layer, and in the end is separated from the substrate.

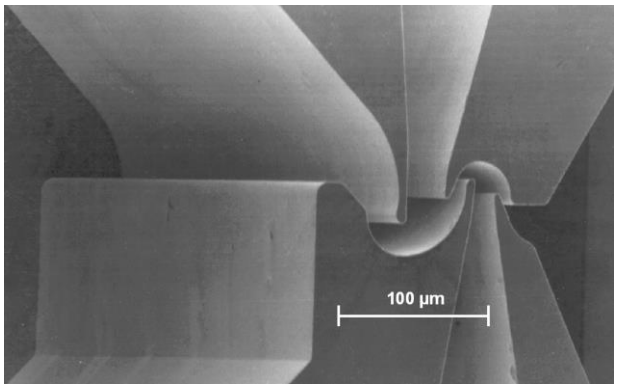


Figure 2.6. LIGA process for 3D fabrication (Adapted from [64]).

The LIGA process was one of the first cleanroom 3D structuring processes to appear in the market, but with the advances in multi-layer technologies, the EFAB process appeared. It uses a similar technology as the LIGA process, but with the use of several lithography and electrodeposition steps. With it, several patterns can be transferred, and since is a multi-layer process, the 3D is more complex. Since these processes are done in cleanroom steps, the integration is automatically achieved. In Figure 2.7, a microgyroscope is done with the help of 37 lithographies, using Ni plating and Cu as sacrificial layer. In the end, the copper is removed and all the Ni structures stay suspended [65]. As another example, this technique was used to fabricate an integrated coaxial cable for RF switches and couplers for millimetre-wave frequencies [66]. Other techniques such as deep reactive ion etching and ion milling steps are also quite common when 3D structuring is required, of which some examples are given in [67]–[71].

Embossing [72] and molding techniques are also quite common when 3D microfabrication is required. With such techniques, it becomes easy to replicate the same structure hundreds of times, giving more reliability and scalability to some devices. EBAF and LIGA processes are generally

good processes to fabricate molds for such devices. Using resins, these molds can be casted and used several times for mass production [73]–[75].

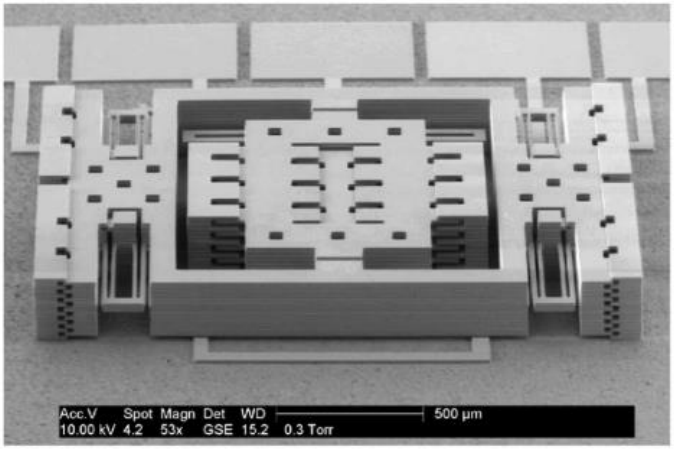


Figure 2.7. EFAB process of a microgyroscope (Adapted from [65]).

Self-assembly and self-folding techniques are emerging technologies that are similar to EFAB and LIGA processes. In these techniques, the usage of lithography and electrodeposition steps creates complex 2D patterns that can be automatically folded into 3D structures, transferring the 2D lithography patterns to other planes. The main advantages are focused in the usage of standard cleanroom techniques and without a big amount of lithography steps. High aspect/ratio semi-complex structures can be fabricated quickly and with a low cost. A disadvantage of such technique comes with the production of 3D structures that are not integrated in substrates. Some examples of such process can be found in [76]–[78], where complex 3D objects are released in an aqueous medium. In the other processes, like LIGA and EFAB, the structure can be released or not in the end, with the use of a sacrificial layer. It is believed that the self-folding technique can also be adapted to have an automatic integration with the substrate.

2.2.4. Fabrication processes overview

Looking at the requirements for the 3D structure presented at the beginning of this chapter, 2PP and IP are not good option because the final result does not have a good aspect ratio in the sub-millimetre scale, meaning that using such technologies would not be suitable to creating a small cubic antenna with 500 µm edges. The two direct writing techniques, LCVD and FIB are slow processes, not scalable and with reduced material application, one for ceramics and the other for platinum structures. FDM and SL standard techniques are not suitable because they cannot achieve

resolutions for features with less than 10 μm, and are limited to polymer composites. SLS would work to fabricate such structure, but would not be scalable in a cost-effective way. Cleanroom techniques are the processes that fulfil all the requirements, as both EFAB and self-folding work. Self-folding is in fact the technology with more advantages, because it becomes possible to pattern in all directions and use considerably less steps in the fabrication process. In the end, this process was chosen because it can create high aspect ratio structures with complex patterns in every direction, in a cost-effective way inside a cleanroom. The structures can be produced with metals and can have small features of a few micrometres, because it only depends on the lithography steps. Devices with 1 mm of height and width and with 10 μm of thickness are a reality with a self-folding technique. Transforming the self-folding process into a self-integration process of 3D microstructures with other components is, as explained before, one big objective of this work. The next section (2.3) will go through the self-folding technology, how it works and what kind of structures it can produce.

2.3. Self-Folding

The recent technique of self-folding, used to fabricate 3D micro structures from 2D planar structures, will be described in detail in this chapter. This already implemented microfabrication flow is the core of this project's final process. Based on it, and using cleanroom standard techniques, a new novel process flow will be developed to get a more reliable, and scalable, microfabricated device.

2.3.1. Surface tension driven folding

One of the main challenges to the microfabrication of 3D submillimetre structures is the 2D dimensionality of cleanroom fabrication technologies. With standard techniques and lithography patterns, it is easy to develop complex structures from the top and bottom faces of the substrate (z-axis), but it is almost impossible to pattern structures in the other axis (x and y). A few novel techniques like two-photon lithography, laser micromachining and ion beam milling can overcome this challenge, but they are complex, expensive and time-consuming. 3D self-assembly and self-folding is a prominent technology that promises to overcome some of the disadvantages from other novel techniques. Based on an ancient Japanese art, called origami, from a 2D pattern a 3D object

is created. Since manual folding is almost impossible in the submillimetre scale, the inclusion of surface tension-driven forces allows an automatic folding of the, so called, hinges [12], [79].

These surface tension forces will be used to lift the lithographed patterns using temperature control. For that, and since most of the usage of these systems will be related with electronic devices, there is a need for this devices to be conductive, therefore solder (Sn/Pb) metal layers are used as hinges. When these hinges are melted, the surface tension with other liquids or air promotes the movement of the suspended structures. In Figure 2.8, a simple cubic design is shown to exemplify the self-folding process. This 2D planification, represented in a), is constituted by two major layers: the square plates of the device in grey (generally the active area of the future 3D device), and the folding hinges in black. In b), the cross-section is showing that the hinges have to be significantly higher than the plates, so that when the melting occurs the surface tension can allow the formation of a big bubble of tin that will help lifting the plates. In c), the hinge is melted and acquires the shape of a bubble and, finally, in d), e) and f), considering that one of the plates is fixed, the other starts moving [12]. Other techniques like electroactive polymers, magnetic forces or stress induced forces were also published in recent works [80], [81]. With such techniques, the possibilities are almost infinite in terms of complex structuring and complex designs, allowing the development of high ratio, thickness vs width and length, out of plane devices, thus bringing a whole new range of opportunities and applications to MEMS and biomedical devices [12], [79].

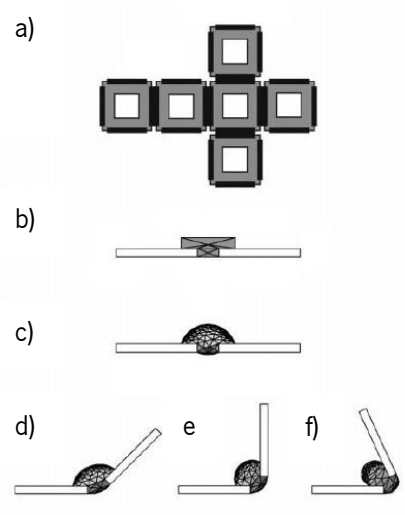


Figure 2.8. Self-Folding Process. a) 2D planification of the sample; b) Side view of the microfabricated structure with the panels and the hinge; c) Melted hinge after the temperature increase; d) e) and f) folding step where the hinge lifts the right panel [79].

2.3.2. Self-Folding in aqueous medium

Self-folding to create small 3D objects has already been published, with different purposes and applications. The process appeared in 2007 in the group of David Gracias from the University of Johns Hopkins after several years of development [79]. In this well elaborated paper, the authors created a process to obtain 3D objects with this technique, creating simple structures in an aqueous medium. The same authors published different folding mechanisms and more complex designs with a lot of different applications in the subsequent years. One good example is the creation of microgrippers [82] that can fold with a low temperature (Figure 2.9).

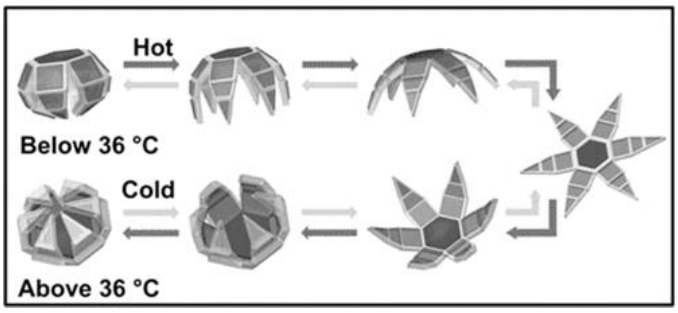


Figure 2.9. Microgrippers developed by David Gracias laboratory [82].

These authors published a work [83] that illustrates and shows how to make this process in detail, and where they reveal that the equilibrium folding angle is directly related with the volume of the hinge, therefore the thickness of this thin film will be critical for the folding step.

Anacleto [12] used this technique to develop sub-millimetre sized antennas. He made a complex simulation study on the antenna design, creating a 3D U-shaped structure with 500 μm of length. He achieved these 3D structures well patterned and well defined in an aqueous medium. This turned to be an issue in the characterization and functionalization of the 3D objects, because it was impossible to manipulate and attach these small structures to complex devices. This created the necessity for a new project, where these small structures should be developed on top of the final device. The author work flow is described in Figure 2.10. The process is simple and only uses cleanroom standard techniques. It is composed of a PMMA sacrificial layer that will be removed in the final steps of the process, an evaporated adhesion layer (Cr) and a seed layer (Cu) to perform the critical electrodepositions on the next steps.

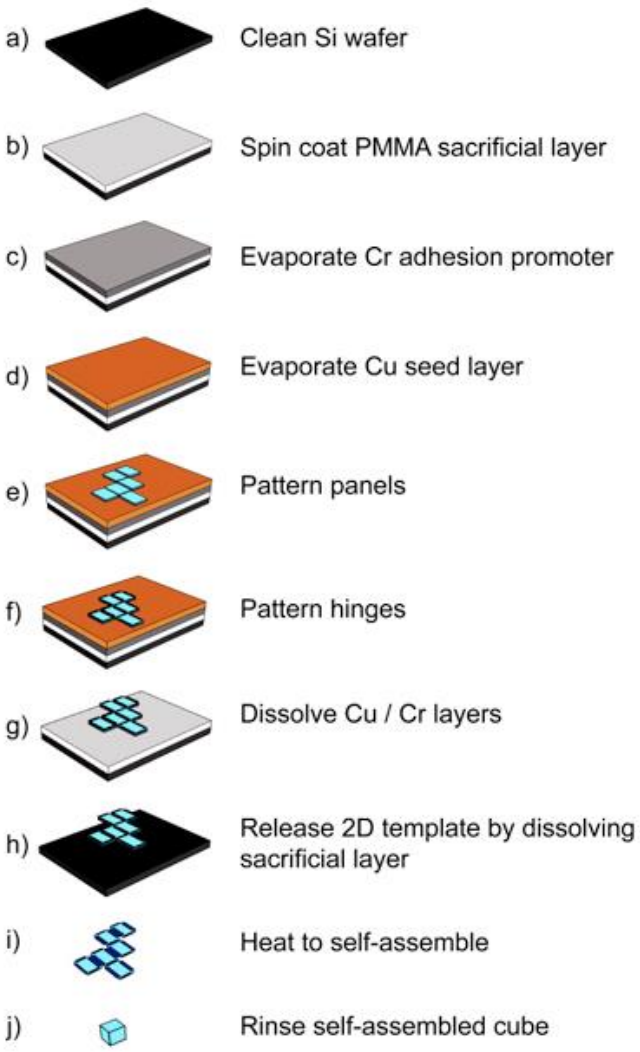


Figure 2.10. Process flow adapted from [83].

A lithography step and a subsequent electrodeposition are performed for patterning of the plates, and these steps are repeated with a different mask to pattern the hinges. Finally, the sacrificial layer is dissolved, releasing the 3D objects in an aqueous medium. The process of folding is also described by the authors of [83] in six steps:

1. Place the 3D objects in a petri dish and distribute them uniformly;
2. Add 3 to 5 ml of 1-Methyl-2-Pyrollidinone (NMP) and 5 to 7 mL of Liquid Solder Flux (this flux will help to destroy the natural oxidation layer that appears in the 3D structures)
3. Heat to 100°C for 5 min. In this step, the flux dissolves the oxide layers
4. Increase the hotplate temperature to 150°C for 5 min. Then, increase the temperature to 200°C until the folding occurs. After reaching 200°C the folding starts and the mixture can turn brownish and starts to burn.

5. When the 3D samples are folded, the hot plate is turned off and the solution is allowed to cool down.
6. Rinse the structures with acetone and then IPA, to clean them, and store them in ethanol.

Folded structures are shown in Figure 2.11

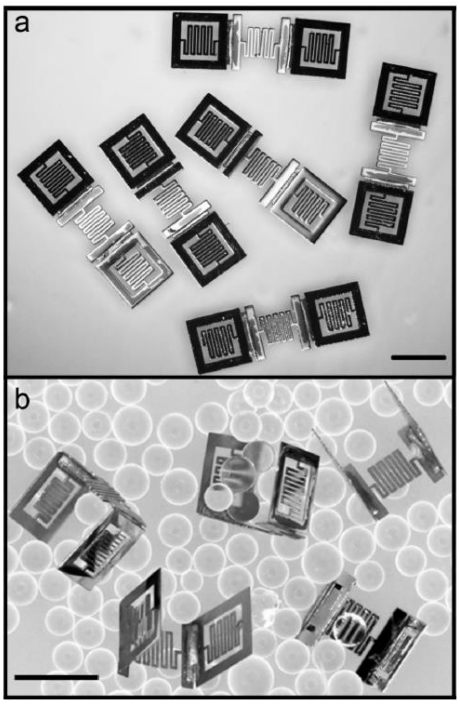


Figure 2.11. 3D antennas developed with a self-folding technique (Adapted from [12]).

This self-folding technique is a viable procedure to create semi complex 3D devices. However, the main challenge is the release of the samples in aqueous medium, which prevent their reliable packaging and integration with other system components. A new integrated self-folding process was developed in this work to fabricate 3D structures on a silicon substrate to be used as sensors or actuators.

Chapter 3. 3D Integration development

In this chapter, the development of the 3D integration methods required to fully package the system components for a micro-cooler device are explained. First, the ultra-small packaged micro-cooler, and its packaging requirements, are presented. To fully understand the fabrication methods for such a complex process, the self-folding technology in aqueous medium, previously described in the literature, was replicated. In order to implement these processes at INL, a Ni and Sn electrodeposition setup was developed and calibrated to produce the thick metal films for the planar antenna microstructures.

3.1. Ultra-Small packaged micro-cooler

Following the guidelines of the project, and respecting that integration of complex devices should be considered from the beginning of the development, the concept device for the creation of a complex highly integrated micro-cooling system is shown and explained in this section. This first test device is intended to work as a stand-alone wireless device that can cool down a small area of brain tissue, keeping the hot side temperature as low as possible. This will require the development of a packaging concept to obtain the required miniaturized device. It is imperative to know and understand how the different fabrication steps and components of the microsystem, highlighted in Figure 3.1, interfere with each other in order to develop the self-folding process and the integration of the different components.

The importance of the selected packaging technology is not only critical for the electrical connections, but also for structural definition, e.g., vacuum encapsulation, and thermal dissipation, e.g., heat sinks for certain devices [34]. In [84], the packaging is analysed to understand how high power LEDs can be packaged to provide a correct thermal management. The inclusion of dummy thermal conductive structures to dissipate the generated heat in the device can solve thermal issues. The inclusion of TSVs, or the bonding of the device to heat sinks, must be considered when such device is being made. Other devices, such as microdevices developed for biomedical applications, require biocompatibility of the packaging while being lightweight. The device reported in [46] is a

good example of a complex biomedical device that is composed by retractile needles that can be used as microelectrodes in brain tissue.

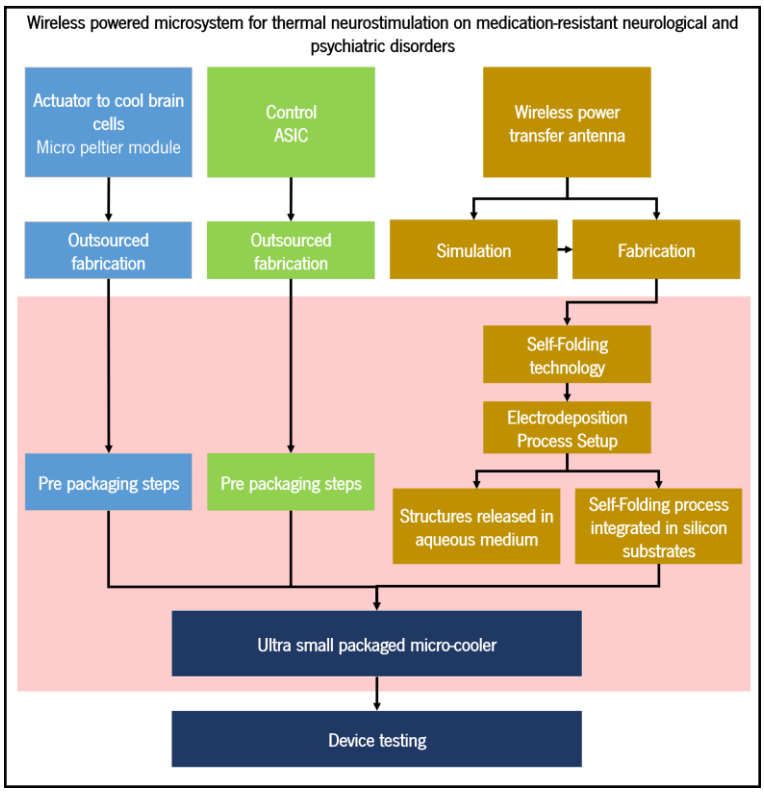


Figure 3.1 Project diagram. In red is highlighted the area of interest that is important to take into account before developing a new process.

For the proposed micro-cooler, the cooling actuation method relies on a micro Peltier module to lower the temperature of the local brain tissue, which must be packaged appropriately, assuring a good heat sink from the hot side of the device. In addition, this system is powered by an external device through a coupled wireless power transfer antenna that must be integrated into the small package. Nevertheless, since the integration of the antenna with the remaining system components is the goal of this work, it is also important to understand how the other two components, the ASIC and Peltier device, are interconnected between them inside the packaging.

3.1.1. Pre-packaging steps

It is expected that the ASIC and Peltier components are fabricated independently. The ASIC device will be produced in a CMOS foundry, and the full wafer will be individualized in small dies of 1.5 by 1.5 mm^2. The actuator, i.e., the Peltier module, will be produced with standard processes

and hundreds of small devices will be produced in each wafer. On the back side of such wafer, a thick layer of copper will be grown in order to create a heat sink. To grow such a copper layer, a thin seed layer of 100 nm of copper needs to be sputtered to allow for an electrodeposition step. This sputtered layer, in some cases, must be accompanied by a thin adhesion layer of another material, like chromium or tantalum. The electrodeposition will create a thick film of 500 µm to 1 mm, thus guaranteeing that the hot side has enough thermal connection to dissipate the heat that is generated in the thermoelectric chip. After deposition, the substrate will be diced to separate each Peltier chip with its own small heatsink. In this case, the electrical connection will require either wire bonding or flip chip in case the pads are placed on the front or the back side of the wafer, respectively. Considering that the antenna will be produced in this PhD thesis and that its integration will be considered from the beginning, the wafer will be diced to individualize each antenna. This small receptor is made of nickel and tin, and it will be fabricated on top of a silicon substrate. The device measures only 500 by 500 by 500 µm and it will be connected to the back side of the wafer, where a flip chip ball grid array will be placed to integrate it with the other devices.

Figure 3.2 a) ASIC designed in house to control the microsystem; b) Peltier device integrated with a heat sink layer of Cu; c) 3D antenna required for this device.

3.1.2. Packaging process flow

For the first test vehicle, the only required in-house fabrication process will be the antenna's, as the other components will be outsourced. Therefore, it will be impossible to do a complete wafer-level packaging of the three modules. The idea behind the research project of which this PhD's work is part of requires the use of 3D stacking integration methods like the ones presented in chapter 1.3.2. As explained, pre-processing steps are required before proceeding to the packaging process flow. The small ASIC microchip and the peltier device have to be integrated in laminate substrates that will be designed in a way that will make the two devices between them and

will also allow the connection of the 3D antenna. In the end, the electrical connections between the laminates and the devices will be achieved with wire bonding and flip chip ball grid arrays (Figure 3.3).

As seen in Figure 3.3, a grid array will be included on the back side of the laminate substrates in order to create the 3D stacking opportunity. To protect the wire-bonding connections, a polymer mold compound will be deposited on the two devices. In the peltier chip, the upper part will not be covered by this mold compound, since it will act as the micro-cooling plate and, therefore, it needs to be in direct contact with the brain tissue.

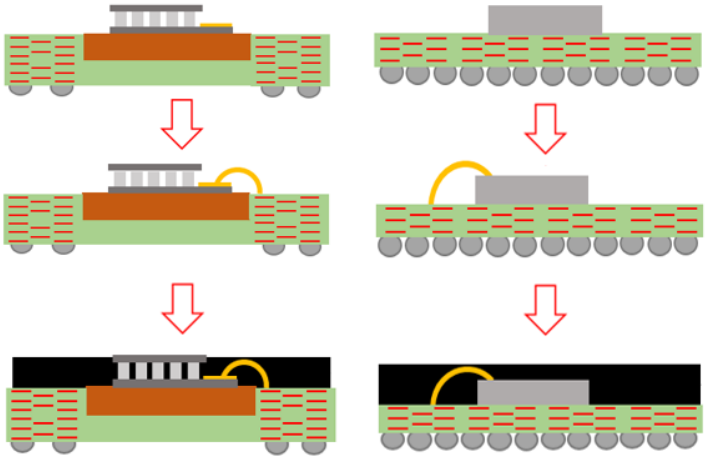


Figure 3.3 Integration of the chips (left: Peltier device; right: ASIC device chip) with laminate substrates and corresponding wire bonding, succeeded by injection of the mold compound.

For the interconnection between the ASIC and the thermoelectric device, through-package-vias (TPV), also called through-mold-vias (TMV) will be used (Figure 3.4). These vias interconnect the different systems, assuring the electrical and thermal connection between the devices inside the mold compound. It is a well implemented technology used by semiconductor companies like Samsung and Amkor [85]. Using a lithography and an electrodeposition of copper, it is possible to interconnect the two systems, as well as helping with dissipating the heat that the Peltier generates on the back side.

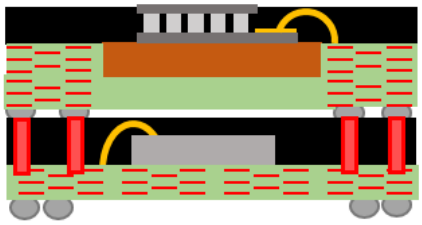


Figure 3.4 Fabrication of the through-mold vias.

The solder balls added in the chip containing the Peltier device create a direct connection between the two laminate substrates, ensuring all required interconnections between the ASIC chip, the antenna and the thermoelectric device. Like so, the system becomes highly integrated and it is expected to be smaller than 5 by 5 mm.

At this stage, it is hard to understand if the heat sink placed below the Peltier device and the complex thermal connection between all the different materials will be enough to dissipate the heat that is generated. In this scenario, a possible solution could be the implementation of thick copper bars in the system to conduct heat to other areas of the device for greater dissipation. In this way, several thermal vias would be implemented and distributed in a way that would not interfere with the electrical connections. These thermal vias would have a fundamental role in the 3D-stacked device, since they would drain the thermal energy from the thermoelectric device's hot side, keeping the overall temperature range inside the temperature limits. Thermal vias have already been reported in some small integrated systems [86]. To achieve this, the first proposal is to etch the whole system in specific places, followed by the sputtering of a conformal seed layer, and lastly an electrodeposition of the thermal vias (Figure 3.5). The main issue with this proposal can potentially be related to the etching step: since it will probably be done with DRIE, it can damage and destroy the whole system. A second way to tackle this specific problem is the etching of the small holes in each individual device and immediate electrodeposition of the thermal via. The major issue with this approach is its time-consuming nature, because instead of one lithography, three lithographies would have to be made, one for each chip. Regarding the remaining fabrication steps, they are all standard and common steps done in the INL cleanroom and will not represent any foreseeable problems in the future.

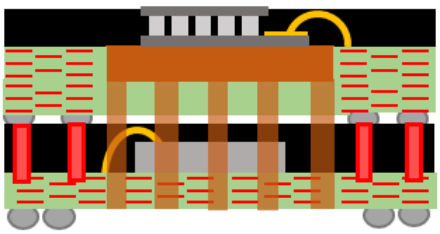


Figure 3.5 Fabrication of the thermal vias (represented in brown).

With the previous steps, the microdevice is ready to be integrated with the energy receptor. For that, and assuming that the complex self-folding process worked as in device presented in Figure 3.6, the antenna will be electrically connected to the back side of the wafer. After all the previous steps, the system is ready to be packaged. This antenna will be connected to the ASIC chip through direct ball array interconnection.

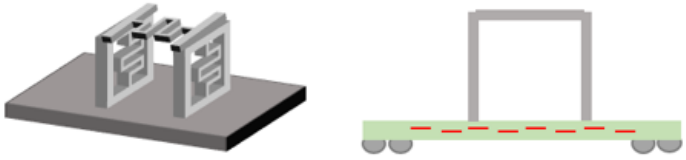


Figure 3.6 3D self-folding antenna fabricated on top of a silicon substrate.

In Figure 3.7 it is possible to observe the final integrated device's side and front views. The front view is intended to show that the thermal vias are placed away from the electrical connections, to not interfere with the electrical signals transmitted between the three modules. In the end, this device should be encapsulated with a biocompatible material, e.g., PDMS or parylene, to prevent rejection from the human body. Such encapsulation can be easily achieved with techniques like dip-coating or CVD processes. The final ultra-integrated microdevice, as previously explained, can be a solution for small implantable devices.

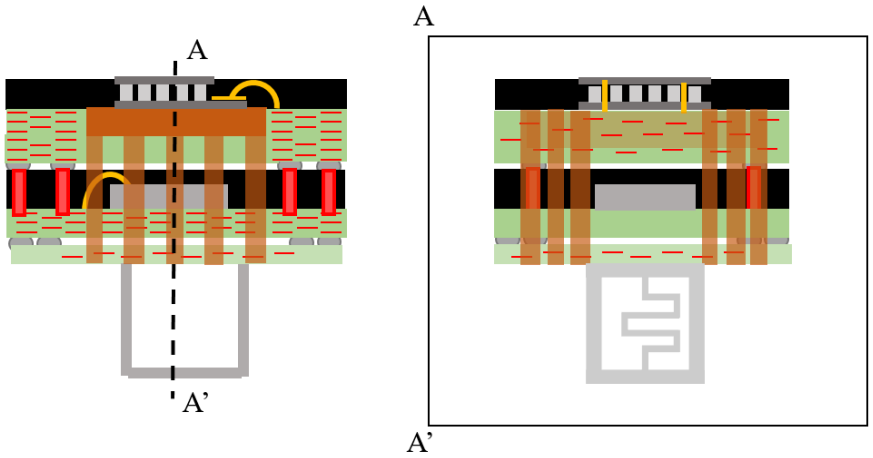


Figure 3.7 Proposed final integrated device.

3.2. Electrodeposition setup development

The electroplating of Ni and Sn is a crucial step in the implementation of the 3D self-folding technology. Unfortunately, such electroplating setup was not available at the INL facilities, as neither Ni nor Sn electrodeposition techniques are common in the MEMS industry. To fill this gap in the cleanroom, the electrodeposition setups required in this project were developed in-house. These systems were designed in such a way that at any time, they can be adapted for the deposition of metals other than Ni and Sn that might be required in the future, which means that the value of these systems is not limited to this PhD's work.

The process flow that will be used in the cleanroom was described in 2.3, where the small plates of the 3D structure will be composed of nickel to avoid incompatibilities with different wet etching steps in the full microfabrication process. These plates, designed to have 10 µm of thickness, will be electrodeposited and they will be coupled with 15 µm thick tin hinges.

The INL cleanroom is designed to work with 8-inch wafers (diameter: 203 mm), so every process should be adapted to this wafer size in order to guarantee the reliability and reproducibility of the process flow. The A.M.M.T. system is a complex electrodeposition machine present in the cleanroom that is capable of depositing thick films of copper. Since this system uses a specific wafer holder, the new setup should also be designed to use this holder (Figure 3.8). The holder electrically connects to the wafer on its edge and the current is transmitted by a screw on its back. The majority of the holder is made out of PEEK (a strong plastic with high chemical resistance),

sealed with four O-rings and closed with 8 screws made of the same material. This guarantees the protection of the metals (electrical connections) from the electrolytes used in the chemical bath. The exposed wafer diameter is 194 mm, so the borders for the electrical connection can measure up to 9 mm (4.5 mm in each side). This will influence the lithography processes, as the edge of the 8-inch wafer has to be open for a better electrical connection with the seed layer.

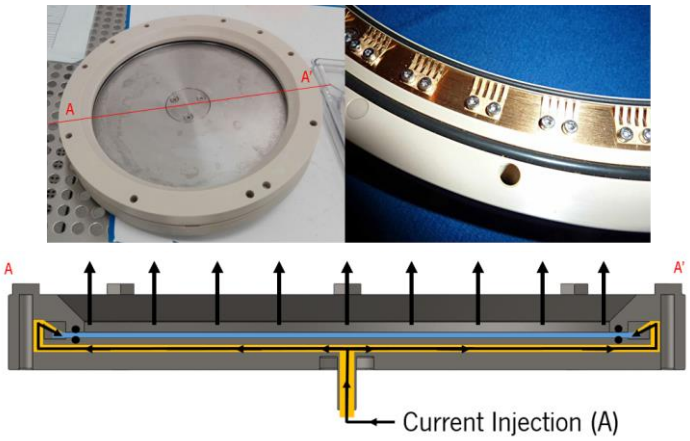


Figure 3.8. Wafer holder; spring loaded electrical connection; section view of the electrodeposition holder: silicon wafer (light blue); electrical path (black arrows);

The holder measures 250 mm, which dictates the smallest size of the electrodeposition setup's main chamber. It is connected with an M8 screw, so the cathode needs to be connected to the holder with a compatible conductive screw thread. For the anode, a similar holder is proposed for a 200 mm square of material using only a metal screw connection on the back and two O-rings to prevent the liquid from flowing to the bottom of the metal plate. This metal plate will have 2 mm of thickness, which will be useful for continuous deposition and allow for multiple electrodepositions before it needs to be replaced. This anode will be placed in the opposite side of the cathode, giving space for the electrolyte to flow in the middle. It is important to consider the distance between the cathode and the anode because it is one of the variables that has an impact on the uniformity and deposition rate. Inside the chamber, the liquid should be circulating at all times to prevent crystallization on the walls and tubing of the system. An in/out layout for a common chemical pump will be added to achieve this continuous flow and two chambers will be used in order to have an overflow for liquid circulation.

3.2.1. Nickel electrodeposition system

A first iteration of the electrodeposition system was developed and is described in Appendix 2.e. Everything seemed to be working fine except for the electrical conductivity of the liquid, so this should be the main concern for the design of the final version of the system. The placement of the anode and the cathode is crucial for the electrodeposition to work correctly. Looking at the schemes shown in Figure 3.9, the middle scheme (b)) was the one implemented in the first version of the in-house setup and, since it didn't perform as expected, it will not be considered for the final version of the system (Appendix 2.e).

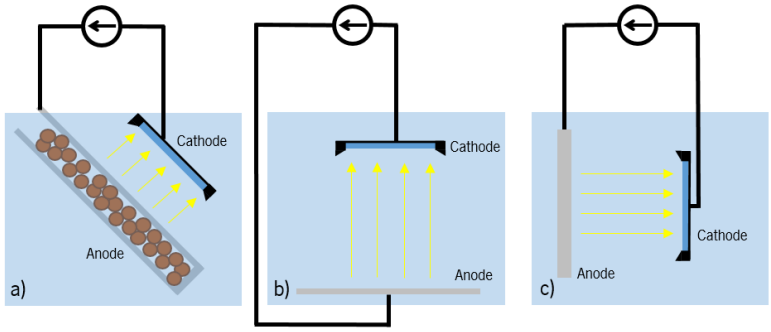


Figure 3.9. Cathode and anode position in different electrodeposition systems. a) A.M.M.T. system for copper plating; b) First version of the electrodeposition system design in this work; c) Classic electrodeposition setup.

The first scheme shown in Figure 3.9 is the A.M.M.T. system (Appendix 1.g). In this setup, the wafer holder and the anode are tilted 45°. To mill a system like this, special angled tools and a more powerful CNC with 3D machining would be required. So, the classic electrodeposition setup seems to be the most reliable system that can be machined on the available CNC. Just as it was required in the first system version, this final system should be cheap, compatible with the A.M.M.T. wafer holder, and include a pump to circulate the liquid. Additionally, it had to be designed to have the anode and cathode placed vertically. Before starting the design of this system, it is important to note that the biggest tool available had a size of 100 mm, limiting the depth of milling to this value. Since the wafer holder measures at least 250 mm, it is not possible to mill this setup in its final vertical position in this machine. Therefore, the system has to be machined in a horizontal plane and then placed vertically for the electrodeposition process.

Figure 3.10 presents a vertical chamber that is milled from the side. The system has a cover that is held vertically, like the chamber. A seal is needed to connect the chamber to the cover and to ensure that the system does not have any leaks. This seal will be made with a thick rubber that will be squeezed between the two parts. In the main tank there will also be two chambers: the inner chamber for the electrodeposition step and the outer chamber for the electrolyte flow (red arrows in Figure 3.11). The cathode and anode will be held vertically in front of each other, thus avoiding the air gap problem that appeared in the first iteration described in Appendix 2.e. The metal plate will be connected with a screw thread on the back side of the inner chamber. This metal plate will be tightened in between the inner chamber and a fixing ring. Two O-rings will also be used to prevent any leakage on the anode. The flow of the electrolyte will occur in the direction of the red arrows in Figure 3.11: the liquid is injected at the bottom of the inner chamber and it overflows to the outer chamber, being then pumped back to the inner chamber, creating a constant electrolyte flow.

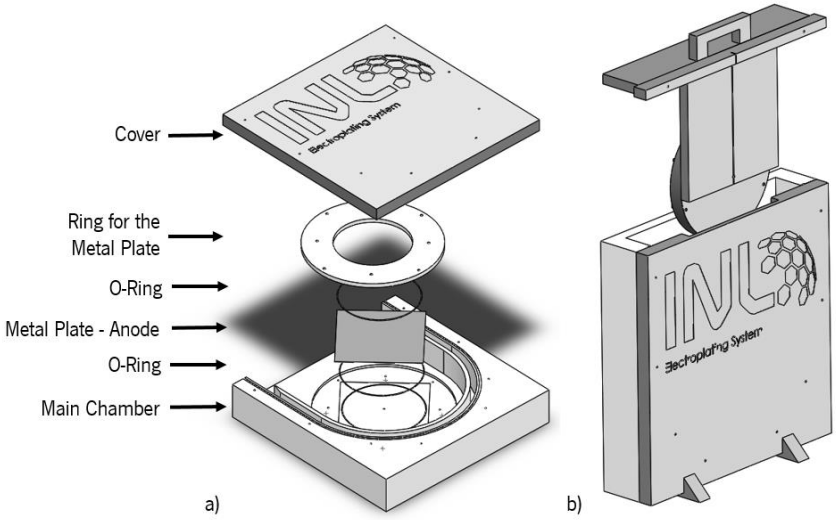


Figure 3.10. Electrodeposition setup – second version. a) Deconstructed main chamber; b) Main chamber with feet in final position and wafer holder attached to the wafer handler.

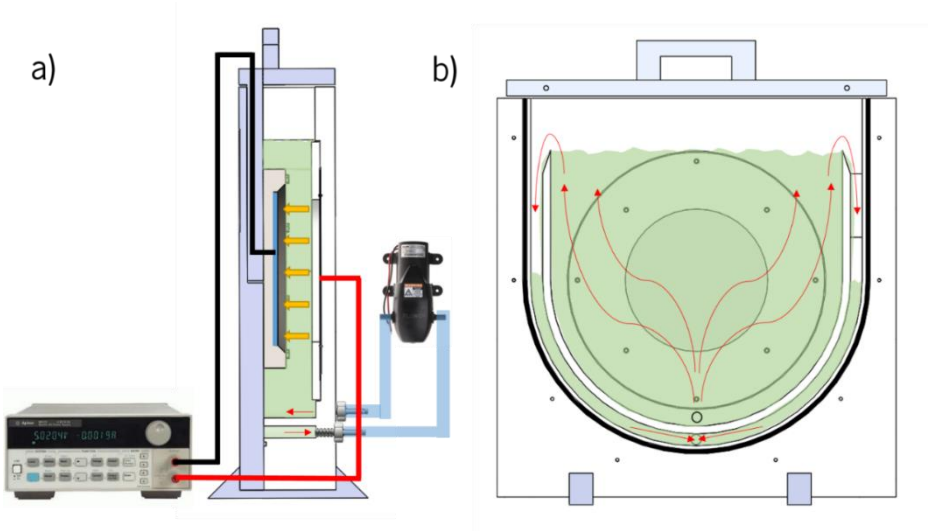


Figure 3.11. Electrodeposition setup – second version. a) Side view with the details of the electric circuit and the pump system; b) Front view giving the perspective of the interior of the chamber (the seal rubber is represented in black), the liquid flow is presented with the red arrows.

It is imperative to know the correct volume of liquid that the system can handle at a certain time. The inner chamber can hold 6.4 L of electrolyte, the outer chamber, in turn, can hold 0.88 L. The volume of the wafer holder (1.36 L) needs to be considered. The full system can be filled with around 6 L of electrolyte, of which 5.4 L will stay on the inner chamber, and the other 0.6 L will overflow to the outer chamber. A pump from Xylem will be used at a flow rate of 2.8 L/min. With this capacity, the pump will recirculate the full volume of liquid in approximately 2 min. A 1 cm diameter O-ring is needed as the main seal of the chamber. The distance between the cathode and the anode was fixed at 6 cm, like in the previous system. As shown in Figure 3.11 a power source from Keysight will be used to connect the anode and the cathode of the system, creating a current flow through the electrolyte. No temperature control was implemented at this stage, since most of these electrolytes can deposit at 21°C (room temperature in the cleanroom), which will be the predefined temperature for every process. To mill this system, four plates of polyethylene (PE) were bought from Polylanema®: one with 500 by 500 by 100 mm to machine the main chamber, two plates of 500 by 500 by 30 mm to make the cover and the ring for the cathode, and another one with 700 by 400 by 25 mm to produce other necessary components, such as the feet of the system and the handler for the wafer holder. The design was transferred to a CAD software named ArtCAM that generates the gcode files, for CNC machine (in this case, a Flexicam Viper CNC machine that is available at INL).

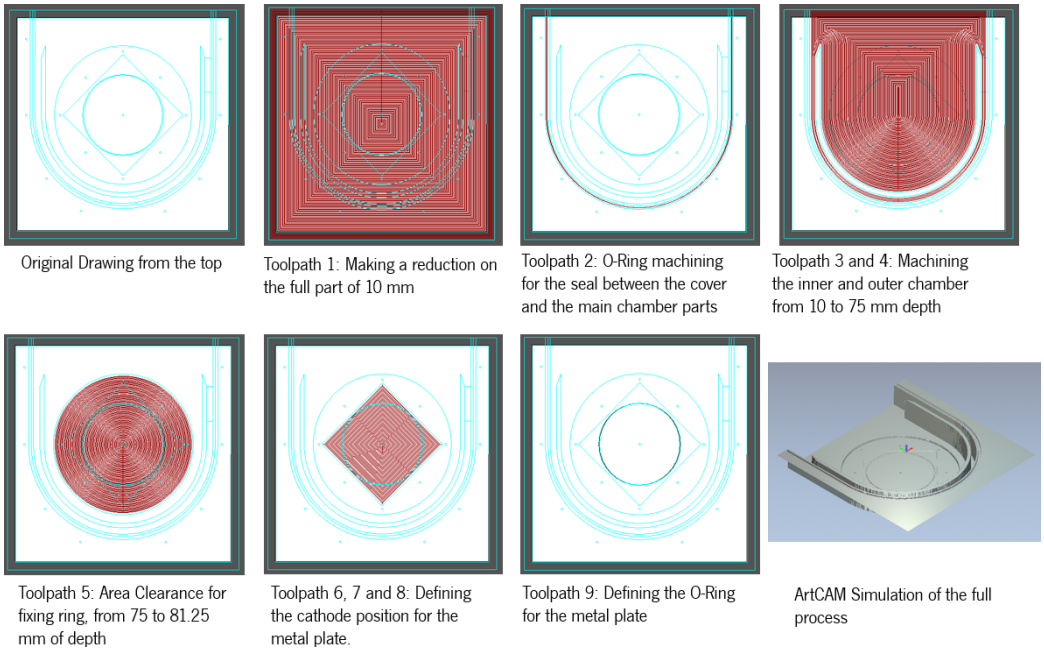


Figure 3.12. Detailed ArtCAM process.

The machining process for the main chamber took more than 30 hours. Drilling and milling tools are used to clear and drill the different areas of the chamber. The machine allows the usage of 5 tools at a time. The process resorted to an 8 mm tool for big area clearances such as the inner chamber and the fixing ring, the 6 mm tool for the big O-ring that will seal the chambers with the cover, and the 4 mm tool for drilling the screws that will fix the ring and the electrical connection of the metal plate. A final 1 mm tool was used to define the O-ring that will avoid any leaks from the chamber through the electrical connection screw. The final product of the milling process is shown in Figure 3.13. The left image is the result of the milling process on the CNC where it is possible to see the main chamber with all toolpaths milled correctly. On right side of the same figure, the full system is presented. There are two power sources, one for the pump and another one for the electrical connection between anode and cathode.

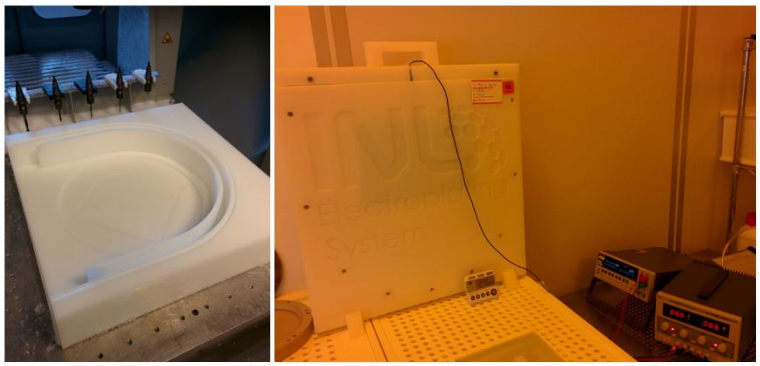
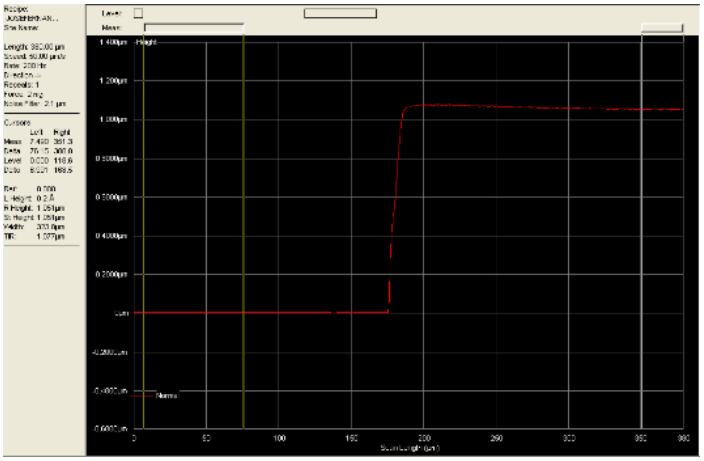


Figure 3.13. Main chamber after milling and full system inside the cleanroom.

3.2.2. Electroplating setup calibration

After developing the electroplating system and checking that every parameter is correct, i.e., that the pump is circulating the fluid with a constant flow and an accurate electric current is passing through the nickel electrolyte, it was time to undertake the first tests of nickel plating. The electrolyte used in this system is a Watts nickel plating solution commercially available from Alfa Aesar®. This electrolyte's chemical composition and chemical compatibility is analysed in Appendix 2.

To start using the system, it was necessary to eliminate any oxide layers in the anode. To do so, a 1 A current was injected in a dummy wafer during 30 min. Knowing that its area was approximately 300 cm^2, it originated a current density of 3.27 $\mathrm{mA/cm}^2$. After this step, the electrodeposition process was ready to start. In this case, with the same current density, the process lasted for two hours and no problems occurred, meaning that an air layer did not interrupt the system's electrical connection. The final result was a very reflective wafer covered with a grey layer of a conductive metal, indicating that the uniformity and grain of the electrodeposited layer were adequate (Figure 3.14).



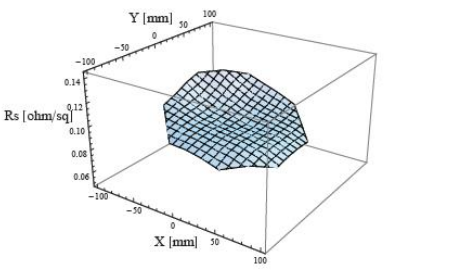


Figure 3.14. Wafer with plated layer, sheet resistance and profilometer measurement of the thin film of Ni.

Analysing the sheet resistance of the metal, the results were quite satisfactory (Figure 3.14). The uniformity was standing in approximately 20%, meaning that if the goal was a 10 μm thick metal layer, this deposited metal layer thickness could vary from 9 to 11 μm. It was also noticed that the thin film was thicker on one side of the wafer than the other. This error could be related with a non-uniform current distribution or a bad positioning of the wafer in the chamber. A rotation of the wafer could solve this non-uniformity problem, therefore this will be considered in the next iteration of the system.

To understand how the electrodeposition system was working, a resistivity mapper was used. This four point probe equipment calculates the resistivity of a metal thin film in a certain volume. This setup is normally used to obtain deposition rates and uniformities of sputtered or electrodeposited layers. This automatic machine is composed of 4 spring gold plated tips that measure a potential difference between the needles that are side by side in the probe. The sheet resistance is a measurement that respects equation 3.1.

$$R_s = \rho \times \frac{L}{W \cdot t} \tag{3.1}$$

$$R_s = \frac{\rho}{t} \tag{3.2}$$

The sheet resistance (R_s) is related with the value of resistivity, ρ, in a determined volume that is given in Ω.m. The volume of the measurement is given by a block of W x L x t, that represent the width, length and thickness of this block, as shown in Figure 3.15. To simplify the calculation, the machine considers that W and L form a square. Since the area is given by a square, L=W, equation 3.1 instantly becomes equation 3.2.

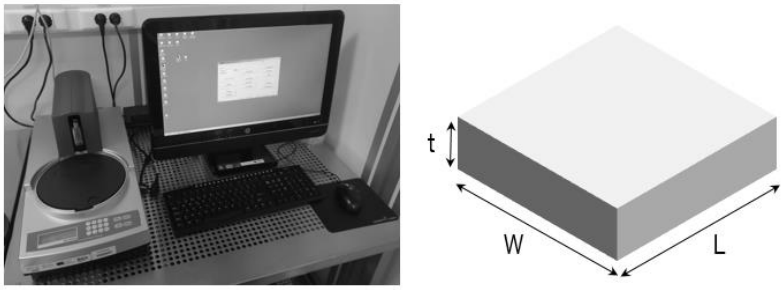


Figure 3.15. Four point probe setup.

Nickel has a bulk resistivity of $7x10^{-8}$ Ω.m, a value higher than copper ($1.206x10^{-7}$Ω.m), meaning that nickel is less conductive than copper. The nickel layer was measured in the mechanical profilometer: 1.05 μm. Using equation 3.2, and considering the value of thickness

measured on the profilometer and the average value of R_s presented in Figure 3.14, the resistivity of the stack with electrodeposited nickel and a copper seed layer was calculated, and the result was $1.014x10^{-7}\Omega.m$. Comparing the bulk resistivity with the measured value, there is a significant difference that comes from the fact that the nickel layer is on top of a copper/tantalum seed layer, and the electrodeposited nickel is porous, unlike the bulk state of the metal. The conductivity (σ) of the material is given by equation 3.3, and the value is $9.86x10^{6}$ S/m.

$$\sigma = \frac{1}{\rho} \tag{3.3}$$

The electrodeposition process was calibrated with dummy wafers to understand how the exposed area, injected current, time of deposition and layer thickness are related. The used mask consisted of an exposed area of $9.54\ cm^2$. For the first test, a dummy wafer with a patterned photoresist was placed in the electrodeposition setup for 30 min with 500 mA of current being injected. In the end, the photoresist was removed and the structures were measured with the mechanical profilometer. The average thickness obtained on the full wafer was 28.3 μm.

$$P_{rate} = \frac{Thickness(\mu m)}{Time(h)} \tag{3.4}$$

$$C_{density} = \frac{InjectedCurrent(A)}{Area(cm^2)} \tag{3.5}$$

Using equations 3.4 and 3.5, it is easy to obtain the plating rate (P_{rate}) of the system and the applied current density ($C_{density}$). It is also undeniable that both of them are related, and the plating rate will depend on the current density. With that said, a new value was created to relate all these components, the Plating ratio (P_{ratio}), and this value is obtained through equation 3.6.

$$P_{ratio} = \frac{P_{rate}}{C_{density}} = \frac{\mu m.cm^2}{A.h} \tag{3.6}$$

This plating rate becomes essential to understand how the system works. The obtained value is then used to determine the estimated plating rate (EP_{rate}). When performing another electrodeposition, we now know that the plating rate can be calculated for a new current density through equation 3.7.

$$EP_{rate} = C_{density} \times P_{ratio} \tag{3.7}$$

The equation formulated above allows the current density to be changed at any time to obtain different deposition rates. With the new estimated plating rate, it becomes easy to estimate the necessary current and time to obtain desired values of thickness. So, changing the value of

current density will automatically give precise values of time and injected current. It is important to be able to change this value because, sometimes, if the exposed area is small, achieving a small thickness can be impossible with high current densities. Lowering the value of $C_{density}$ will promote a lower plating rate, allowing the deposition of small structures over a long time period. A spreadsheet was created with these formulas, and whenever someone wants to electrodeposit nickel, the spreadsheet makes all the calculations for the system with the dummy wafer as a model.

Looking at Figure 3.16, the influence of the different parameters can be observed. If the current density is reduced to half (b)), the time of the deposition will double and the current injected will be corrected to fulfil the 500 nm. If the exposed area is increased (c)), the injected current has to be higher to yield the same thickness. If the desired thickness is bigger (d)), time will be the parameter that will change. With such system, the deposition of nickel layers on 8-inch wafers is made possible.

a)

Plating step details:

Exposed seed layer area, cm^2	9.54
Current density, A/cm^2 (2)	0.002
Estimated plating rate, um/h (3)	2.160305344
Target thickness, um (4)	0.5
Current, A	0.0190752
Plating time	833 sec (14 min)
Corrective plating time, sec	0

b)

Plating step details:

Exposed seed layer area, cm^2	9.54
Current density, A/cm^2 (2)	0.001
Estimated plating rate, um/h (3)	1.080152672
Target thickness, um (4)	0.5
Current, A	0.0095376
Plating time	1666 sec (28 min)
Corrective plating time, sec	0

c)

Plating step details:

[redacted]

d)

Plating step details:

Exposed seed layer area, cm^2	9.54
Current density, A/cm^2 (2)	0.002
Estimated plating rate, um/h (3)	2.160305344
Target thickness, um (4)	5
Current, A	0.0190752
Plating time	8332 sec (139 min)
Corrective plating time, sec	0

Figure 3.16. Developed calculation sheet for the electrodeposition setup.

3.2.3. Tin electrodeposition system

Following the success of the Ni plating system, the same design was done for the Sn deposition. Unfortunately a big system to electrodeposit Sn in full 8-inch wafers was not possible to achieve. The deposition rates and the reliability of the system did not allow a good Sn deposition of thick films. In Appendix 2.f the calibration tests and the full system are presented.

To overcome this problem, a small beaker with a custom made 3D-printed cover was developed to electrodeposit thin films of Sn. This cover was designed to hold two alligator clips in order to electrically connect the small samples and the anode material with the power source. In this setup, no agitation or temperature control was provided (Figure 3.17). These parameters could

be useful for a professional system, but when a beaker is used, stirring the fluid and precisely controlling its temperature becomes a difficult process. The temperature stayed at 21°C (cleanroom temperature) and the liquid rested without stirring or agitation during the whole process. The solution used in this system is from Caswell® plating, called tin concentrate solution, and its chemical composition and chemical compatibility are described in Appendix 2.

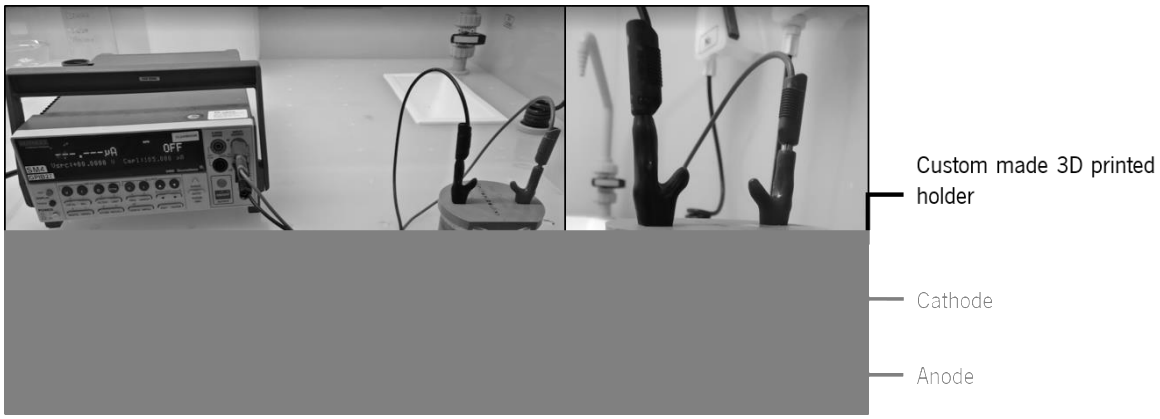


Figure 3.17. Tin plating setup for small samples.

The parameters to electrodeposit tin were calculated considering the current densities recommended by the liquid electrolyte's datasheet. The exposed area on each sample is 0.092 cm^2, meaning that 1.4 mA would be the required current for this area according to the datasheet. This current was injected during 20 min. and the expected deposition should create a thin film of 15 µm. The obtained result is shown in Figure 3.18.

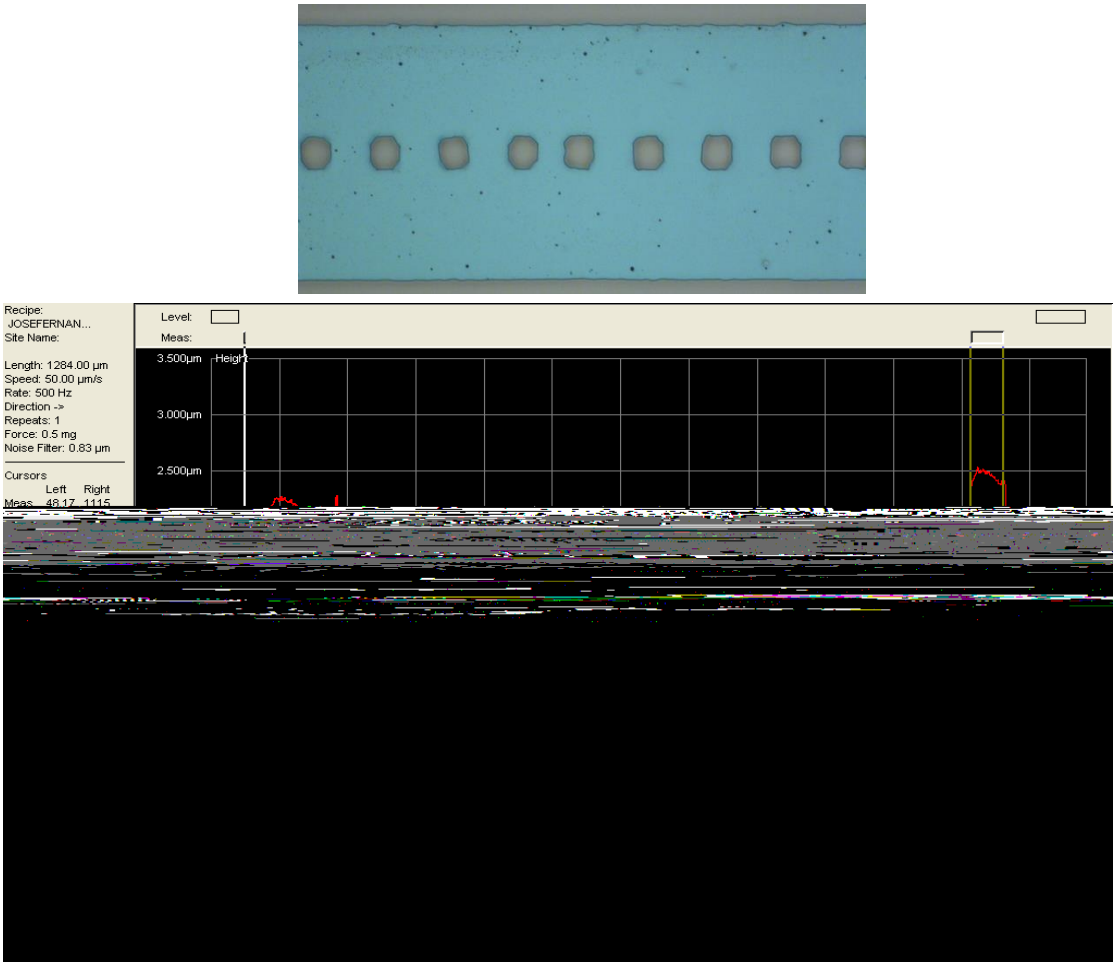


Figure 3.18. Tin sample in a small sample setup with 1.4 mA injected between the anode and cathode.

Looking at the measured thickness in the mechanical profilometer, the obtained value was between 2 and 2.5 µm, which is six times lower than the expected result from the datasheet. This can probably be due to current losses in the system, since the electrodeposition process generates foam on top of the liquid and this foam can come in contact with the alligator connector; the silicon substrate can also conduct current since the material is a semi-conductor, leading to losses on the backside of the sample (Figure 3.19). The following scheme shows where the losses probably come from in this small system. Even so, these results can be used, because the uniformity of the deposits was acceptable, meaning that growing a Sn film with a large thickness is achievable in this setup.

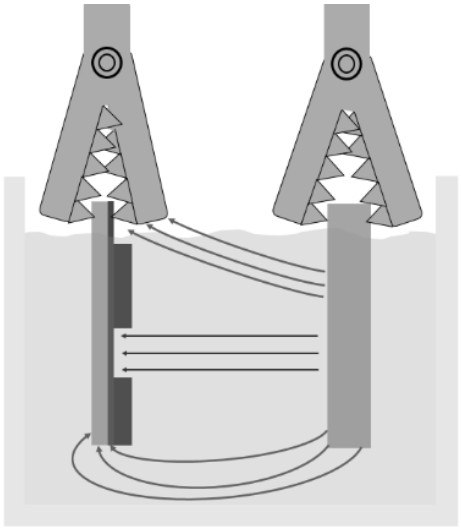


Figure 3.19. Losses in current represented by arrows in brown, in red the electrodeposition current wanted for this setup.

This small setup will be used in the final process, meaning that a dicing step will occur before electrodepositing Sn. With both nickel and tin electrodeposition setups ready, the plating steps are calibrated and ready to be used in the final process. The major change in the process consists on performing the dicing step just before the tin plating, rather than at the end of the whole process.

3.3. Self-Folding process development at INL

The main objective of this work, as previously mentioned, was focused on the integration of the 3D device on top of silicon substrates. For that, the self-folding technique was brought and adapted to INL cleanroom. At a first glance, this process should work as it is reported in [83], but the John Hopkins cleanroom and INL cleanroom are quite different, and some of the techniques are not shared between them. Consequently, there is a necessity to replicate the full process to get exactly the same structures that the previous author produced.

3.3.1. Mask preparation

Self-folding design rules are strict and should be respected at all steps of the process to ensure good results. Several experimental results were produced by the authors of [83] in order to relate the dimensions of the hinges with the dimensions of the plates. Computer simulations of

phase transition, in this case from solid to liquid solder, are a very complicated process and not fully implemented nowadays, so the authors were never able to simulate this process with finite elements software (FEM). In order to achieve satisfactory results without having to perform time-consuming experiments, the design rules reported by the authors are respected in this project.

As is shown in Figure 3.20, the authors of [83] show that the hinge's size should be directly related with the size of the plate that will be lifted up. So, in this case, if the plate measures L, the hinge should measure 0.2 x L of width and 0.8 x L of length. Considering the dimensions given in [12], the nickel plate should measure 500 µm, and the hinge should measure 400 x 100 µm.

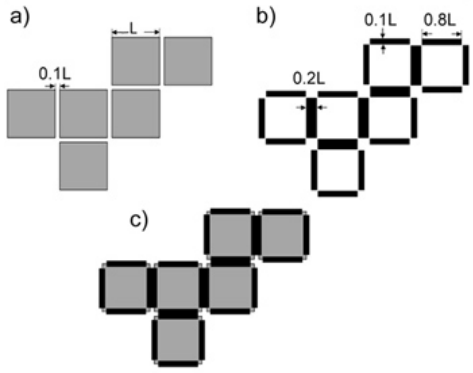


Figure 3.20. Recommendation dimensions for a 90° folding [83].

To improve the removal of the sacrificial layers, holes are designed in the samples, generally in the mask, to create access points for the chemicals to reach the whole sacrificial layer underneath the metal plates. Generally, these holes will not allow more than 15 µm of undercut. With this, chemical waste is reduced in the process, and it takes considerably less time to process each sample. These holes can later be removed to achieve better antenna performance.

The process will require two masks: one with the structural plates of the device and another one containing the hinges. The first one is shown in Figure 3.21 in red. There are two types of antennas that were designed by Anacleto, and these two antennas are replicated hundreds of times throughout the wafer. It is possible to clearly see the holes that were made in the plates to facilitate sacrificial layer dissolution. Both types of antennas have side plates that measure 500 by 500 µm; the main difference is the middle plate that in type a) measures 500 by 500 µm and in type b) measures 500 by 980 µm. This mask also contains alignment marks for the alignment between lithographies and alignment marks for dicing of the wafer in small dies. For the hinge mask, the design rules were respected and the hinges (green in Figure 3.21) measure 400 by 100 µm. The

small holes of 15 by 15 µm were also implemented in both masks for the previously mentioned reason. After having the design ready, the mask has to be written and prepared to be used in the final process. The virgin masks are bought from a company called Nanofilm®, and they are made on a 1 mm thick glass coated with 500 nm of chromium and 530 nm of photoresist AZ1518.

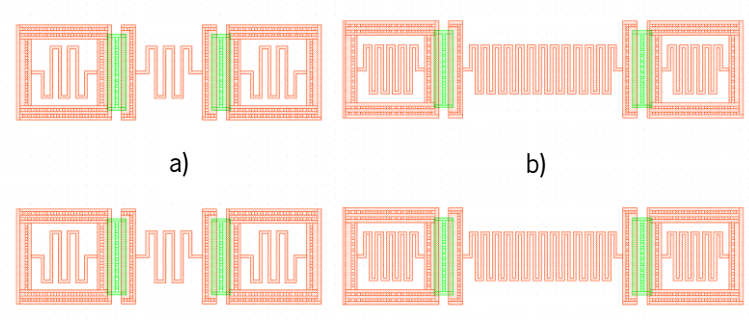


Figure 3.21. CAD drawing of the small antennas plates (red) for mask 1, and hinges (green) for mask 2.

The process to make a mask is described in Figure 3.22. First, the mask is exposed using a direct writing laser (DWL) machine. The structures and the alignment marks are exposed in a process that takes 4 hours. After that, the blank mask is manually developed for 90 seconds, followed by a chromium etching for 100 seconds, which is the time that this chemical takes to etch the full 530 nm with 50% of overetch, i.e. extra time to be sure that everything was properly etched. After this, the mask is dipped in acetone for 10 minutes (to remove the photoresist), then IPA for another 10 minutes to remove the acetone, and finally it is rinsed with DI water.

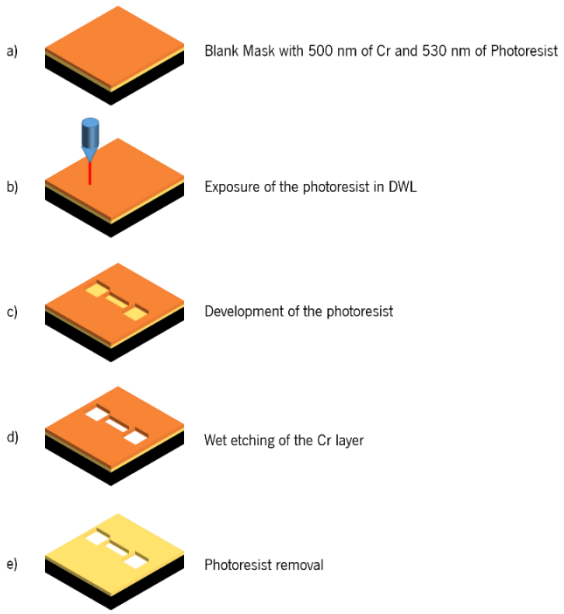


Figure 3.22. Mask process flow.

After this sequence of steps, the mask is ready to be used in the mask aligner. In case the masks have residues of photoresist on them, these can be removed with a solution called piranha. This solution is composed by 50% of a strong acid, in this case H_2SO_4, and 50% of a strong base, in this case H_2O_2. Mixing both generates a lot of heat and creates a very strong reaction when in contact with organic materials which does not attack metals. Since the photoresist is organic, this chemical removes all its residues without damaging the mask.

3.3.2. Standard cleanroom processing

The core process described in 2.3.2 is based on 4-inch wafers, but since the INL uses 8-inch wafers in its cleanroom, this was the selected wafer size. Apart from the thickness, which is not an issue (the 8-inch wafer is 725 µm thick while the 4-inch one is only 512 µm thick), the characteristics of the wafers are the same. Additionally, an 8-inch wafer can yield 4 times more devices than a 4-inch one.

In Figure 3.23, the final process flow is shown, and we can conclude that the similarities between the developed process and the original one presented in Figure 2.10 are high. The changes made to the process were mostly the materials used in the different layers. Nevertheless, every change can be critical in a process development. The sacrificial layer generated a lot of discussion when creating the process flow. Poly(methyl methacrylate) (PMMA) was used in previous works. At INL this material can be coated with a spin coater with thicknesses ranging from the hundreds of nanometres to a few microns. Nevertheless, the PMMA used in the cleanroom is dissolvable in acetone, meaning that if any lithography is placed on top of it, the PMMA will be cleared away when removing the photoresist. However, at INL, a PVA Plasma Asher removes photoresist without using acetone, but it affects metal layers. Considering the process flow proposed by the other authors, at least 4 different metal layers will be present in this microfabrication process, so using ashing to remove photoresist was out of the question. With this, the only option to remove photoresist was acetone, which meant that removing the first photoresist layer would greatly affect the PMMA layer, thus rendering this material an unsuitable solution in this process.

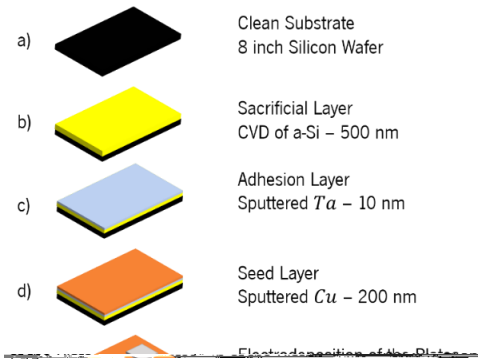


Figure 3.23. Microfabrication process flow for 3D self-folding structures adapted to INL cleanroom.

Amorphous silicon (a-Si) layers presented themselves as a promising solution, as they have fair uniformities, they can be patterned by lithography, they can be deep reactive ion etched on SPTS Pegasus, and, more importantly, they can be isotopically removed in SPTS Xactix quickly and with great undercut etch. An a-Si layer of 500 nm was, therefore, chosen as the sacrificial layer to replace PMMA. PECVD was the technique used to deposit a layer of such material. The reaction described in equation 3.8 occurs inside a chamber at a fixed temperature and pressure. This process normally occurs at really a high temperature, but with the help of a plasma it can be reduced quite significantly.

$$SiH_4 \rightarrow Si + 2H_2 \qquad 3.8$$

On the PECVD there were two different recipes for the same process, where the major difference between the two recipes was the working temperature. One was done at 150°C and the other at 300°C. In contrast with the temperature, both run at 950 mTorr of pressure. Two dummy wafers were deposited with a SiO_2 layer, and then the a-Si was deposited on top of it (Figure 3.24). This extra strep is needed because if an a-Si layer was deposited on top of a Silicon wafer, there would be no way to distinguish them in the interferometer measurement. The indication was that

the deposition rate of the material was 39.11 nm/min, so to deposit 500 nm, 12 minutes and 47 seconds were required. The dummy wafers were processed and the thickness results are presented in Figure 3.24.

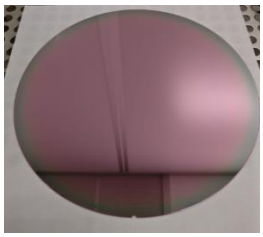


Figure 3.24. Wafer deposited with a-Si at 150°C.

Looking at both results in terms of thickness (Figure 3.25 a) and c)), the a-Si layer deposited at 150°C has a low non-uniformity of just 1.26%, while the one deposited at 300°C has a non-uniformity of 35%. On the other hand, depositing at a low temperature results in twice the residual stress, meaning that thick films deposited at 150°C will peel off quickly. So, there is a trade-off between the two processes: one is more stable and the other is more uniform. In this case, the 440 nm are good enough as a sacrificial layer, so the 150°C process was chosen.

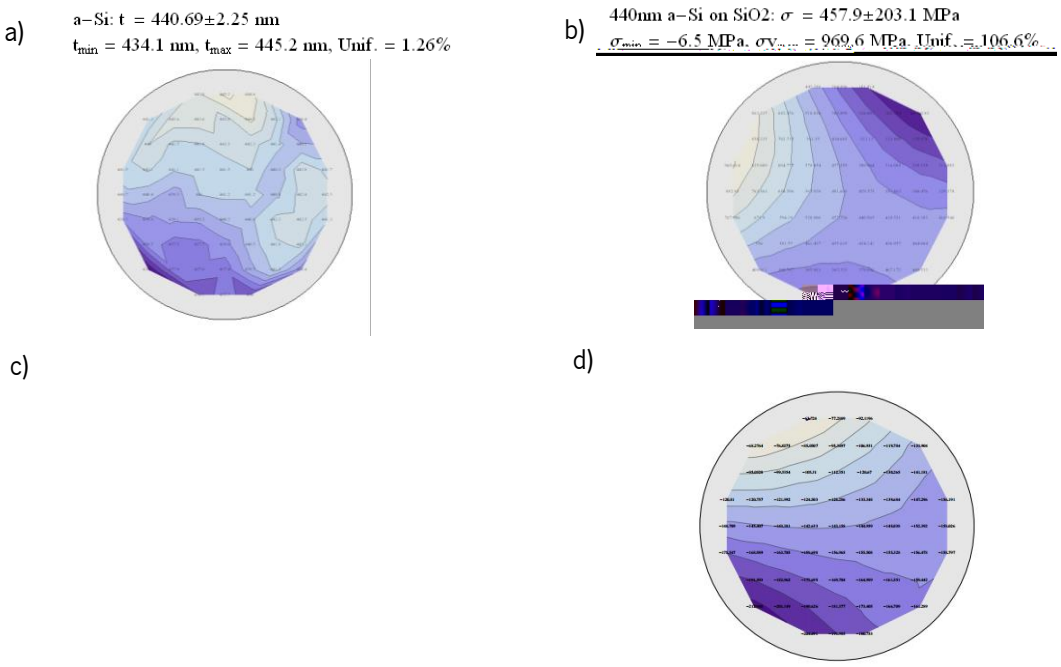


Figure 3.25. Thickness measurements (left) and Residual stress measurements (right) of two a-Si depositions at different temperatures, in the first row a-Si layer deposited at 150°C and on the bottom a-Si deposited at 300°C.

After the deposition of photoresist, the wafer is ready to go to the mask aligner. In the mask aligner, the wafer is placed together with the mask that is shown in red in Figure 3.21. The chuck holding the wafer lifts up and places the wafer in contact with the mask. This contact method is rough for the mask as it starts to get damaged, but it ensures a better resolution to the lithographies, and since the photoresist layer is quite thick, the high resolution is extremely important to obtain the small 15 by 15 µm holes. Additionally, all the mask aligner filters have to be removed to give the maximum UV power, in broadband, to the exposure.

The exposure dose for a 40 µm photoresist is 3762 $\mathrm{mJ/cm^2}$, therefore, since the light intensity of the lamp at that time was measured at 39.4 $\mathrm{mW/cm^2}$, the exposure time should be 95.48 seconds. If the full length of the exposure is performed all at once, the photoresist heats up and deforms with the generated air bubbles. Therefore, to avoid this, the 95.48 seconds were divided into 5 steps of 19.1 seconds, with intervals of 10 seconds between them.

After the exposure, the wafer needs to rest for 1h15min, as recommended in the datasheet. Then, the wafer goes back to the SUSS equipment, where a development process with AZ400K is performed. The process takes 240 seconds to fully develop the photoresist. After that, optical microscope photos were acquired to inspect the results. The first thing that was noticed was the presence of some particles on the bottom of the exposed photoresist (left side of Figure 3.27). To remove these particles, the wafer was placed in a DRIE tool to do a $\mathrm{O_2}$ clean of the wafer. When the photoresist is exposed to an $\mathrm{O_2}$ plasma, the material starts to be removed. This cleaning step is quite common when thick photoresists are used and it is called the DESCUM process.

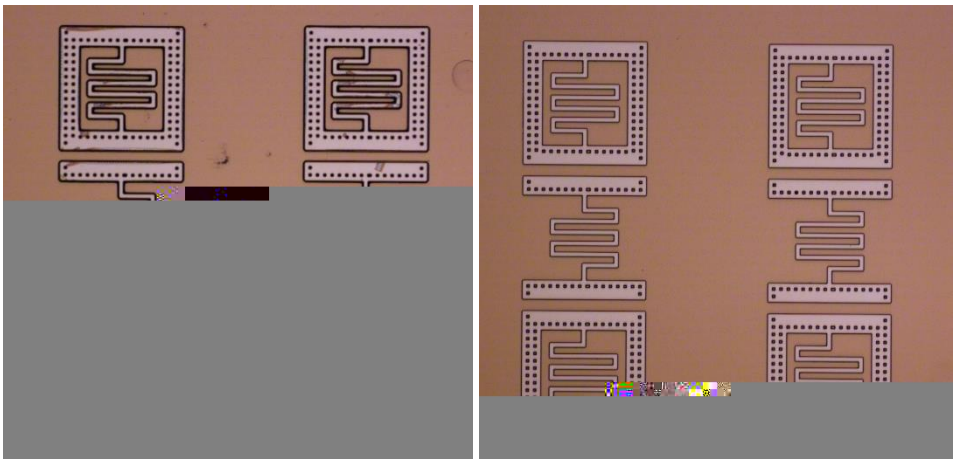


Figure 3.27. First lithography before DESCUM (left) after DESCUM (right).

Since the particles on the bottom are much thinner than the total thickness of the photoresist, they are removed perfectly without significantly affecting the photoresist itself (right side of Figure 3.27). Comparing with process described in [83], the only notable difference is the use of thinner photoresists, for the lithography step when compared with the current 40 µm thickness.

3.3.3. Electrodeposition

With the edges of the wafer and the plates of the small structure exposed, the wafer is ready to go to the nickel electrodeposition, where the goal is to deposit 10 µm of nickel.

Plating step details:

Exposed seed layer area, cm^2	1.18
Current density, A/cm^2 (2)	0.01
Estimated plating rate, um/h (3)	10.80152672
Target thickness, um (4)	10
Current, A	0.0118000
Plating time	3333 sec (56 min)
Corrective plating time, sec	0

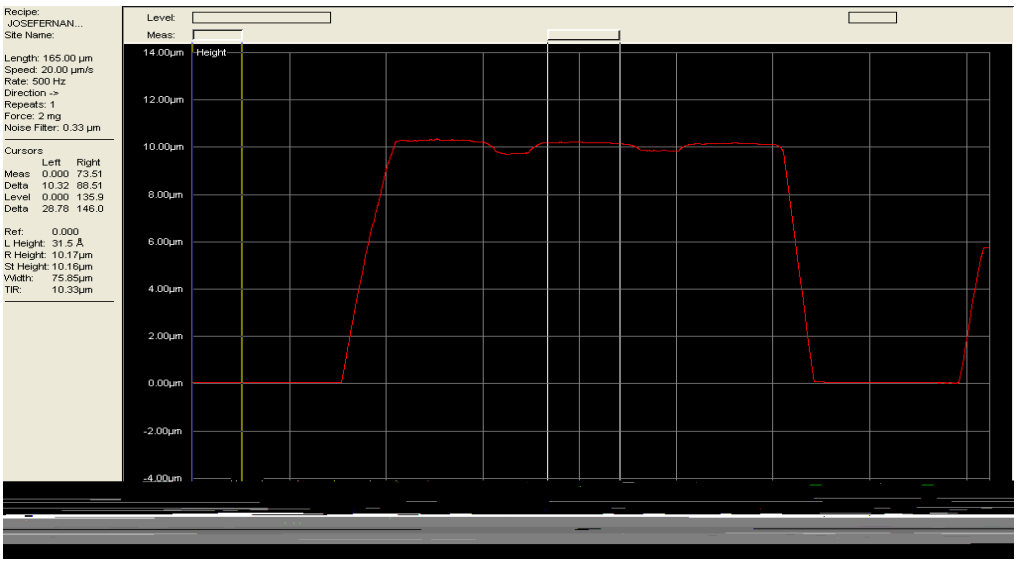


Figure 3.28. Electrodeposition of nickel: Electroplating parameters and optical microscope photo on top; Profilometer measurement on the bottom.

For the electrodeposition step, a lot of variables need to be known before the process can begin. Firstly, the exposed area needs to be calculated in order to relate this area with the current density that will be applied. Analysing the CAD file, the total exposed area was calculated and the value was 1.180 cm^2. In the calibrated system, injecting a current density of 0.01 $\mathrm{mA/cm}^2$ gives

an estimated plating of 10.8 µm per hour, meaning that the wafer should be dipped in the electrolyte for 56 min with a current of 12 mA to get a plating with 10 µm of thickness. The result of this process is presented in Figure 3.28, where an optical microscope photo and one profilometer measurement are presented.

The minimum value of thickness of 10.17 µm was measured at the centre, and the maximum value was 11.3 µm, at the border, meaning that the non-uniformity is approximately 10%. After the electrodeposition step, the photoresist needs to be removed to perform the second lithography. To do this process, the wafer is dipped for 10 min in acetone, then 10 min in IPA and finally rinsed with DI water. In the end, the wafer is ready for the next lithography step.

The lithography step to pattern the hinges is performed exactly in the same way as the previous one. The only difference is the mask used (Figure 3.21, in green). The process runs with the same recipes for coating with a 40 µm

developed in this work and the one that was made in the original author's laboratory: the original hinge layer was made out of leaded solder (Sn60/Pb40), which is no longer available for purchase due to environmental concerns. The workaround was using pure Sn electrodeposition. The main challenge was to understand if this change could affect the complete process flow, but it was concluded that the main difference would be the melting temperature in the self-folding step.

From the original authors' work, the SnPb should have a thickness of 15 µm, so this value was respected in the first tests (Figure 3.30). Later on it was found that a Sn layer of that thickness was not enough. After much experimental data trial and error, the thickness was fixed at 20 µm. This difference was attributed to the fact that the previous author was able to deposit a perfect T-shape hinge of SnPb, while our system deposited a pure Sn Y-shaped hinge.

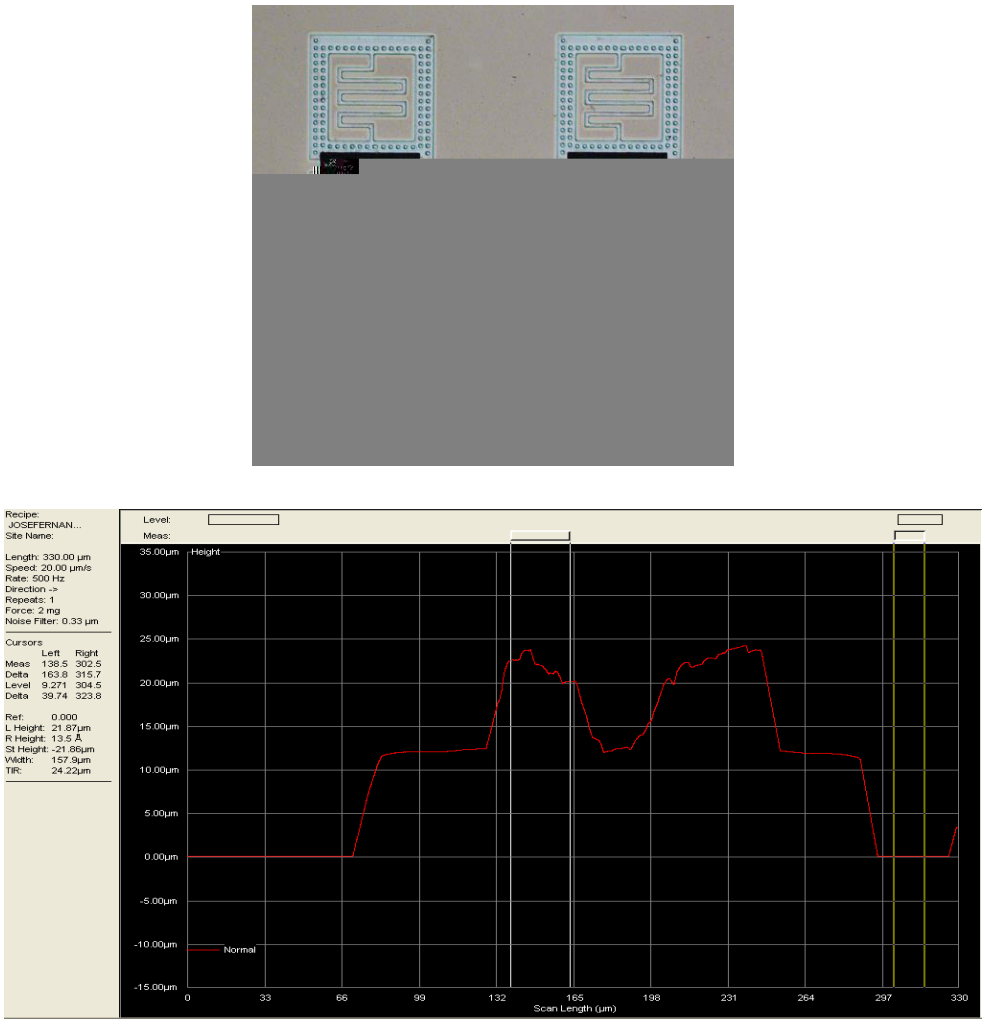


Figure 3.30. Tin electrodeposition: optical microscope photo (top); profilometer measurement (bottom).

3.3.4. Removal of the sacrificial layers

After the deposition of Sn, the structure is complete, as all the metal layers are deposited, and the next step is the release of these structures by removing the layers that are underneath them: amorphous silicon as a sacrificial layer, copper as a seed layer, and Tantalum as an adhesion layer for the seed layer. These layers need to be removed from the top to the bottom, starting with a copper etch. Wet etch is the only available technology that allows for isotropical copper etching. To perform this step, a chemical compatibility test was made to verify what chemical could be used to dissolve the 200 nm of Cu. At the INL, these copper layers are generally removed with a chemical called Aluminium etchant, as this etchant is suited to remove metals such as aluminium and copper. One sample was dipped into this chemical to understand if the Ni or the Sn layers would be etched. After a couple of minutes, it was obvious that this chemical attacked both Ni and Sn and didn't remove the copper entirely, as seen in Figure 3.31. Therefore, Aluminium etchant was not suitable for this experience and a new chemical was bought to etch copper.

Figure 3.31. Left: Sample dipped in Al etchant for 2 min; Right: Close up on the Ni structure attacked by Al etchant.

The new chemical, called copper Etchant 49-1, was bought from Transene®, and after analysing their datasheet, they confirm that their etchants can be used in the presence of other metals, like solders, gold, nickel and complex alloys. This chemical can be used at room temperature, but it increases its etch rate if the temperature is increased. Typically, this etchant has a rate of 4 nm/s, so 50 seconds are required to etch the 200 nm thick seed layer. The authors of [83] use the APS-100 copper Etchant from the same supplier, but the official data of the chemical states that it is not compatible with nickel, therefore it was discarded as a viable option.

The solution was heated to 40°C and the process was done for 150 seconds (the triple of the required time, because the undercut etch has a much slower etch rate). After that, the sample was analysed under the microscope and the results were much better than the ones shown in Figure 3.31. In Figure 3.32, it is possible to see that the colour of the substrate changed considerably, meaning that the copper layer was etched. The devices were still attached to the substrate, but there was no visible copper and no visible damage to the Ni and Sn layers.

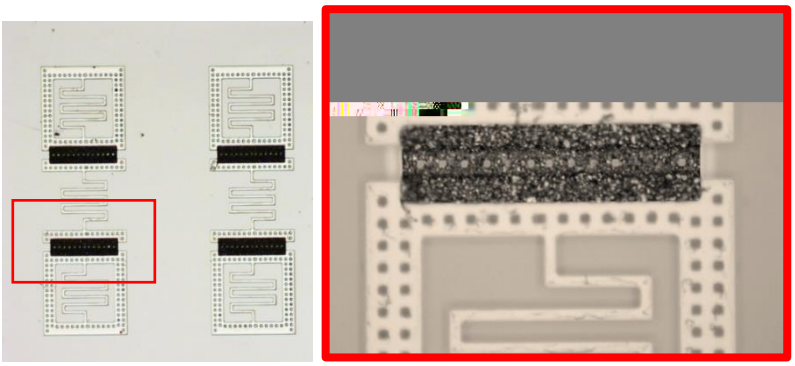


Figure 3.32. Sample after seed layer removal, and zoom on the main layers of Nickel and Tin.

After removing the copper, there were only two layers left that separate the devices from the original substrate: tantalum and amorphous silicon, both removable with XeF_2. The samples were placed in the SPTS Xactix, and a cyclic recipe of 30 seconds was used. Since the objective was to remove all the sacrificial layer, 50 cycles were performed to ensure the complete separation of the samples from the substrate. Then, these samples were transferred to an IPA container to store them before the folding step. As visible in Figure 3.33, the samples still have traces of the copper layer on their backside. Nevertheless, this should not affect the folding step, as this layer has less than 200 nm of thickness. The samples are now ready for the most critical step of the process, the folding.

Figure 3.33. Several devices released after XeF_2 etching.

3.3.5. 3D Folding

The presented folding step was inspired by the original work, but some changes were absolutely necessary. Firstly, the hinge material is different, meaning that some changes will occur during the folding process. The temperature has to be different, because Sn does not melt at 180°C like the SnPb alloy that was electrodeposited in the original work. The temperature to melt Sn should be at least 250°C. Additionally, NMP (the chemical used in the original process) can't be used in the INL cleanroom for safety measures, as it is highly aggressive for human health and evaporating it can be dangerous not only to the operator, but to all the cleanroom users. Benzyl ether, an organic liquid, was chosen as an alternative bath solution. This chemical only evaporates at 300°C, it is not harmful for the human body and it is a cheap solution that is likely suited to the developed process.

The samples were dipped in Benzyl ether, mixed with 5 ml of liquid flux. Then, the solution was heated to 100°C and it was kept at this temperature for 5 min, evaporating the flux and destroying all the oxide layers in the Ni plates and Sn hinges. The temperature was then increased to 200°C and kept constant for 5 min. These waiting times are required to ensure a homogenous temperature of the solution. In the end, the temperature was raised to 260°C, and this temperature was maintained for another 5 min. Finally, the solution was cooled down to room temperature and the devices were extracted.

After analysing the dozens of structures in the solution, it was possible to conclude that only some of them achieved the required 90° angle. The others had random folding angles, both lower and higher than 90°. As mentioned before, it is known by experimental results that the volume of the hinge defines the final resting position of the moving plate, meaning that the different angles can be related to different volumes of the hinge in the different samples. The fair uniformity and low control of the Sn plating step are probably the root cause for such results in folding angle uniformity. In Figure 3.34, the two types (a) and b)) of antennas with correct folding can be observed; in c) two devices got attached to each other, as the Sn worked like a glue between metals. In d) a fully folded structure is seen from the top, where the copper can be observed. As predicted, the copper does not have any influence in the folding step. Making this proof of concept is highly important and promoted a lot of mistakes, errors and calibrations that will not influence the next fabrication processes.

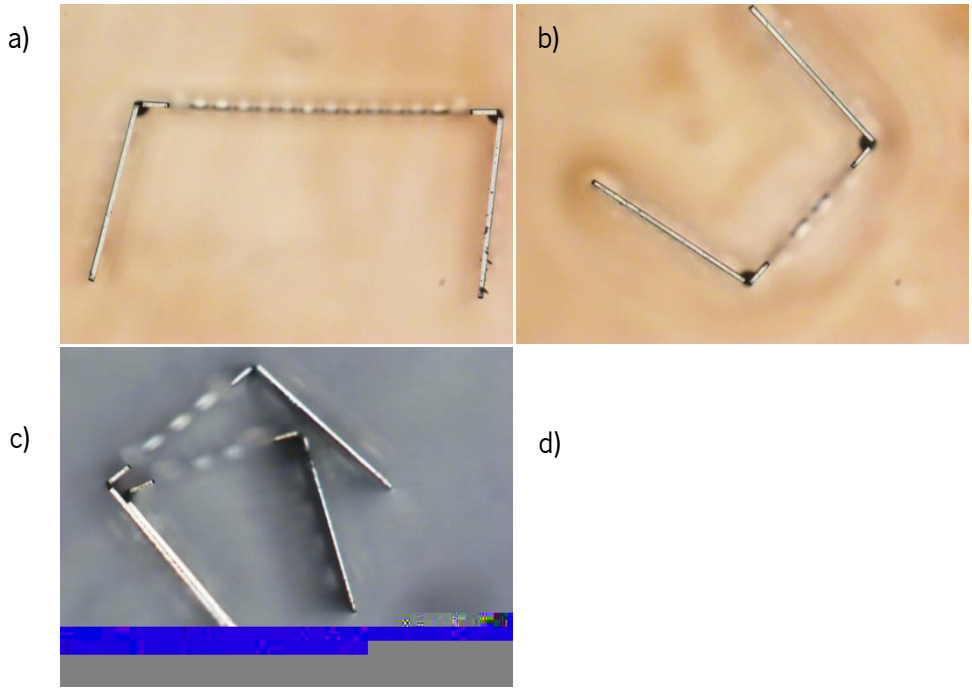


Figure 3.34. Examples of devices after the self-folding process.

3.4. Conclusion and process comparison

The implementation of a self-folding process in a new cleanroom with different equipment and regulations was successfully achieved. From the beginning it was known that replicating the exact same process would be complicated. Machines and materials used in different fabrication centres are not the same and some adaptations had to be made, yet none of these proved to be critical for the self-folding application. Looking to Table 1, one of the most important differences relies on the sacrificial material that was changed due to incompatibilities with the INL cleanroom. The hinge material was also changed: the electrolyte for SnPb deposition was discontinued from the market in several suppliers, so a new solution was used: pure Sn hinges. Changing these two materials was tricky, but after some calibration and experimental iterations, the achieved results were quite similar between processes.

Table 1. Material comparison of the two processes

Materials used	Original process as described in [83]	Developed process
Substrate	4-inch silicon wafer	8-inch silicon wafer
Sacrificial Layer	PMMA with 5 µm	Amorphous Silicon with 500 nm
Adhesion Layer	Chromium with 30 nm	Tantalum with 10 nm
Seed Layer	Copper with 150 nm	Copper with 200 nm
Photoresist	SPR220 – 10 µm	AZ9260 – 40 µm
Device Plates	Ni – 10 µm	Ni – 10 µm
Device Hinges	SnPb – 15 µm	Sn – 20 µm

In conclusion, the original process was successfully transferred to the INL cleanroom, and both processes originated the same structures. This is not only an important step for this project but also opens doors to new and innovative processes that can be done in the cleanroom for MEMS and biomedical applications. Again, this process is not the objective of this work, but the proof of concept was necessary before proceeding to more complex stages. Fortunately, all the decisions made in the process flow did not affect the device fabrication and these were obtained (like in previous works) in an aqueous medium. As mentioned before, it is hard to characterize and measure such devices operating as antennas, so the need for a more complex, out of the box process becomes a priority for the future of this technique.

Chapter 4. Integration case studies

MEMS and NEMS are a trend in the micro and nanodevice research field, and creating such structures generates numerous possibilities that bring new opportunities and applications that were, until now, unthinkable of. This market of building sensors and actuators is, since the 90's, a trend that already resulted in products ubiquitous in our daily life [87], [88]. Smartphones, smartwear and medical equipment are just a fraction of the full market where MEMS are extremely relevant. Airbag accelerometers, microphones and blood measurement devices are additional examples of devices that changed the world and that we use every day. With the ability to sense and actuate at the microscale, those devices englobe a lot of knowledge, such as integrated circuit design and mechanical, material, chemical, fluid, optical and electrical engineering. Microfabrication of such devices is the speciality of the INL cleanroom, which gives a lot of opportunities for this project. NEMS nanofabrication is limited to the research field for now, but in the future it will most definitely be the dominant approach to build complex sensors and actuators [47], [87].

After fully implementing the self-folding process, the next step relies on the elaboration of a new and complex process where the same structures will end up attached to a substrate. With such process, the self-integration of complex designs becomes a reality in the fabrication step. For that, some case studies were considered to validate the process and understand how far this technology can go. It is believed that such out-of-plane devices will bring forth new possibilities for MEMS applications.

In this chapter, simulated devices are shown in order to understand which kind of systems will be implemented in the final process [47]. An actuator based on thermal expansion, a 60 GHz antenna, and a 36 GHz antenna will be designed to be included in the self-folding fabrication process.

4.1. Thermally actuated micro tweezers

Thermal actuation is a well know technique to generate large forces and produce movement in MEMS. The actuation of such devices is based on the thermal expansion of different materials. Usually, these thermal devices are electro-thermal actuators, meaning that an increase of the

The heating power (Q) generated is proportional to the product of the resistance (R) with the squared injected current (i), and is given by:

4.9

The resistance of a given object is given by:

4.10

Analysing equation 4.10, the resistance R (Ω) is given by the electrical resistivity ρ (that is measured in Ω.m) multiplied by the ratio of the length: l (m); with the section area: A (m

becomes easy when all the material properties are known. The following equation shows how the length variation (ΔL) is directly related with the heat generated by the Joule effect [90].

$$\Delta L = \frac{\alpha . Q . L_i}{Cp} \qquad 4.14$$

In principle, L_i, α and Cp are the same for both of the arms, and their expansion depends only on the generated heat. Since this value is only dependent on the section area of the arm, the thin arm expands more than the thicker one. The asymmetric configuration uses this difference between arm expansion as a promoter for the enhanced movement of the actuator. If the thin arm expands more than the thick arm, it will be generated a movement in the Y-axis, as shown in Figure 4.1. Before proceeding to fabrication, a complete simulation of the device needs to be implemented. A finite element software, named COMSOL®, was used for this propose. In COMSOL®, multiple physical domains can be combined in the same simulation in order to understand how devices will work once fabricated. This process, as previously referred, was made only as a proof of concept, so in principle the device itself could be optimized to achieve better results. However, since this was not the objective of this project, a simple design was adopted.

The 3D design of the device was made by an iterative experimental procedure. Therefore, some dimensions were changed during this process in order to achieve better results. To make things work, a parametric process of changing dimension after dimension was done in order to get the thermal actuator to work properly. Not every performed simulation will be described in the following pages, only the ones of more interest for this project. The most restraining step for this device, dimension-wise, was the electrodeposition of nickel. Since until now the smallest feature that had been electrodeposited with the new system described in chapter 3.3 was measured at $15\ \mu m$ of width, this was adopted as the smallest feature size.

Three features were tested in the parametric sweep: the length of the thinner arm, the length of the thicker arm and the width of the thinner arm, these three measurements are shown in Figure 4.2. The values on the same figure presents the model which achieved the best results. Analysing it, the minimum feature size, 15 μm of width, was respected. The thickness of the device is 10 μm and its arm length is 815 μm. The model consists of the device attached to three nickel pads with a Sn layer between them, all of this on top of a silicon block. This full system was placed inside an air box of 30x30x30 mm to simulate real test conditions.

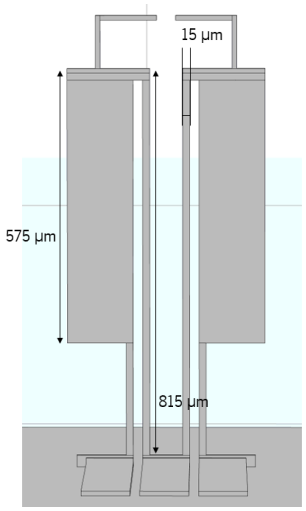


Figure 4.2. Thermal actuator designed in COMSOL after parametric simulation.

The materials of each component are shown in Figure 4.3. The Sn is only used on the junctions between the pads and the device itself, and the silicon is the support, while the rest of the device is made of nickel. The model was composed by three main physics interacting with each other. The "Electric Currents" module describes how a current will pass through the device, considering the resistance of each material and the conductance between interfaces. The "Heat Transfer Module" is the module that will deal with temperatures, mainly with the influence between materials when they are at different temperatures. The last module, called "Solid Mechanics", will calculate the different displacement and deflection of the materials when the forces are applied to them. These three modules are connected with different Multiphysics: one that connects the electrical part with the temperature by the joule effect, and another one that connects the temperature with the solid mechanics through the strain equations. In the end, this simulation makes a full relation between the injected current and the displacement of the different materials.

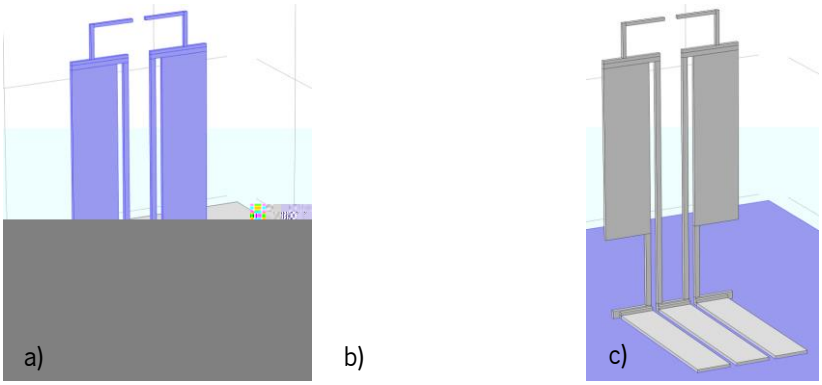


Figure 4.3. a) Nickel (Ni) objects in simulation; b) Tin (Sn) objects in simulation; c) Silicon (Si) objects in simulation.

Table 2. Simulation Parameters.

Parameters	Electrical Conductivity	Heat Capacity Cp	Density	Thermal Conductivity k	Relative Permittivity	Young's Modulus E	Poisson's ratio v
Units	S/m	J/(Kg.K)	Kg/m3	W/(m.K)	-	Pa	-
Nickel (Ni)	9.86×10^6	445	8900	90.7	1	219×10^9	0.31
Tin (Sn)	9.56×10^6	228.05	7300	65.19	1	48.8×10^9	0.36
Air	-	1015.17	1.203	0.0256	-	-	-
Silicon (Si)	-	678	2320	34	-	160×10^9	0.22

With these three modules, it is easy to understand what the needed parameters for each material are. Regarding the electrical conduction, the only relevant materials are the Ni and the Sn metals. The Air box will only be used for the heat transfer between the device and the air, so only the thermal parameters are needed for this material. For the silicon, since it works as the fixed structure in the simulation, all of its mechanical properties are needed and, since no electrical current will flow through it, the electrical parameters were ignored.

Most of the chosen parameters were already present, as a standard value, in the software. Most of them suffer some variations with the temperature, and this is implemented in the simulation. The values presented in Table 2 are all for a room temperature of 20°C, so when the simulation starts, with the increase of the temperature, these values change. Some direct conclusions that can be seen in Table 2 are for example in terms of temperature: air conserves a lot more heat than the other materials, because its Cp is the highest. The thermal conductivity (k) is the lowest, meaning that the heat in the air takes more time to be transferred to other materials. For the electrical parameters, the nickel conductivity was extracted from the measurements made in the Electrodeposition setup chapter. There, a resistivity measurement of the thin film was made, considering that the conductivity is inversely proportional to the resistivity, the conductivity of such thin film is 9.86x10^6 S/m. This was the only parameter that was changed from the standard COMSOL parameters, and the others were kept as is in order to get the better results out of the simulation.

It was assumed that the device is electrically isolated from the silicon wafer. Consequently, for the electrical component of the simulation only the Ni device, the Ni pads and the Sn interconnections were considered. In this module, the electrical current is conserved without any losses to other materials. The central pad is connected to ground, i.e., zero volts, and the adjacent pads are connected to a current source. The initial values were fixed at zero volts. The solid

mechanics module was applied to the device and the silicon substrate. The air was ignored as the only displacement that needs to be measured is the displacement of the device. In this module there is a need to define what is fixed and what can move, and the only constrain applied to the system was at the bottom of the substrate, therefore all other materials can expand in every direction. All the objects are in a stationary position in the beginning with no forces or movement in any direction. The heat transfer module was applied to every object in the simulation, air included. The initial temperature applied to the system was 20°C, and on the air box the extremities were fixed at 20°C. Fixing this temperature gives the air box an approximation to an infinite box, because the air will work as a heat sink. If this temperature is not fixed, the simulation software will assume that the walls are isolated, and the box of air will heat up and retain all the heat of the system.

Before simulating, the mesh needs to be well defined, as it is the most important parameter of every simulation. The mesh is composed by an array of elements that will define the required geometry. In each of those elements, the software will make the calculation considering them as one single point. This means that the thinner the mesh is, the more time consuming the simulation

After the meshing, the next step is the definition of the study to be made on the system. This study will be parametric to inject different currents and allow us to observe what happens in the system. This current is the only input that can change in the system. The outputs will be, for each mesh element, a temperature, a voltage, the measured stress and a displacement. For each injected current, these values can be measured and compared.

4.1.1. Displacement analysis

Like every thermal actuator, one of the main purposes is to create movement when an electrical signal is applied. The displacement of the device can be used for several applications, but in this proof of concept device, the displacement itself is the main goal. These micro tweezers open when an electric current is applied, and close when it is turned off.

The displacement of a given point in the Y-axis was determined by this simulation, and looking at the graph in Figure 4.5 it is possible to see that the displacement increases with the injected current. Nevertheless, this is not necessarily the best result, as the simulation software does not know the physical limits of the material, and this displacement is given only by the stress and the temperature of the material. So, for this displacement, there are physical restrictions that will be analysed in another study.

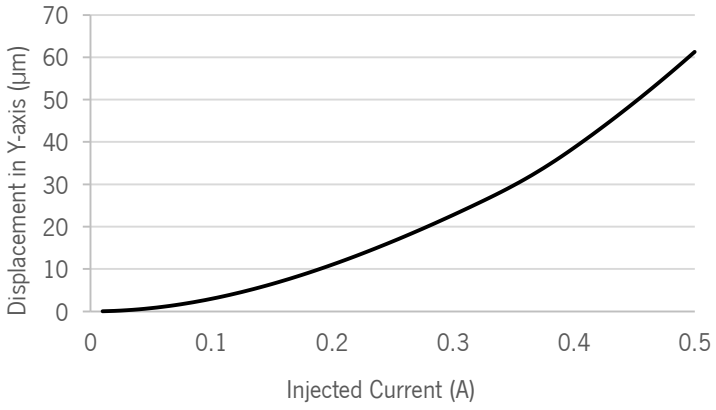


Figure 4.5. Displacement of a given point in the Y-Axis.

In Figure 4.6, the full displacement of the device as a function of the injected current is shown. In the image, the colour device is stressed after injecting the current, and the black lines show the device's original position for comparison purposes. After analysing both graphic and image, some remarks about this device can be made: only after injecting 190 mA a 10 µm

4.8, the voltage measurement results are shown on the surface of the device, where we can see the voltage decaying as the current goes from the source to the ground. In the end, after the device's fabrication, the measured resistance will be compared with the simulated value.

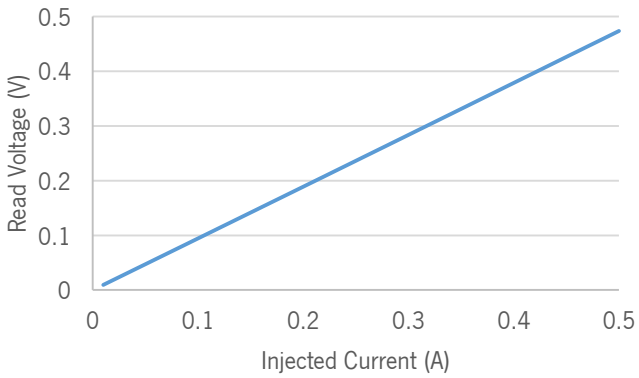


Figure 4.7. Current vs Voltage Graph; Value of voltage obtained on the simulated pad, the current is fixed in each simulation.

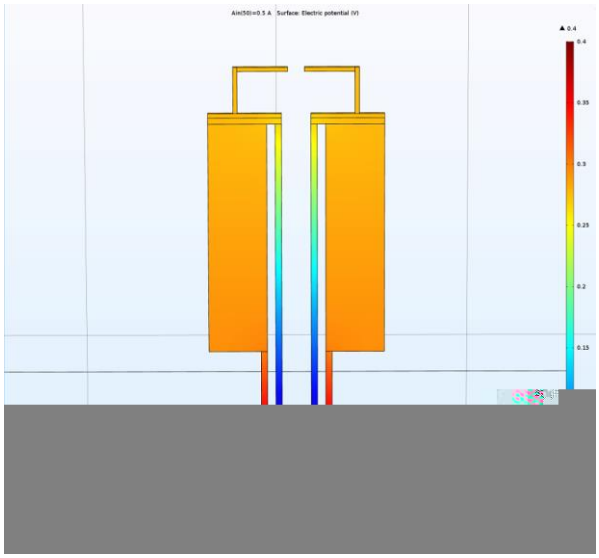


Figure 4.8. Voltage distribution in the thermal actuator when 250 mA are injected.

4.1.3. Stress analysis

When mechanical solids expand, the generated forces create stress in the materials. This stress deforms the material within its elasticity point, until it gets to its breaking point. This breaking point depends on the material that is being stretched or compressed, and it's called ultimate tensile strength.

Table 3. Ultimate Tensile Strength in different nickel electrodeposited thin films [91].

Ultimate Tensile Strength (MPa)	
Watts Nickel Solution	Sulfamate Solution
345 to 485	415 to 610

For the bulk nickel, the tensile strength can reach values of up to 600 MPa [92], but when this material is electrodeposited, this value can be lower. In Table 3, the maximum values of stress for two different solutions are shown. When a Sulfamate Solution is used, the mechanical properties of the nickel quality are considerably better than when a Watts nickel Solution is used. In this project, and as mentioned before, a Watts nickel solution will be used, therefore these mechanical properties are inferior, thus fixing the maximum stress at 345 MPa. So, this will be the first big restriction of our device.

The stress measurement, with the help of COMSOL, gives us a full overview of this variable on the critical points of the device. In Figure 4.9, the critical points are shown in a 3D perspective. These critical points are the places where, if this stress is higher than 345 MPa, the structure will break. The thin arms of 15 µm are not only the most flexible part, but also the critical points of this device. In principle, this will be where the mechanical failures of the device will occur. So, an analysis was made to the arms, to understand which values of stress are measured when the current is injected.

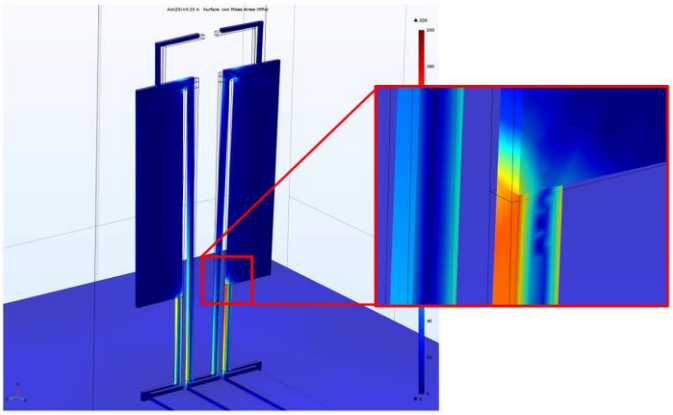


Figure 4.9. Stress map of the structure after injecting 250 mA.

In Figure 4.10, the maximum stress measured is shown for each injected current. The value of 345 MPa (maximum nickel electrodeposited stress – dotted line) is obtained when 380 mA are injected in the device, meaning that the thin arms will most likely break if the current is increased

beyond that value. The bulk material's ultimate tensile strength (maximum stress - dashed line) is not exceeded even with 490 mA injected into the device.

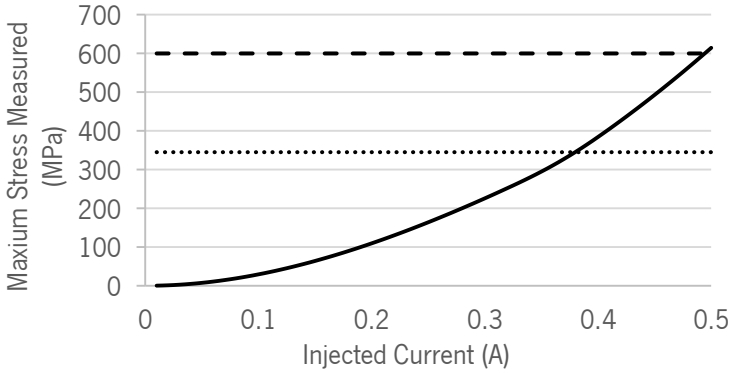


Figure 4.10. Continuous line: Maximum stress measured in the thin beams of the device; Dotted line: Maximum value of stress for a Ni electrodeposited thin film with a Watts Solution; Dashed line: Maximum value of stress for bulk Ni material.

This restriction is extremely important when testing the devices, and with such results we conclude that in the real device the 380 mA input current shouldn't be exceeded, meaning that the maximum displacement is limited to a maximum of 34.754 μm in each arm.

4.1.4. Temperature analysis

Since temperature is the variable that will generate the expansion of the material, and therefore cause the main movement of the device, it is extremely important to have it under control, meaning that knowing the temperature is a key parameter to having a working thermal actuator. Additionally, there are restrictions in the material properties: if a certain temperature is exceeded, the material can melt and the device is destroyed.

Observing Figure 4.11, it becomes evident that, as expected, a lot more heat is generated in the thin arm than in the thicker arm. The air that is surrounding the device is its only heat sink, so the temperature is dissipated slowly and the device is heating a lot. This heating is the displacement precursor, therefore this should translate into more displacement. In [93], the authors tested the nickel thin film melting points from 5 nm to 2 μm of thickness. What they concluded was that after 1.5 μm the sputtered thin film only melts when its temperature exceeds 1452.85°C, which is also the bulk nickel melting point. But, when electrodepositing a thin film, the porosity of the layer can be quite higher than a layer that was sputtered, and it can include other components

on the nickel layer composition. In principle, the electrodeposition system should be depositing pure nickel and not nickel alloys, but the porosity is an issue that must be taken into account.

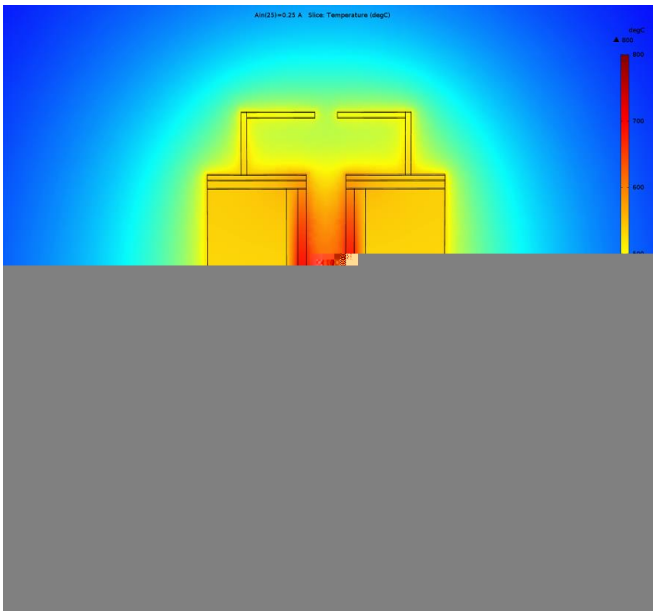


Figure 4.11. Simulated temperature in the device after injecting 250 mA.

Looking at Figure 4.12, this restriction of temperature for the bulk nickel material is only exceed when 490 mA are injected in the device.

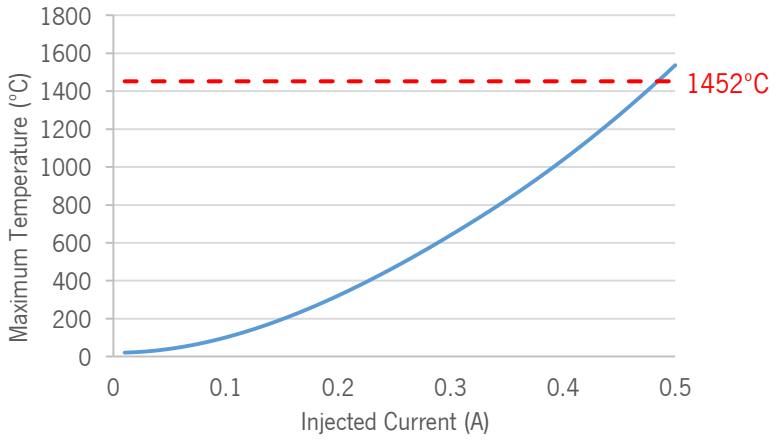


Figure 4.12. Continuous line: Maximum temperature measured on the beam of the thermal actuator; Dashed line: Maximum temperature of a Ni thin film in the literature [93].

4.1.5. Final device analysis and design

Using a standard asymmetric thermal actuator, we will theoretically be able to show an out-of-plane actuator working like a micro tweezer. This simple design will be able to move

approximately 35 µm per arm, and the main restriction is the stress measured on the thin beams. This stress, which occurs after injecting more than 380 mA, surpasses the maximum tensile strength of the material, and will probably cause failures that will break the device.

Using the simulation, the device was designed in CAD in order to transfer it to the process flow with the use of lithography steps. Considering Figure 4.2, the main dimensions were respected and the device design was obtained in Figure 4.13. Two different designs were made, one with larger distance between the two arms of the tweezer and one with the ones that were simulated. As it was mentioned before, the hinges are the critical point of the full self-folding process, and that being said, respecting the design rules is the most important step. In both cases, the design rules defined in chapter 3.3.1 were respected, meaning that the hinge should measure 80% of the attached plate. But since a new hinge was being made for the first time in design a), with 160 µm, the b) option was done to be sure that on the end, if design a) fails, the hinge design that is already proven to work will not fail.

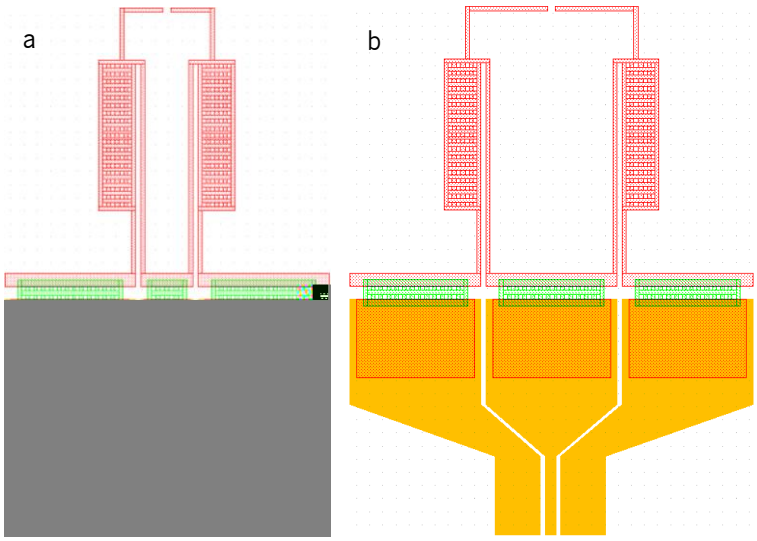


Figure 4.13. a) Simulated thermal actuator design, with two hinges of 400 µm and one with 150 µm b) Design with three hinges of 400 µm.

The three different masks are shown in different colours. The anchors that will be patterned in the first lithography are represented in yellow. This design was obtained respecting a pitch of 50 µm and it was based on pad connectors used in different fabrication processes at the INL. The nickel plates are represented in red, and these respect the simulation dimensions. The thicker arm, however, will also have the small 15 x 15 µm holes to make it easier to remove entirety the sacrificial layer located beneath the device. This change will affect the device since the total cross section

area of the thicker arm will be smaller, meaning that its resistance will be higher. As explained before, the resistance of the device is the most important variable that will determine the final displacement of the thermal actuator. It is expected that, in the end, this device has more resistance than the simulated one, so the displacement can be even greater.

4.2. 3D On-wafer antennas

Besides the previous thermal actuator, two different 3D antennas were also fabricated to test the process's flexibility.

4.2.1. 60 GHz Small cubic antenna

The small cubic antenna was originally reported in [12], and it will be implemented in this fabrication technology. The 3D U-shaped antenna has a meander lie in the middle of its panels, as this approach increases the electrical length of the antenna, thus decreasing its resonant frequency at the expense of radiation efficiency. The antenna was designed to have 50 Ω of impedance and work at 60 GHz. The miniaturization of such a device is a major improvement when the objective is the integration of this data and power receptor with other implantable micro devices. The design of the antenna in the simulator is shown in Figure 4.14.

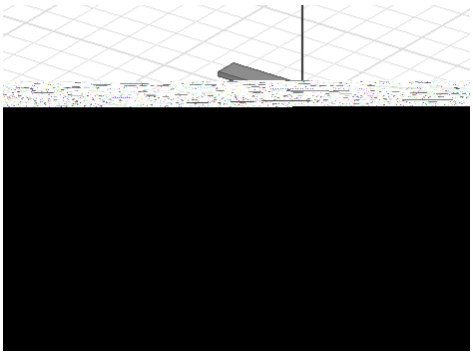


Figure 4.14. Small U-shaped antenna designed in [12].

The characterization of these small devices was reported to be quite difficult because the small antennas were obtained in an aqueous medium and, therefore, an interface board had to be designed to connect the antennas to measurement equipment as seen in Figure 4.15 [76] . Given the antenna's reduced dimensions, the interface board interferes with its characterization.

Consequently, it was of significant interest to fabricate these antennas already integrated with a much smaller transmission line.

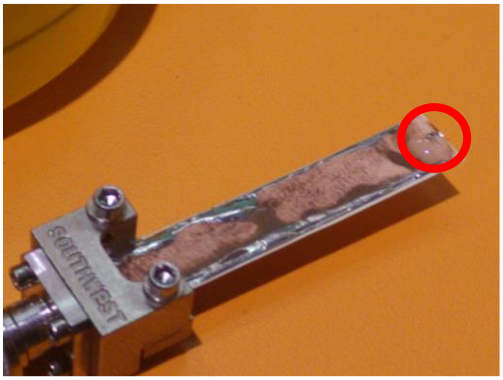


Figure 4.15. Small U-shaped antenna (inside the red circle) connected to the interface board.

The antenna's design was transferred to the CAD software to convert its pattern to the lithography masks.

In Figure 4.16, the small antenna was deconstructed into its 2D planification with an anchor that will be used to connect the small device to the substrate. The approach to achieve the self-assembly of the antenna was to separate one of the antenna's faces from the others, as shown in Figure 4.16. This was done to ensure that all the faces will be connected to the substrate. The hinge material, presented in green, is placed on the ends of the top plate and in one of the lateral plates (represented in red), in such a way that when the hinges fold to 90° the two will connect and close the U-shape structure, as depicted in Figure 4.17.

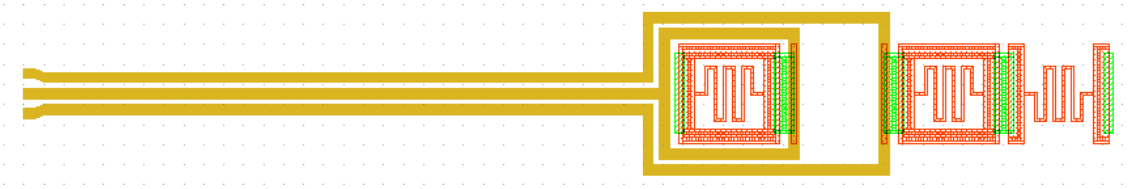


Figure 4.16. Transferred antenna pattern to a CAD design, along with the transmission line.

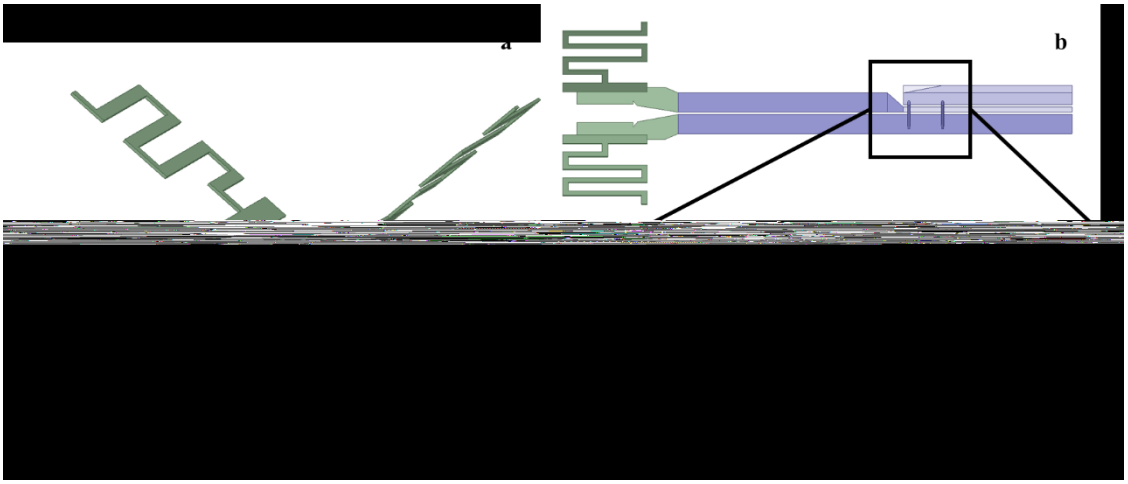


Figure 4.18. Meander dipole antenna. Inset: detail of the CPW-CPS transition.

On this case, the antenna is a dipole, so the folding step is not as complicated as the U-shaped antenna described before. The structure is composed by two independent metallic meanders that will be lifted like is it shown on Figure 4.18 a). Being that said, the design consists on the CAD showed in Figure 4.19. On the image, the red layer represents the meanders, the yellow layer the transmission lines and in green the hinges that will fold the structures into different angles.

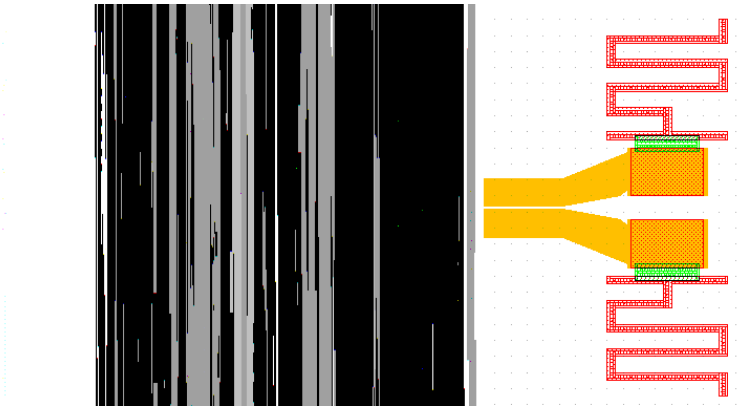


Figure 4.19. Transferred antenna pattern to a CAD design, along with the transmission line.

Since this electrical connection will be of great importance in the future, a passivation layer between the anchors and the substrate is needed in order to isolate the devices from the silicon itself. This passivation layer will be done with Al_2O_3, an oxide layer used in many devices fabricated with cleanroom processes. The passivation layer for isolation proposes, will be the first step of the process, then a new seed layer (and respective adhesion layer) will be deposited. After the silicon sacrificial layer is grown on top of the stack, the first lithography step is done with mask number one. Then, with DRIE, the amorphous silicon is opened and the seed layer gets exposed. The first electrodeposition of nickel is then performed, and the Ni anchors will grow to the same thickness as the sacrificial layer. After this new implementation, the rest of the process is completed with the fabrication of the device itself. Being this a new process, it is hard to know and understand if this anchor will have any direct influence on the folding step.

To add more variety and demonstrate the unlimited number of applications this technology can produce, the different devices shown on Chapter 4 will be implemented. The full complex process is shown in Figure 5.1.

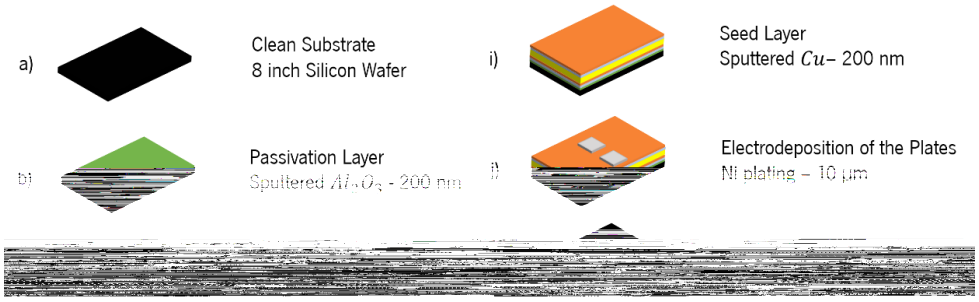


Figure 5.1. Final process flow for the microfabrication of 3D self-folding devices on top of silicon substrates.

5.2. Anchored process flow

With the usage of the fabricated tools for electrodeposition and the tools described in Appendix 1, the fabrication steps were iterated one by one, and like in every other process, some measurements were made in between. Many calibrations, measurements and adjustments were made through the process and, eventually, a good and reproducible process was developed, and it will be described in the next sub-chapters.

5.2.1. Masks

The first thing to do is the writing of the lithography masks. For that, the DWL system was used and the drawings obtained in the simulation chapter were implemented. The proof of concept devices were the two small antennas for wireless communications and the out of plane thermal actuator. The design of these small devices was translated to CAD software and then to the DWL for exposure. In the lithography process, it is also important to remember that alignment marks will be necessary when processing these wafers. In Figure 5.2, the alignment marks implemented in the overlapping masks are shown. Mask number one is presented in yellow, and no alignment is needed prior to being exposed.

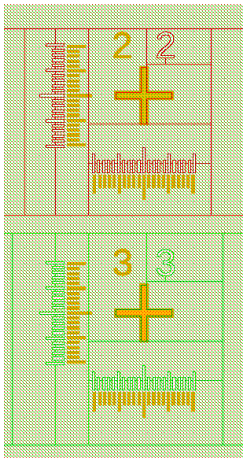


Figure 5.2. Alignment marks used in the process masks.

The mask that will contain the plates of the devices is presented in red; in this mask there is a matching cross in the middle a grid for the left and right alignment, and another for top and bottom alignment. With this grid, it is possible to observe how misaligned is the sample after doing

the lithography process, since each bar of the grid represents 100 nm. The third mask is similar to the second one, and a cross and two small grids are used to align it with the first layer.

The mask process is well calibrated, and following the INL guidelines it is possible to quickly process it. The mask for the anchors (mask number one) required 2h29min of laser writing to complete, while the second mask required 2h38min and the last one, for the hinges, took 1h34min. This last mask is less dense than the other two, so this explains the shorter time that the laser took to write it. After having the masks ready, the process was started in 8-inch wafers.

5.2.2. Substrate passivation

The silicon wafers used in the cleanroom are produced by "Silicon Valley Microelectronics - SVM", and their characteristics are shown in Table 4. As it is shown, the resistivity is not that high, meaning that a shield layer should be used to avoid electrical losses.

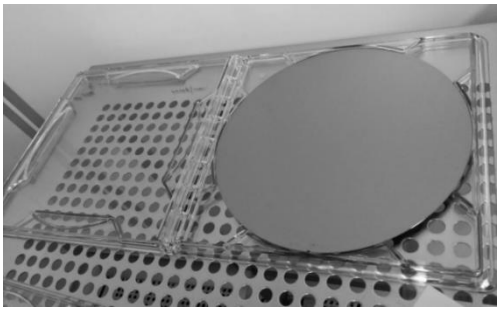


Figure 5.3. Blank silicon wafer used in the process.

Table 4. Silicon Wafer characteristics.

Parameters	SVM silicon wafer
Diameter	200 mm
Type	P/Boron
Orientation	<100>
Resistivity	1-100 Ohm.cm
Thickness	725 ± 25 µm

Building complex electronic devices on top of silicon requires a passivation of the substrate. Silicon is a semi-conductor material, meaning that if the device is fabricated on top of it, current losses and parasitic capacitances will appear. For that end, an isolating material is needed. In the literature [94], [95], some examples are given, but the most used ones are oxided. Oxide layers

have resistances in the Giga Ohm range, meaning that the current will not flow through them when the devices resistances is just a couple of ohms.

The chosen layer was aluminium oxide (Al_2O_3), in which is often used in most cleanroom processes. The sputtering deposition of this material is made on Timaris FTM, and the process takes less than 30 min. In this machine, the wafers move below a big target of Al_2O_3 at 15 mm/s for a total of 140 passages. The deposition rate is around 0.1 nm/s, meaning that this machine can be tuned to get extremely precise thicknesses. The detailed recipe is shown in Appendix 3.a.

These thin layers have special optical properties, and depending on the film thickness, different colours can be observed. In Figure 5.4 a) and b) two different thicknesses present two different colours: for 100 nm, the thin film is more blueish, and for the 200 nm layer, the thin film is more yellow. The wafer presented in b) was also measured with the interferometer. In this machine, a piece of silicon must be measured as the reference and then the wafer with the oxide layer is mapped. In the mapping of the Al_2O_3 layer, the value is automatically extrapolated by the comparison between the measured value and the reference silicon wafer.

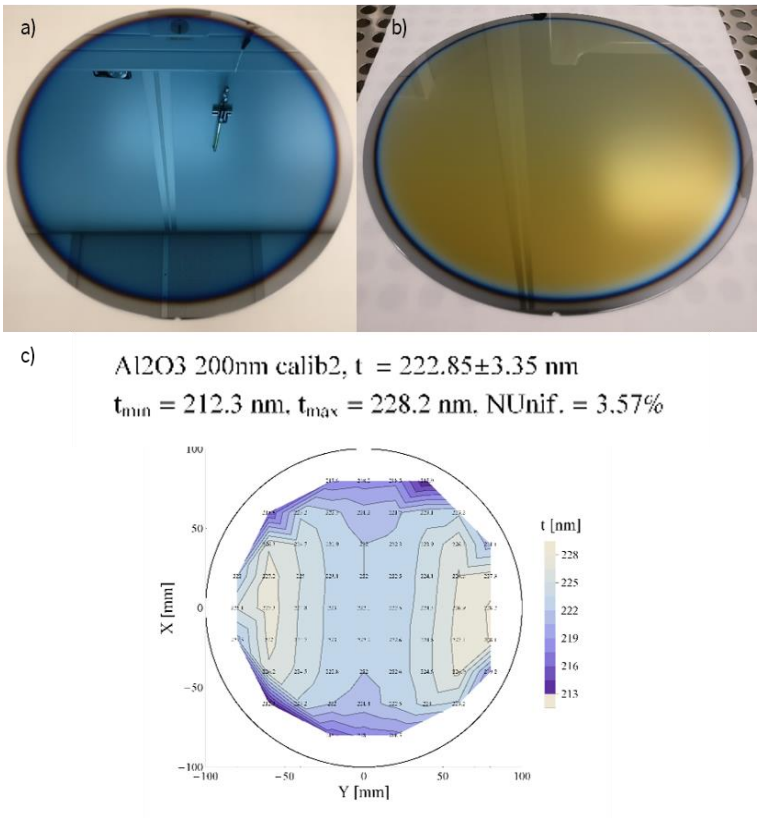


Figure 5.4. Al_2O_3Deposition; a) Silicon wafer with 100 nm of Al_2O_3; b) Silicon wafer with 223 nm of Al_2O_3; c) Interferometer measurement of the layer thickness.

Analysing the final measurement, the layer has 223 nm with an error of 3.6%. This error is not significant and it should not affect in any way the rest of the process. The wafer was calibrated to have at least 200 nm of thickness at all points.

5.2.3. Seed layer deposition

The wafer is now completely isolated from the top layers, meaning that every device that made on top of it will not suffer electric interferences from the substrate. The electrodepositions are the main processes in this fabrication procedure and, as explained before, the seed layer metal is absolutely necessary in order to grow thick metal layers. This seed layer should be a different material from the device itself. After depositing everything, this seed layer should be removed to avoid short circuits, and if all of the metals are the same, when etching the seed layer, the remaining structures would also be attacked. Since the devices will be made out of nickel, the chosen seed layer was copper. Copper is highly conductive and has a good adhesion for electrodeposited metals [96]. Since electrodeposition grows thick layers of metal, and these layers increase the stress of the thin films located below them, it is important to have a seed layer with a thickness in the order of hundreds of nanometres for increased durability. With some nanometres, the conductivity may be enough to electroplate metals, but when these metals get thick, the stress that they create can be high enough to peel the seed layer off the substrate. With that said, the copper seed layer will be 200 nm thick. In order to get the copper on top of the Al_2O_3 layer, an adhesion layer needs to be sputtered. Tantalum is the adhesion layer predefined in the INL. With a thickness of just some nanometres, the peeling effects disappear and the seed layer becomes strong enough to handle a big electroplated layer. Therefore, 10 nm of tantalum were sputtered immediately before sputtering the 200 nm of copper. The adhesion and the seed layers were deposited in the same sputtering process without taking the wafer out of the chamber. The 10 nm thick tantalum adhesion layer took 1min06s to sputter, with a deposition rate of 0.08 nm/s. The 200 nm thick copper has a similar deposition rate of 0.07 nm/s, the process took 47min. After the film depositions, the wafer was measured in the sheet resistance mapper, and results show that the uniformity is 5.14%, a really low value that is perfect for this process (Figure 5.5). The detailed recipes used in the machine are presented in Appendix 3.b.

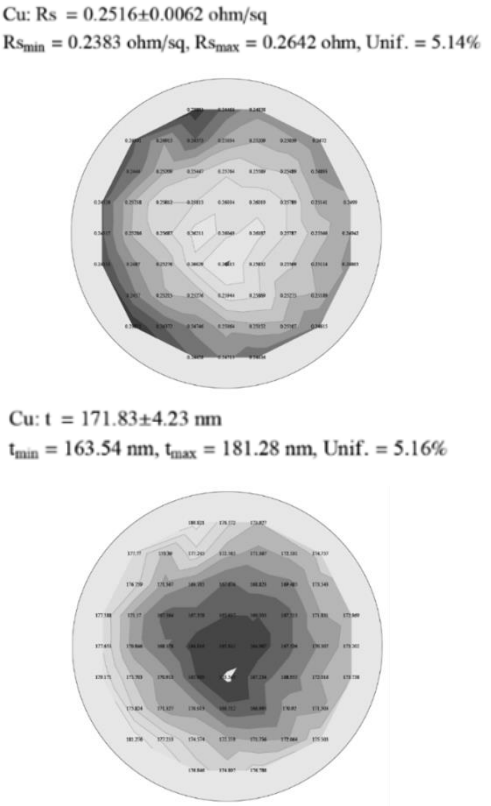


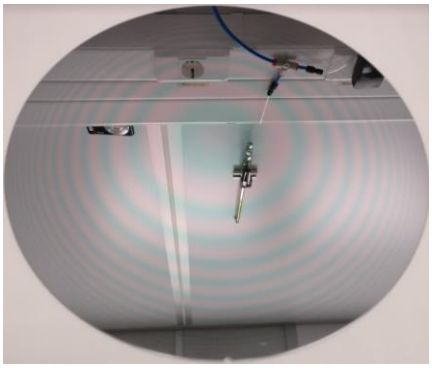
Figure 5.5. Top: sheet resistance measured in the full wafer; Bottom: thickness obtained based on the copper resistivity and the obtained sheet resistance.

The copper sputtered in Kenosystec at INL has a resistivity of 4.32x10^{-6} Ω.m. Using the resistivity and sheet resistance, the film thickness can be estimated using the equation 3.2. The thickness was targeted to be 200 nm, and the obtained value was 171 nm. This was not corrected with more sputtering because the copper quickly starts to oxidate, therefore proceeding with the process was more important than growing the remaining 30 nm of copper. The layer of copper is thinner at the centre of the wafer, but this is not problematic and it is mainly caused by the position of the sputtering target inside the chamber. The results are quite good so far and the process can continue on top of this seed layer.

5.2.4. Sacrificial layer deposition

The deposition of amorphous silicon is the step that follows. This layer was previously calibrated (3.3) because it was not used in the INL as a sacrificial layer. This time, the appearance of the wafer was a little different, and the a-Si didn't look uniform (Figure 5.6). Unfortunately, measuring the thickness with the interferometer became a complicated process. Before measuring

the a-Si, a map for the copper deposition was taken in the interferometer. Then, a stack of materials (in this case 200 nm of Cu and a-Si on top) was created, but for some reason the results were not satisfactory and the machine was not able to measure it precisely. It is important to notice that the interferometer is used to measure transparent or semi-opaque thin films, and the metal layers are highly reflective for this measurement. So, a dummy wafer with the same layers was processed to measure the thickness in the mechanical profilometer. Before depositing the a-Si a polyamide tape was placed on the centre of the wafer in order to create a profile from the top of the a-Si to the Cu on the end of the deposition. The results were quite satisfactory because in the centre the thickness of the a-Si was 466 nm (Figure 5.6). This value is only a thickness measurement without knowing the uniformity, but then again, measuring the uniformity of a-Si on top of copper with the available tools was not possible. So, the uniformity was assumed to be not far from the uniformity measured before in chapter 3.3. The detailed recipe is shown in Appendix 3.c.



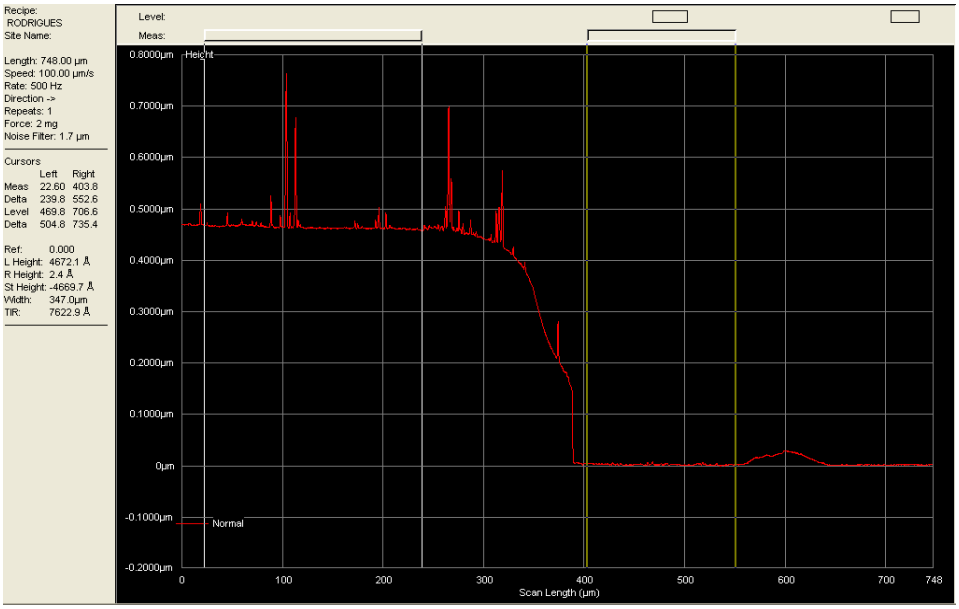


Figure 5.6. On Left: Amorphous silicon deposited in wafer; On Right: Profilometer measurement of the a-Si after removing the polyamide tape.

Patterning a-Si with the anchors will be the following process for the self-folding devices. This process will go through a lithography step and then DRIE.

5.2.5. First lithography

For the first lithography, the wafer was placed in the vapour prime oven at 150°C. The surface was activated with a chemical called HDMS, which turns the surface of the wafer hydrophobic, not allowing the connection of water molecules to the photoresist that will be coated.

The photoresist AZ9260 is used for patterning thick layers; in this case, it was spin coated at 3000 rpm to achieve a thickness of 8 µm. Since this patterning will be used not only to etch the a-Si but also as a mask layer when electrodepositing the anchors, the edge of the photoresist was removed in order to transfer the electrical contact to the border of the wafer. The wafer was exposed using the mask number 1 in the mask aligner. The exposure dose for this photoresist is 1763.2 $\mathrm{mJ/cm^2}$, and the intensity of the lamp was 39.4 $\mathrm{mW/cm^2}$. Since W=J/s, the time needed to expose this photoresist layer is 44.75 seconds. The exposure was made in contact mode, meaning that there is no gap between the wafer and the mask when the lamp is turned on. After the exposure the wafer went for the development. The wafer was developed with AZ400K for 240 seconds. In Figure 5.7, the final result of a patterned anchor is showed.

Figure 5.7. Left: Development of the photoresist (residues visible on the bottom layer); Right: Wafer after DESCUM process of 15 seconds.

The process parameters are described in Appendix 3.d. Since the photoresist is thick, the development is not perfect, so the wafer goes through a DESCUM clean where the photoresist is etched everywhere, removing all the residues that are on the copper layer.

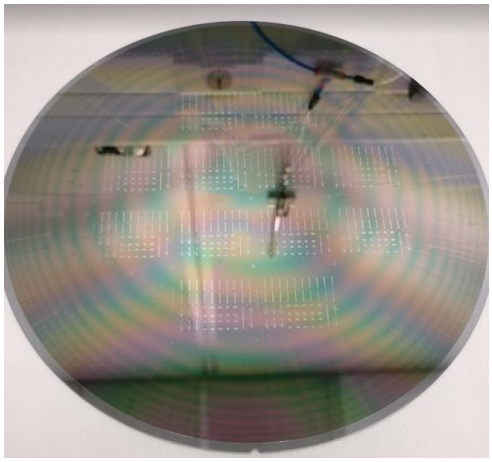


Figure 5.8. Wafer patterned with a photoresist of 8 μm.

With DRIE, the a-Si is open with a process that runs for 180 seconds, with the injection of two different gases, SF_6 and C_4F_8 in a vacuum chamber. The SF_6 attacks the Silicon isotropically, then with C_4F_8 the wafer is passivated on the etched walls, creating an etching cycle (Figure 5.9 b) and c)). In c) we have represented the first cycle, in d) the second cycle and in e) the third cycle. If these cycles are repeated, the process goes down without doing any lateral etching. In the end, an etching step is performed in order to remove the passivation layer (Figure 5.9 f)). The process recipe is shown in Appendix 3.e.

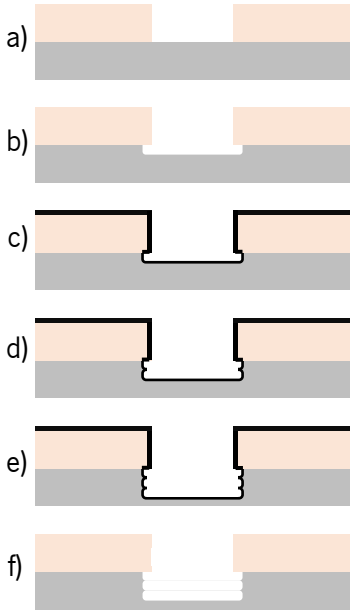


Figure 5.9. Anisotropic DRIE of Silicon a) Patterned substrate for the etching process; b) Etching step with SF_6 where the silicon is attacked; c) Passivation with C_4F_8 to protect the side walls; d) Second etching level - repetition of step b) and c); e) Third etching level – repetition of step b) and c); f) Passivation layer etching.

5.2.6. Electroplating

After the DRIE step, the copper remains exposed and is immediately transferred for the electrodeposition setup to avoid any contamination or oxidation of the metal layer. The electrodeposition process followed the setup calculations detailed in chapter 3.2. It is known that mask number one has an exposed area of 9.54 cm^2. Using a current density of 0.001 $\mathrm{A/cm}^2$ and the desired 500 nm of thickness, the calculation sheet gives values of 9.5 mA of current during 28 min, as shown in Figure 5.10.

Plating step details:

Exposed seed layer area, cm^2	9.54
Current density, A/cm^2 (2)	0.001
Estimated plating rate, um/h (3)	1.080152672
Target thickness, um (4)	0.5
Current, A	0.0095376
Plating time	1666 sec (28 min)
Corrective plating time, sec	0

Figure 5.10. Values used in the electrodeposition step.

The current density needs to be reduced in order for the metal to deposit slowly and uniformly. If the current density is too high, the nickel ions start depositing only in some places, resulting in a non-uniform layer. In Figure 5.11, the sample deposited at 0.001 $\mathrm{A/cm}^2$ is shown.

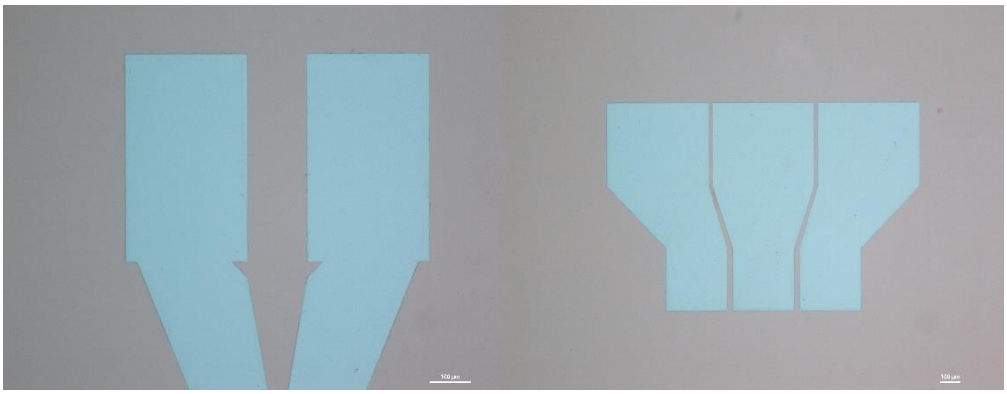


Figure 5.11. Wafer deposited with $0.001\ \mathrm{A/cm}^2$.

Table 5. Profilometer measurement of the first Ni deposition.

Site	Profilometer Measurement (µm)	Real Deposited Value (µm)
Centre	-0.02	0.48
Top	+0.02	0.52
Notch	+0.03	0.53
Left	-0.01	0.49
Right	-0.04	0.46

The sample was measured in the profilometer, and the measured value is the difference between the a-Si and the plated Ni. So, the value should be zero for a perfectly electroplated nickel with the desired dimensions. The resist is removed to be sure that it is not being considered in this measurement and that the needle of the profilometer will pass on top of the a-Si and the plated Ni. To remove it, the wafer is dipped in acetone for 10 min. Once the photoresist is completely dissolved, the wafer is cleaned with IPA and then rinsed with DI water. The measurements obtained are shown in Table 5, and the average thickness of the Ni anchors is 0.496 µm.

5.2.7. 3D devices patterning

The wafer is now ready for the deposition of the second seed layer. These new adhesion and seed layers were deposited exactly with the same parameters as previously reported. Since now the wafer has 5 different layers, it is impossible to measure the sheet resistance value of the copper, so the thickness is believed to be the same as last time. Now, the process continues like the one described in chapter 3.3, where the structures are aligned with the anchors. These structures will be deposited with two different electrodepositions, and in the end all the sacrificial layers will be removed.

The second lithography will use mask number 2 to define the plates of the small devices. For this lithography it was used a thicker photoresist layer. The chosen value was defined in order to be able to play a little bit with the electrodeposition of nickel. The desired thickness was 10 µm, but since this process was being tested, a photoresist layer of 40 µm was used. AZ9260 was used again, but the spin coating is done at 1000 rpm and is repeated twice, each time creating a 20 µm layer. The used parameters for exposure and development are the same that were used in chapter 3.3. The exposure step had a big difference, because it had to be aligned with mask number one. The process parameters are shown in Appendix 3.f. Finally, a DESCUM process was applied to clean the surface before electrodepositing nickel again (Figure 5.12, a), b) and c)). The

electrodeposition area is now different, so using the same spreadsheet the new values were calculated. The area is 3.99 cm^2, and to deposit 10 µm the current was kept at 40 mA for 56 min.

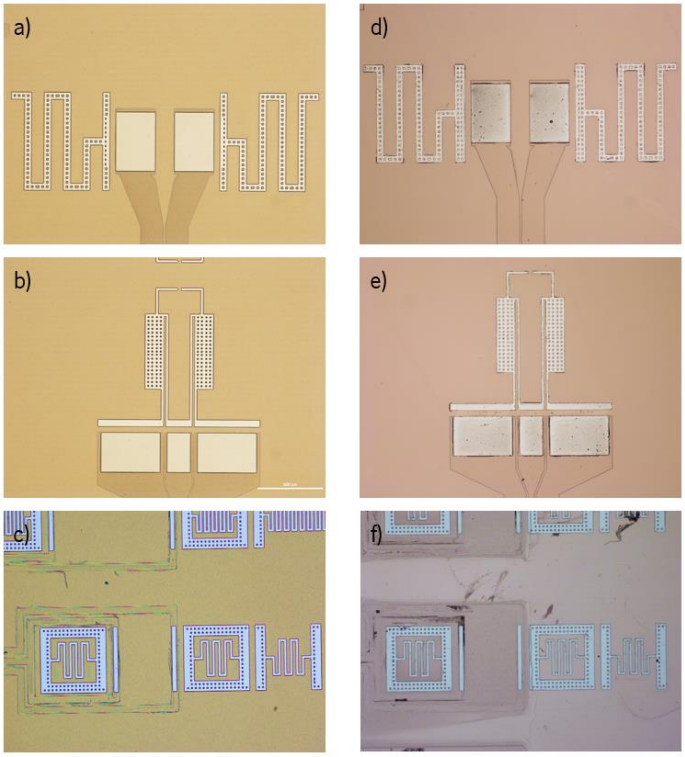


Figure 5.12. a), b) and c) are the photos of the lithography done with mask number 2; d), e) and f) are the photos after the electrodeposition.

Plating step details:

Exposed seed layer area, cm^2	3.99
Current density, A/cm^2 (2)	0.01
Estimated plating rate, um/h (3)	10.80152672
Target thickness, um (4)	10
Current, A	0.0398690
Plating time	3333 sec (56 min)
Corrective plating time, sec	0

Figure 5.13. Parameters used on the second electrodeposition

In Figure 5.12 d), e) and f), the electrodeposited plates are observed. Resorting to the mechanical profilometer, the obtained values are shown in Table 6. The values are really close to the desired value, giving an average value of 9.64 µm of thickness.

Table 6. Profilometer measurement of the second Ni deposition.

Site	Profilometer Measurement (µm)
Centre	9.45
Top	9.92
Notch	10.01
Left	9.54
Right	9.26

After removing the photoresist with acetone and IPA, the wafer looks a little bit dirty. This can be solved with a small DESCUM of 15 seconds. After inspection, it was possible to conclude that the plates were deposited and the alignment was really good, therefore the next lithography could be performed to deposit the Sn hinge layer. The hinges lithography will be done in the same level as the lithography for the plates; the photoresist will be the same, and the thickness is also 40 µm.

The results of hinge deposition are shown in Figure 5.14, where it is visible that the hinges were well aligned with the rest of the devices, and the small pillars of 15 by 15 µm were correctly exposed and developed. These structures were the most critical ones, because without these holes the undercut etch would not be performed. The second and third lithography recipes are described in detail in Appendix 3.f.

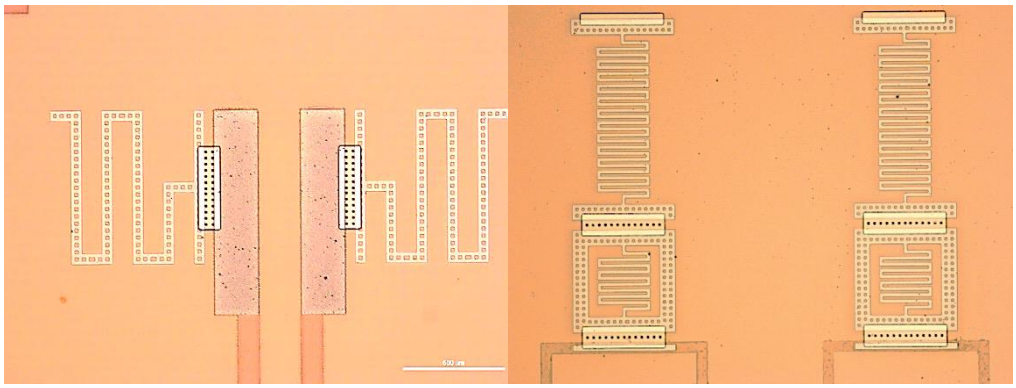


Figure 5.14. Lithography with mask 3: hinges of the self-folding devices.

5.2.8. Individualization and final deposition steps

After the final lithography, the electrodeposition was performed in a small beaker, meaning that the wafer needed to be diced in small dies that would fit in this setup for electrodeposition. The dicing was made through the dicing marks that were patterned on mask number 1. The cuts were

made in two directions (90° rotation), making perfect squares of 30 by 30 mm. The process runs at 5 mm/s for approximately 10 min. Each die will be processed separately with different Sn plating conditions. An opening for the electrical connection needs to be made, but this small square will not be dipped into the electroplating solution to not interfere with the plating area.

In Figure 5.15, the small square obtained from the wafer is shown. At the top, the big square with exposed copper can be seen. In this square, the alligator connector will be plugged to ensure a uniform current distribution in the die. The dies are now ready to electrodeposit Sn for the device's hinges. Each wafer has 12 usable dies, and this process was made with more than one wafer to test the Sn hinges. The Sn deposition should achieve thicknesses bigger than 20 µm. In chapter 3.2, the deposition rate of the Sn plating system was found to be six times less than what is described in the datasheet, therefore, to deposit 25 µm of Sn, it was used a current injection of 25 mA during 20 min. The result of this step is shown in Figure 5.16, and the measured value of tin thickness is between 20 and 25 µm.

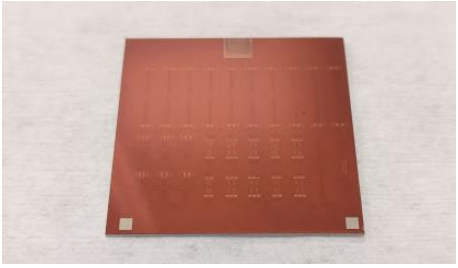


Figure 5.15. Die with the third lithography step done and ready for electrodeposition of Sn.

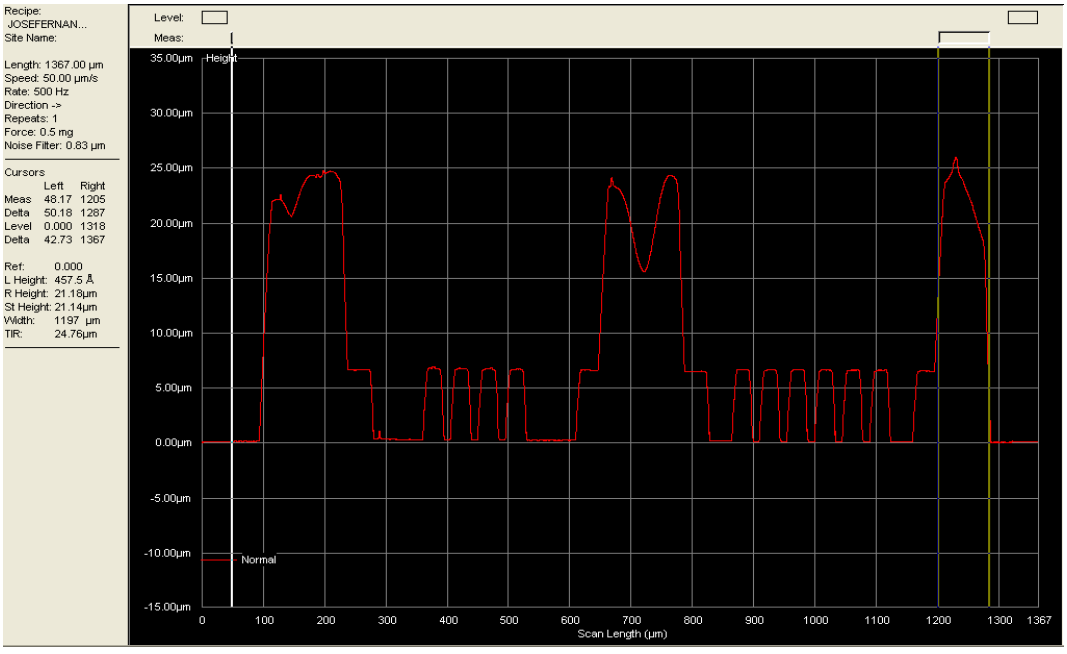


Figure 5.16. Profilometer measurement of Sn deposited on top of the Ni structures.

Regarding the hinges shape, they present a Y-shape, unlike the desired T-shape form which was expected by following the process described in 2.3. Even so, the hinge is electrodeposited in place, and in Figure 5.17, the three main devices are shown with the corresponding hinges in place.

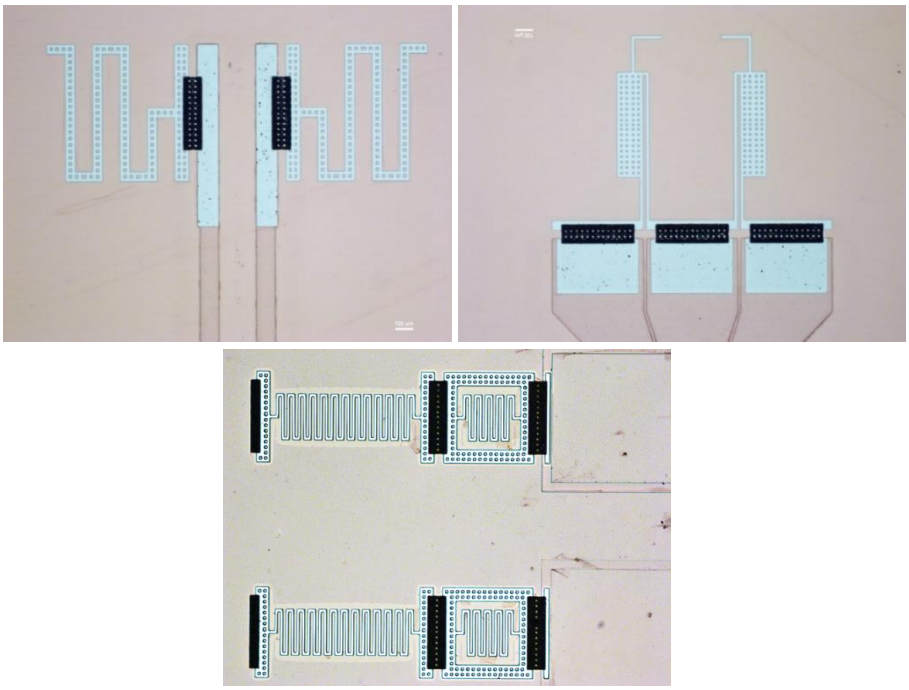


Figure 5.17. Deposition of 25 μm of Sn in the three different structures.

An SEM image of the two electrodeposited layers can be seen in Figure 5.18, where the hinge material can be observed on top of the nickel plates and the Cu layer. The hinge is a little bit rough, but the nickel plates have a nice uniformity; the three are well connected and the holes to remove the underneath layers can be seen in the middle of the hinge. In this case, the thickness of the Sn is between 20 and 30 μm.

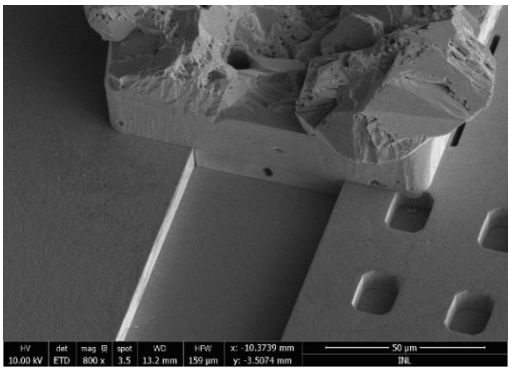


Figure 5.18. SEM image of the two electrodeposition layers for the Ni plates and the Sn hinges.

This was the last deposition step, and a full stack of different materials is now on top of the silicon wafer. Most of these layers are sacrificial and need be removed after this point of the process. The first etch to be done is the Cu seed layer.

To etch, copper Etchant 49-1 was used like in chapter 3.3. Since previous results show that the Cu layer was not completely removed in 150 seconds, this time the beaker was placed inside an ultrasonic bath at 40°C, to promote the moving of the etched residues and increase the undercut etch rate. After the etch, the obtained result is shown in Figure 5.19, where it is possible to see that the a-Si layer becomes visible after the wet chemical etch of the seed layer.

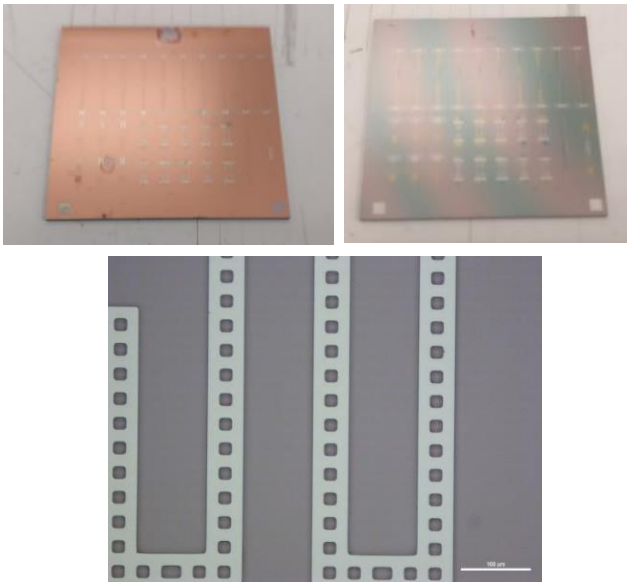


Figure 5.19. Top: Before and after the removal of the first seed layer with copper etching; Bottom: Nickel on top of a-Si, there are no visible residues of Cu in the small holes.

The Tantalum layer that worked as an adhesion layer and the a-Si will be removed on the Xactix equipment. As mentioned before, this isotropic etch will be performed with the injection of XeF_2 gas. This etching is performed in cycles of 30 seconds, to renew the etching gas. After some testing, it was found that to completely remove the sacrificial layer, 100 cycles of isotropic Si etching were needed. The sample regains the colour of Cu, revealing the other seed layer used for the deposition of the anchors. The sample undergoes the copper etching bath again at 40°C. Since that at this stage the structures are suspended in the sample, the ultrasounds were turned off, in order to not create a lot of mechanical forces in them. In the end, the sample goes again on the XeF_2 chamber to perform 5 cycles, in order to remove the last adhesion layer of Tantalum. In this way, the only layer between the devices and substrate is the isolation layer of Al_2O_3. The sample after removing all sacrificial layers is shown in Figure 5.20.

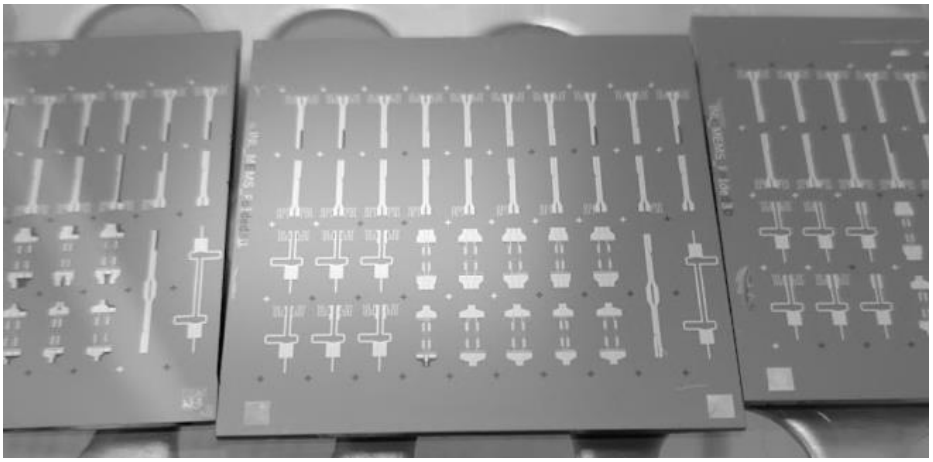


Figure 5.20. Sample ready for the folding process.

5.2.9. Self-Folding of microfabricated structures

The folding process was done as described in the previous chapter. The flow needs to be correctly followed, only in this way, the melting of the hinge will occur uniformly and promoting the correct folding of the structure. The process is the following:

1. Inside a Pyrex beaker, put 200 mL of Benzyl Ether, with approximately 5 mL of Liquid flux.
2. Place the full die inside the beaker.
3. Ramp the temperature up to 100°C and wait for 5 min. In this step the flux dissolves the oxide layers.
4. Ramp the temperature up to 200°C and wait another 5 min. In this process we are trying to get the highest temperature before folding uniformly distributed in the sample.
5. Ramp the temperature to 260°C until the structures visibly fold.
6. Cool the solution to room temperature.
7. Clean the sample with IPA to remove the organic compounds and carefully blow dry with nitrogen.

In Figure 5.21, three of the tests are shown. In a) the volume of the hinge is small (thickness of 10 µm approximately) and the Sn was separated when melted. In b) the hinge had approximately 25 µm and the samples were lifted when the folding occurred. In c) the deposition was so high that even the small holes for etching the underneath layers were covered, consequently when melting didn't create the surface tension forces needed to lift the device, it stayed on the surface of the wafer.

Figure 5.21. a) Deposition of 10 µm, left: before folding; right: after folding b) Deposition of approximately 25 µm left: before folding; right: after folding c) Deposition of more than 40 µm left: before folding; right: after folding.

Observing the structures, folding was the most critical point in the self-folding process. Unfortunately, this folding is highly dependent on the hinge format and volume, and sometimes the structures didn't fold at all. So, a limit of 10 min was fixed after reaching the 260°C. This high variability of folding was noticed right away where different volumes of Sn wouldn't lift the devices properly. After testing some samples, a complete hinge test was performed to understand how the hinge thickness affects the folding angle. For that, eight samples were tried out with different Sn

thicknesses, the angle of folding was analysed, and correlated with the respective deposited thickness.

To measure the folding angle, the samples were brought to a contact angle measurement machine. In this equipment, a lateral camera analyses the side view of the different samples and calculates the angle within three points. The measurement is not that precise, but can give an approximation of the final folding angle (Figure 5.22).

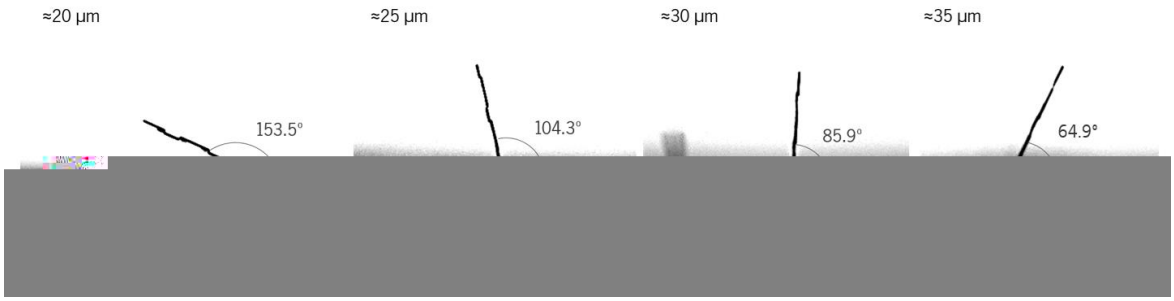


Figure 5.22. Folding angle measurement on a Contact angle measurement machine.

The graph shown in Figure 5.23 was obtained after analysing the eight dies, with different thicknesses. The interest area of folding only occurred in the samples with thicknesses between 20 and 35 µm. Outside of this range the hinges didn't fold and the structures do not lift. Another big problem that was noticed is that the non-uniformity of the Sn deposition was higher than expected and the hinges in the same sample sometimes presented different thicknesses, promoting different folding angles in the same die. This uncontrolled Sn deposition is quite common in the literature, and to get more reliable and controlled values, some electrolyte additives should be added [97]. What we can conclude from this graph is that, if the volume of tin in low, the forces are higher and therefore the structure is pushed to a higher angle. If this thickness is bigger, the folding angle starts decreasing because the Sn bubble promotes less forces, and therefore not pushing the structure so much.

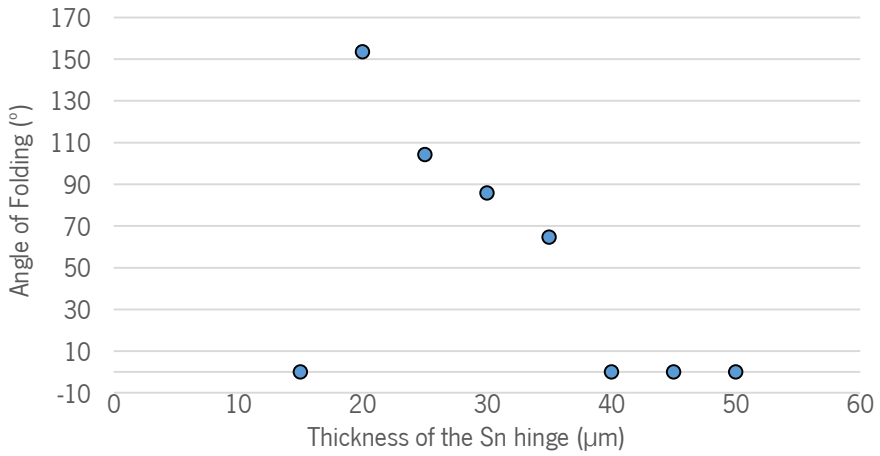


Figure 5.23. Relation between thickness of the hinge and angle of folding.

This non-uniformity of the Sn deposits gives origin to a plethora of different hinges that will not let the structures fold as expected. In Figure 5.24, all of the devices folded in different ways, which is related with the different Sn electrodeposits present on the hinges: in this image, we can identify the different folding angles.

Figure 5.24. Different Sn deposits in the same sample.

In the end, the folding can be controlled, but the Sn plating needs an improvement. The devices fold on top of a silicon substrate and are electrically connected, therefore ready to be tested. In Figure 5.25, the images of some folded structures on top of the silicon wafer are shown, where all of them are connected to the desired pads. In the scope of this work only the micro tweezer was simulated, so this will be the only device to be tested after the folding.

Figure 5.25. a) $60\ \mathrm{GHz}$ Antenna folded on top of a Silicon substrate; b) $36\ \mathrm{GHz}$ Antenna folded on top of a Silicon substrate; c) Thermal Actuator folded on top of a Silicon substrate.

Micro Tweezer functional measurements

The micro tweezer is easy to test and to verify if the simulation was correctly done

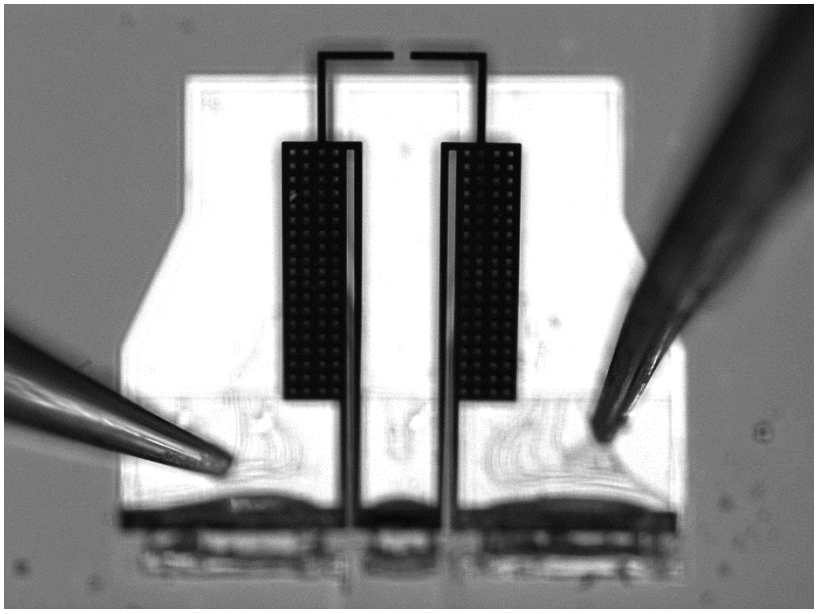


Figure 5.26. Electrical connection to the thermal actuator.

In principle, the connection is the same, except for the voltage values measured. In the simulation results the values of voltage are obtained for each device, and in the measurement setup the voltage will be related to the two devices. In Figure 5.27, the two schematics are shown. Since the thermal actuation comes from the joule effect and this value only depends on the injected current, in principle there is no difference on injecting 200 mA in each device or in both.

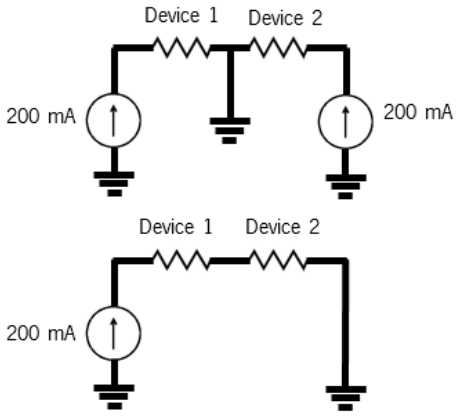


Figure 5.27. Top: Considered schematic for the simulation results; Bottom: Measured schematic.

After injecting a current through the probes, the device started moving as expected: the two devices moved in opposite directions, making the distance between them bigger when increasing the current. But after some tests, it became evident that the device had some limitations. It was

only possible to inject a current of 160 mA, after this value a deformation of the thin arm was noticed, changing its shape and its functionality.

As we can see in Figure 5.28, when the 160 mA are reached, the right arm starts getting darker, which is an effect probably related with the increase of temperature that leaves the arm in a different plane. The device was not destroyed and worked again, however the movement of the system was compromised. After this test, the device was used again to understand the physical limit of the thermal actuator. It worked well again until the 150 mA mark. After that, when injecting more current the left arm started deforming, similar to the right arm in the first experience. Then, the behaviour of the device stopped being linear and the device broke when the current reached 250 mA. This effect can be seen in Figure 5.29. The device in then in open circuit and unable to be used again.

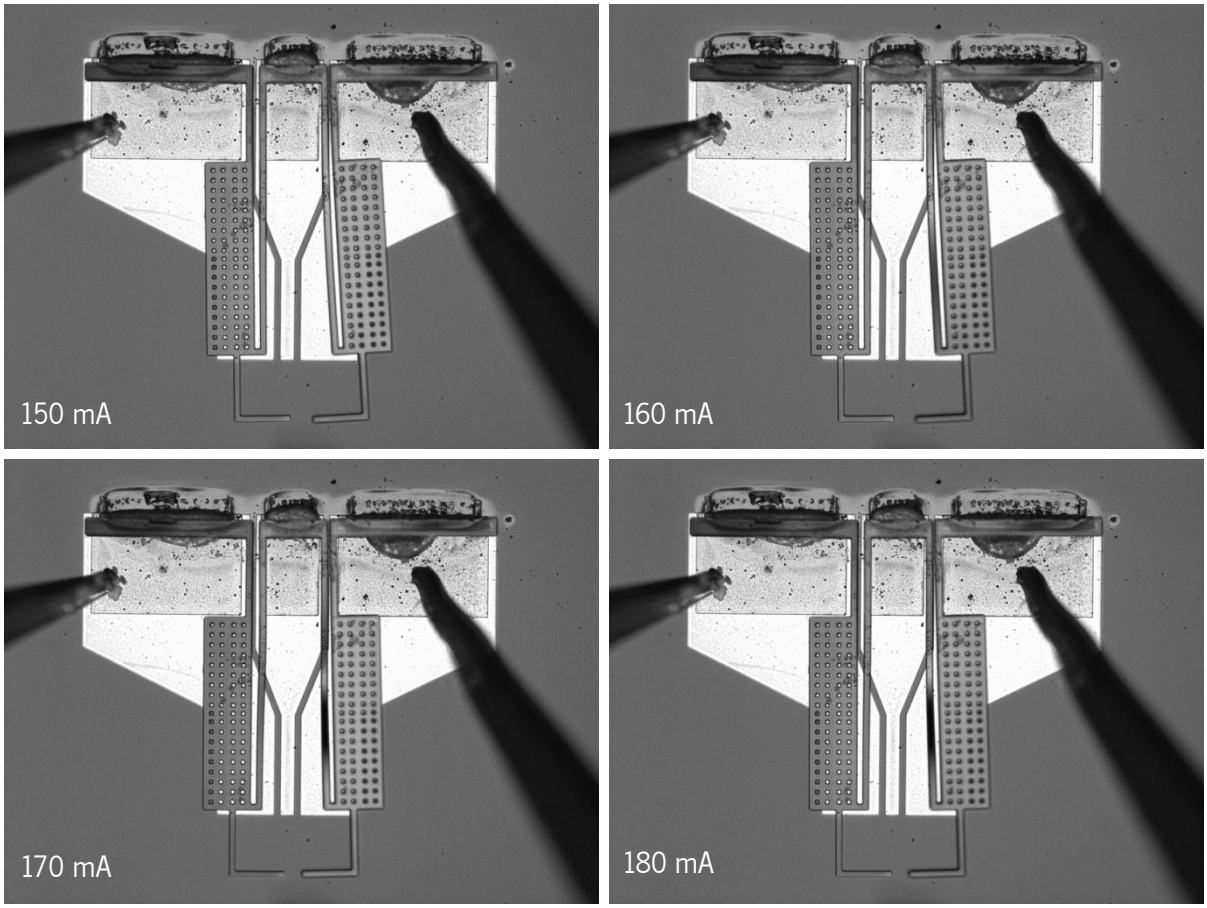


Figure 5.28. Injection of current in a thermally actuated device.

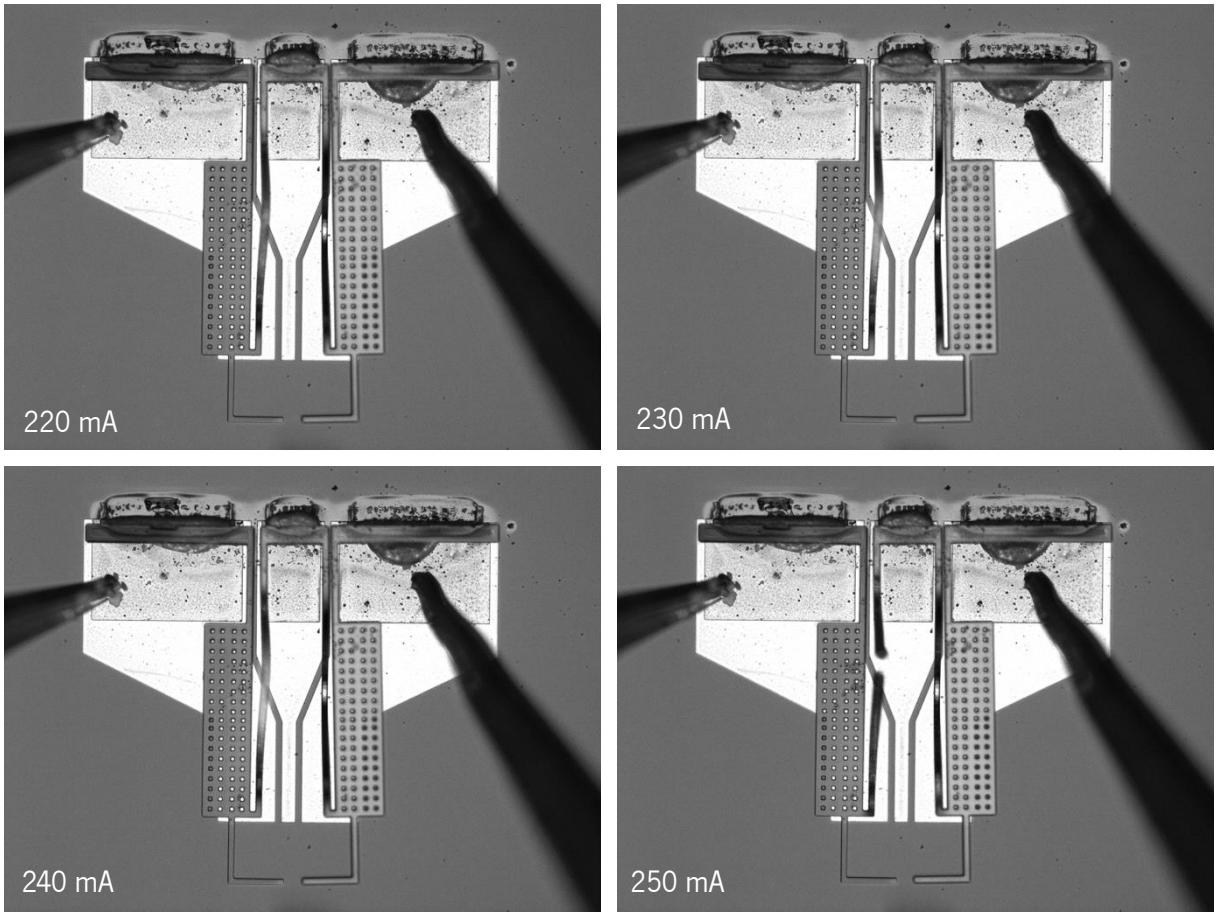


Figure 5.29. Device getting to the breaking point after injecting 250 mA.

5.3.1. Displacement analysis

Two new devices were used for the displacement analysis. Since the other device was destroyed during the first tests. In these new samples, the displacement was measured by taking photos in each resting position and when injecting the current. The values were measured with a dedicated software, by counting pixels with a predefined scale. In Figure 5.30, the displacement of the two thermal actuators when injecting different currents can be observed.

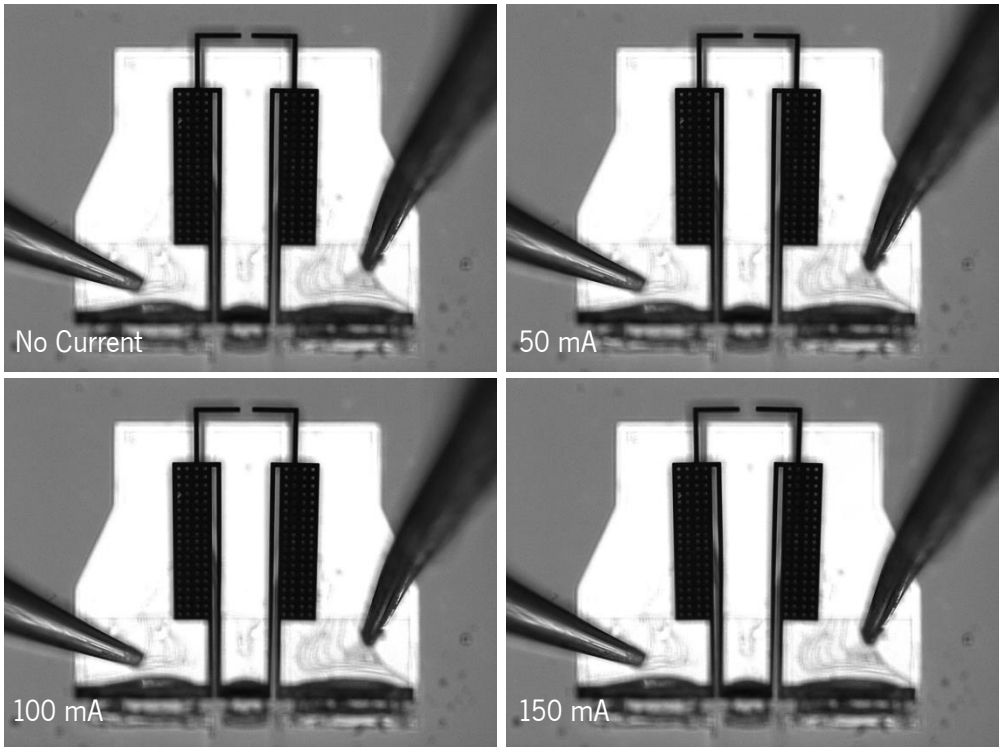


Figure 5.30. Displacement observed when the device is injected with 150 mA.

The current was only injected from 10 to 150 mA in order to avoid deformation of the thin arms. A comparison between the obtained displacement and the simulated values is shown in Figure 5.31.

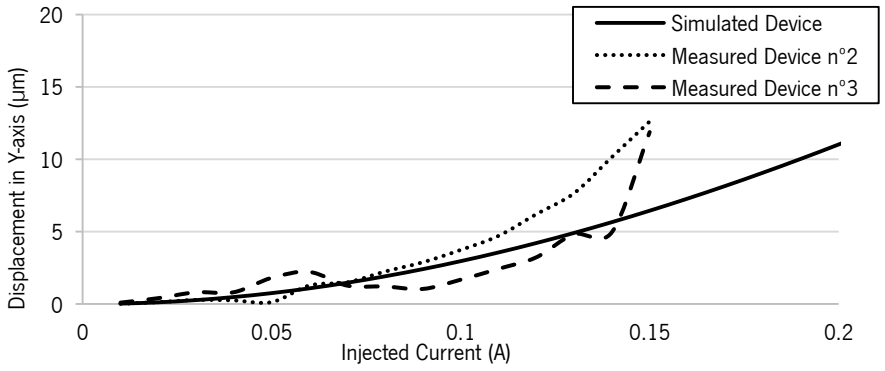


Figure 5.31. Simulated displacement compared with the measured devices n°2 (Dotted) and n°3 (Dashed).

The measured devices do not present a linear behaviour. In fact, when injecting the maximum current, the displacement is almost the double when comparing with the simulated device. This difference can be related with the composition of the real device, which will affect the final resistance of the whole system. In the simulation, when injecting 150 mA, the device had a displacement of 6.5 µm in each arm giving 13 µm of opening between the two arms of the tweezer.

On the end, the displacement was 12 μm when injecting the same current in each arm of the real device, giving 24 μm of opening in the two arms.

5.3.2. Resistance analysis

The displacement of the device was quite satisfactory when comparing with the simulated results, but it was noticed that the measured values were higher. This is probably directly related with a higher resistance of the full system that is generating more heat, and therefore, more displacement. So, in the same device, after injecting the current, the voltage was measured, and the graph in Figure 5.32 was obtained.

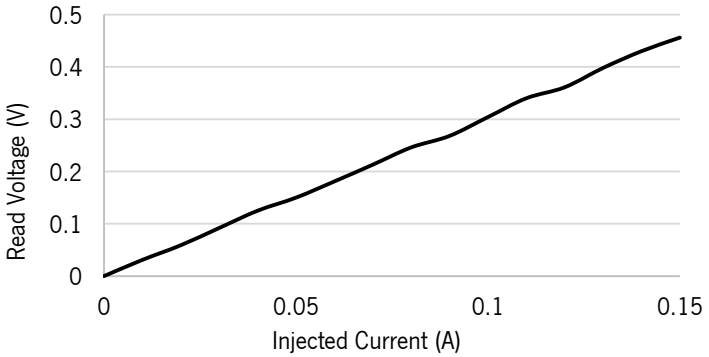


Figure 5.32. Read voltage when injecting current in the thermal actuator pads.

On average, the resistance value of the two devices is 3 Ω. Considering that the two devices are exactly the same, each device has a resistance of 1.5 Ω. Comparing with the simulated results in 4.1.2, the simulated device had a resistance of 0.95 Ω. This higher resistivity can be related with the design of the device that included small holes to get an easier fabrication process, with the composition of the full device and with the porosity of the electrodeposited Ni thin plates. This difference of resistance also explains the higher displacement of the measured device when compared with the simulated one. As explained in chapter 4.1, the generated heat is highly dependent on the resistance of the device, and since the measured resistance is higher, the displacement is also higher.

5.3.3. Temperature analysis

Temperature measurement was done with a thermal camera where a rough analysis was performed. The thermal camera had a limitation of 300°C of maximum read temperature, meaning that if the temperature went above this value the measurement would not be precise.

The device was placed in the camera and connected to the current source, where the current was injected with steps 10 mA like in the last measurements. Since that at INL there were no stress measurement tools, in this test the values of current were injected to understand if the generated heat was the cause for the device breakdown. Taking this into account, the values of current ranged from 0 to 250 mA.

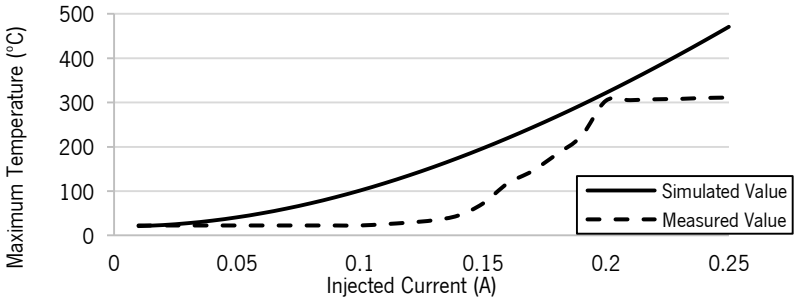


Figure 5.33. Comparison between simulated temperature and measured temperature when injecting current in the thermal actuator pads.

What we can conclude with this measurement is that after the 200 mA the 300°C were achieved and the thermal camera was not able to measure correctly. The values are a bit different from the simulated ones, and after achieving 250 mA an interesting phenomenon took place. The temperature started raising uncontrollably and suddenly the device cooled down and stopped the electrical conduction. With this result, it was possible to see that the breaking point of the device comes from a increasing of temperature in the thin arm: the material heats so much that the arm melts, leading to an open circuit.

Looking at Figure 5.34, the temperature, increased as expected mainly in the thin arm, where the expansion will occur. This expansion, as explained before, creates the desired movement of the thermal actuator. If this expansion is controlled and maintained in the elasticity range of the nickel, its effect on the device is reversible. If the maximum elasticity value is surpassed, the device will never return to the original shape, and will change is behaviour.

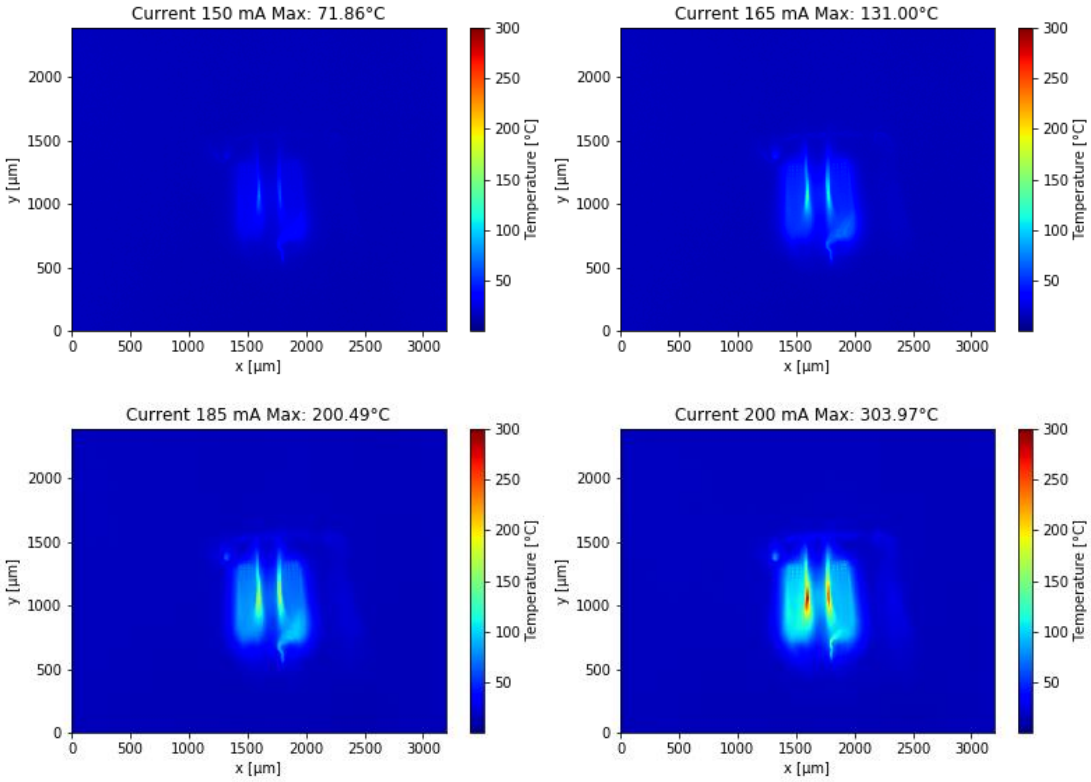


Figure 5.34. Maximum temperature measured in the device.

Chapter 6. Conclusion and future work

6.1. Conclusions

The world is demanding for complete sub-millimetre and micro devices in the next couple of years. The implantation of complete wireless microdevices in the human body will be a reality, and every human body system will be measured, controlled and medicated automatically by small machines that will not interfere with normal function of the organs. To achieve a future like this, integration is a key technological research field. The creation of complete wafer level packaged devices is a trend that will gain more followers in the upcoming years, and it is expected to generate billions of dollars worldwide. This work gave a contribution to the development of new packaging solutions.

Interaction of systems and the human brain is already a therapy and diagnostic tool used in many hospitals. Hundreds of untreatable diseases that afflict thousands of patients are still a complicated issue to deal with for biomedical researchers. Implantable microdevices can be a much needed solution for some of these problems. This thesis was in-line with a project that believes that a small integrated implantable microdevice for cooling brain cells can be a solution for some of those patients. The idea behind this project was to fabricate 3D microstructures and to allow them to be integrated with other microstructures, allowing the fabrication of highly miniaturized devices. Despite it being previously possible to fabricate such structures, there was no available and efficient way to integrate them with other chips and assuring a good electrical connection. So, a complex objective was proposed as the main topic for this thesis: translating an available 3D self-folding process to be used at our facilities, with our anchoring requirements.

One of the requirements of the implementation of this process at the INL was to build two functional research systems for electrodeposition of metals. This technology was not available inside the cleanroom so the first focus point of the project was to study and understand how an electrodeposition setup should work. The system was built in house and was adapted to use wafer holders from INL. The systems were implemented, but in the end, it was only used for Ni electrodeposition. For Sn deposition, a small setup was configured for this specific process. These

setups also became integrated systems of the cleanroom, and they can be used for other metal layers.

In the first runsheet, the main steps of a future complex process were calibrated. Thicknesses of thin films, etching rates and deposition rates in the different machines, and even new recipes were developed in order to be easier to process a wafer from the first to the last step. Even so, the process was in constant changing and tuning, because some incompatibilities or mishaps always appear when working on research based machines. On the end, the first small antennas were produced in an aqueous medium, validating the fabrication flow in INL's cleanroom.

Following what was done on the first process, the new process flow included an additional lithography followed by an electrodeposition step that would be patterned in the sacrificial layer. Before the fabrication, a small thermal actuator was simulated in order to use as a proof of concept for the final process. This actuator composed by Ni, was fully compatible with the standard self-folding technique, without creating new steps on the process. Other two simulations of small antennas produced in collaboration with co-workers were performed to have different devices in the same wafer. In the end, one device was simulated and produced: a micro tweezer based on a MEMS thermal actuator.

The final process began and, as expected, it didn't run from the beginning to the end in one single silicon wafer. Some tuning was needed, and some new layer incompatibilities and complications were found. The most significant problems appeared when electrodepositing Sn in the full stack of materials, promoting a deficient folding step. Nevertheless, the small structures folded on top of the silicon wafer, achieving the desired objective of this project. In addition to the final process, the simulated device was also electrically and thermally tested. This difference was inherent with the resistivity of the simulated material that was lower when compared with the real resistivity of the full device, which generated more heat and, therefore, more displacement.

In collaboration with the INL and their facilities, a novel process for a 3D monolithic wafer level packaging of these small structures was developed. The main objective was accomplished and the devices were correctly attached to a substrate allowing their electrical measurements. In order to achieve such results, the process went through dozens of iterations, calibrations and implementations that took some time, involved a lot of research, knowledge and the usage of complex tools. The originality of this work is translated in its main contribution, a complex process to integrate three-dimensional structures on top of silicon substrates. Placing MEMS on different

planes and integrating complex 3D structures on-chip, projected a lot of different new applications at INL cleanroom.

6.2. Future work

This project was a successful experience and the three dimensional structures were fabricated on top of a substrate. With the 8-inch wafers, the process is close to the big CMOS foundries that manufacture microdevices and CMOS circuitry in 12 inch wafers. The next big step would be to implement the process on top of a CMOS wafer, integrating the 3D MEMS structure directly with a designed ASIC. Therefore, the future for this project will be the self-integration of the two chips in the same process, meaning that the self-folding structure should be fabricated directly on a device wafer, and in the end, fold on top of it.

6.2.1. Process fine tuning

Before getting to the next step, some process issues must be considered, and this integration should be held until the process is completely under control. The process was not flawless, and some steps need a better calibration: the Sn electrodeposition and the self-folding step may be further improved. In the full process developed at the INL, the electrodeposition of Sn was hard to calibrate, mainly because of the poorly elaborated beaker setup and the adhesion with the substrate. Creating a Sn thin film by electrodeposition is not trivial and controlling the process is a really complex task [97]. Even after getting a setup that deposits Sn in every place, the thickness uniformity was not satisfactory and that significantly affected the self-folding step. Also, this deposition should be done in full 8-inch wafers, and that was also not possible in this project. The achieved results were enough to test some samples, but for mass production they were not enough. This step of electrodeposition should be implemented in a system where the thickness and uniformity are rigorously controlled in 8-inch wafers.

The self-folding step was made in a beaker and, in future iterations, this process should run in the full substrate, therefore the final step of folding should also be implemented for 8-inch wafers. In this case, the wafer should be dipped in the big heated tank, and if the Sn electrodeposition is well calibrated, all of the devices should fold at the same time. In conclusion, a new system for folding devices should be developed.

New applications can also be considered to self-integrate different MEMS and create novel microdevices. With such technique, the new devices can be endless and new ideas can be brought to life, creating a whole new group of out-of-plane MEMS. New functionalities and applications can be dreamt of, but most importantly, bringing already integrated MEMS closer to final production and packaging is the most significant contribution of this work.

6.2.2. Innovative three-dimensional routing

Three dimensional routing can be a great advantage of self-integration process and a future work for this process. With the advances in technology and microsystems, the connection between devices becomes often complex and sometimes impossible. Some devices have thicknesses of dozens of micrometres while others with some millimetres, meaning that their level is quite different when integrating them together. In other cases, on the same device, connecting the bottom to the top is not always easy, as going through the full device can be a difficult solution to implement or sometimes even impossible. Wire-bonding techniques or flip-chip technologies are not always the solution and, in some cases, a new technology could be the solution for this problem.

To show how self-folding can be helpful in such a situation, the following scheme will present a 2.5D integration of different devices.

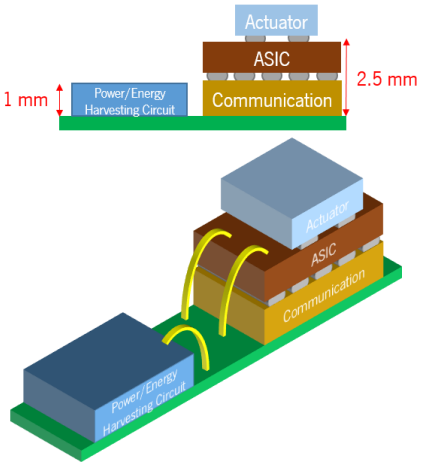


Figure 6.1. 2D and 3D image of a Complex microdevice where normal interconnection technologies are not feasible.

In this case, one of the two devices is really high, meaning that probably doing a wire bonding will be a complicated task. In Figure 6.1, a 3D view of the device with the wires from wire

bonding can be seen. This kind of concept is generally shown in many works, but such connections are generally really hard to perform, mainly because the wires are not able to reach such big heights.

This complex problem could be easily solved with a solution based on integrated self-folding: creating metallic structures that can interconnect the bottom with the top of the chip. In Figure 6.2, this idea is shown. In the substrate where the different devices will be interconnected, the self-folding structures are patterned. Then, after triggering the folding, these routes will lift and connect the different devices in different levels. This good example of future work can bring great advantages in the packaging technology.

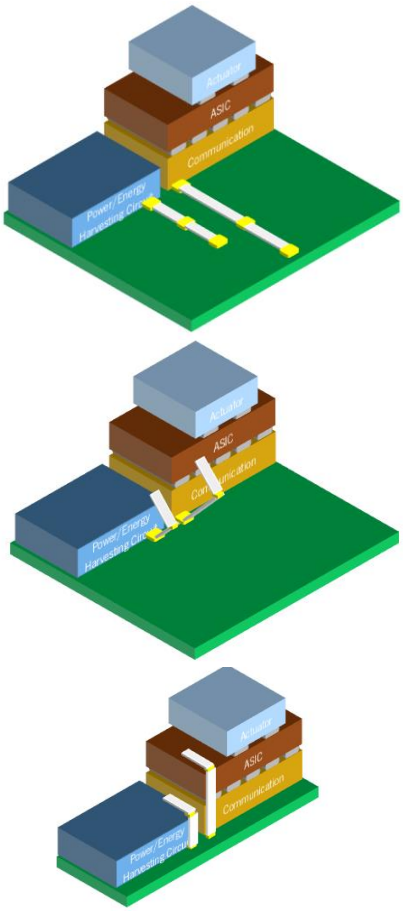


Figure 6.2. Self-folding technique to create 3D routing between different device levels.

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Appendix

Appendix 1. Fabrication Technologies

In this appendix, an overview of the systems that INL provides to do microfabrication is shown. It is important to notice that not every system is described, but only the ones used in this project. The functionality and usage of each system is described as well as the physical processes that occur in each one of them.

a. Sputtering Deposition

For the deposition of thin films in microfabrication, the sputtering technique is well implemented and one of the most used in the last decades, this technique is a PVD (physical vapour deposition) procedure where the particles are transported from a target to the substrate [94].

Inside a chamber a substrate is placed on the opposite site of a target, (a target is the source of the material that will be deposited on the substrate) on a vacuum chamber. After getting to pressures between 10^{-6} and 10^{-10} Torr, a continuous flow of an inert gas, typically Argon, is injected in the chamber, increasing this pressure to values of 1 to 100 mTorr. Inside the chamber, a spark is ignited and an Ar plasma is generated. A negative potential is applied to the target, and the Ar ions (formed in the plasma) are accelerated towards it. The Ar ions collide against the target, transferring its kinetic energy, and sputtering the target material. The target is eroded and the released atoms fly ballistically towards the electrically grounded substrate, depositing a thin film on its surface (Figure A.). A magnetic field acts as an impurity shield around the target, deflecting the charged ions, preventing their deposition on the substrate [94], [98].

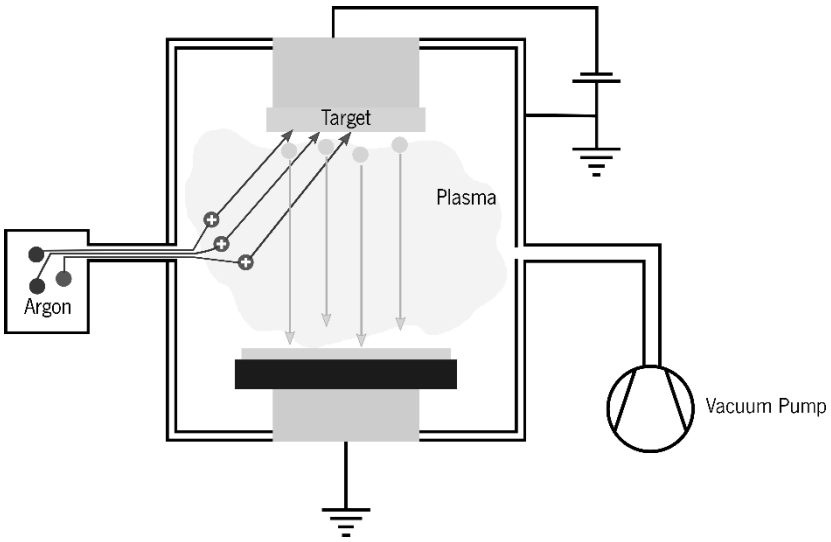

Figure A.1. Sputtering working principle.

Sputtering allows the deposition of conductive and non-conductive materials being useful to deposit metal layers and passivation's layers consequently without, for example, taking the substrates out of vacuum. At INL different systems of sputtering are daily used in several applications. In this project two systems will be used to deposit two different layers.

FTM from Timaris® is a physical vapor deposition tool designed for deposition of high-quality thin films. The tools handles four targets (four different materials), can process twenty five 8-inch wafers, but only one at a time. In the main chamber 3 targets are permanently installed, Aluminium alloy (AlSiCu), Titanium Tungsten (TiW), and Aluminium Oxide ($\mathrm{Al_2O_3}$), and a soft etch chamber that can be used to pre etch the sample to get better adhesion on the sputtering process. The uniformity of the thin films can go as lower as 5% and it is possible to achieve thicknesses that can vary from a few to hundreds of nanometres.

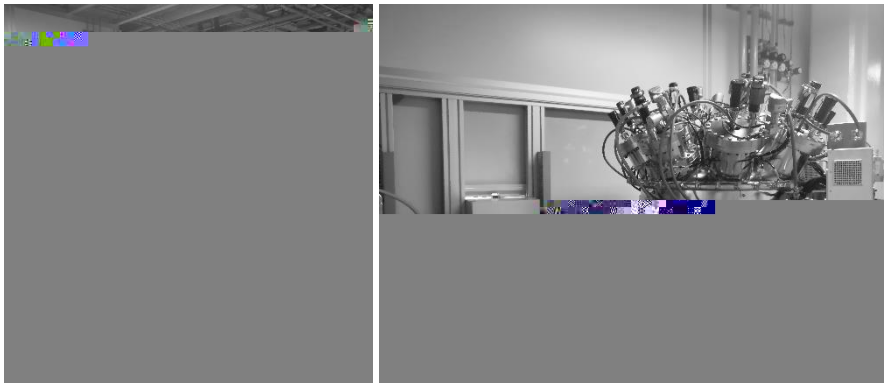

Figure A.2. FTM (left) and Kenosystec (right) sputtering systems.

Kenosystec is the other system that was used on this project. In contrast with the FTM, Kenosystec is a more experimental machine, it allows eleven targets for normal sputtering depositions and is able to do co-sputtering, i.e., sputter different materials at the same type allowing the deposition of experimental alloys. It can handle wafers from 2 to 8-inches, but is less optimized when compared with FTM. The system has DC and RF sources to allow the deposition of metals and non-conductive materials like passivation layers. Normally the targets inside the chamber are the following: Aluminium (Al), Tantalum (Ta), Chromium (Cr), Titanium (Ti), Palladium (Pd), Iron (Fe), Molybdenum (Mo), Magnesium (Mg), Nickel (Ni), Copper (Cu) and Gold (Au), but they can be changed for different materials like Nickel Oxide (NiO), Zinc Sulphide (ZnS), Silicon Oxide ($\mathrm{SiO_2}$) and others. Since this system is experimental, and most of the times the processes are changing, the uniformities are not as good as the other machine, but uniformities below 10% are always achievable.

b. Chemical Vapour Deposition

Like PVD, CVD (Chemical Vapour Deposition) is a technique to deposit thin films on top of substrates. It is used to deposit passivation (non-conductive) layers and widely used in the semiconductor industry having an important role in the transistor miniaturization [94].

Figure A.3. CVD working principle.

The principle is simple, two gases are injected into a vacuum chamber, when together, they react and deposit a thin layer of a new material on top of a heated substrate. After injecting the gases, at given pressure and temperature the reactants are absorbed on the heated substrate surface. The by-products, which appear after the reaction, are removed from the chamber and separated. Due to the toxic nature of the chemicals, these systems need a good filtration and separation of the reaction products, being this a disadvantage when compared with a PVD process.

Uniformities are directly related with temperatures, pressures, gas flows and by-products removal. Creating a thin film by CVD is not only achieved by injecting gases, so additional energy sources are used to achieve better results in industrial machines. Depending on this additional energy source, different kinds of CVD's are used nowadays. Plasma-enhanced chemical vapour deposition (PECVD), photon-assisted CVD and Laser-assisted CVD (LCVD) are three kinds of CVD's with different energy sources. PECVD is the one available in the cleanroom and one of the most used techniques. This deposition technique uses a radio frequency signal to generate a plasma inside the chamber allowing the process to run at lower temperatures, and achieve more stable and uniform thin films [94], [99].

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2 \qquad 6.15$$

$$SiH_4 \rightarrow Si + 2H_2 \qquad 6.16$$

Some of the most common applications for PECVD at INL, are the deposition of amorphous silicon and the deposition of silicon dioxide. In the $\mathrm{SiO_2}$ deposition, there is a reaction between the silane ($\mathrm{SiH_4}$) and the oxygen when a high temperature is achieved. On the Silicon deposition, the high temperature is enough to dissociate the silane molecule, depositing only Si on top of the substrate.

Figure A.4. SPTS CVD system.

At INL, dielectric layers and amorphous silicon is deposited on a SPTS PECVD machine. In the machine the following thin films can be deposited from a few nanometers to some microns thick, $\mathrm{SiO_2}$, Si_3N_4 and a-Si (amorphous silicon). With the help of a plasma, this layers can be

deposited with high and low frequency generators, and at low (150°C) and high temperatures 300°C) depending on the process. On the end the thin layers are deposited with great uniformity (bellow 10%) in full 8-inch wafers.

c. Optical Lithography

An Optical lithography step is a process of patterning structures with the use of a photosensible resin. This process allows the possibility of transfer a 2D pattern from a computer design to a thin film and therefore transform a uniform thin film in complex structures. The lithography process is divided in four main steps: Wafer priming; Coating of the photosensible resin (photoresist); Exposure with the desired mask; Development to remove the residues of photoresist [95], [98].

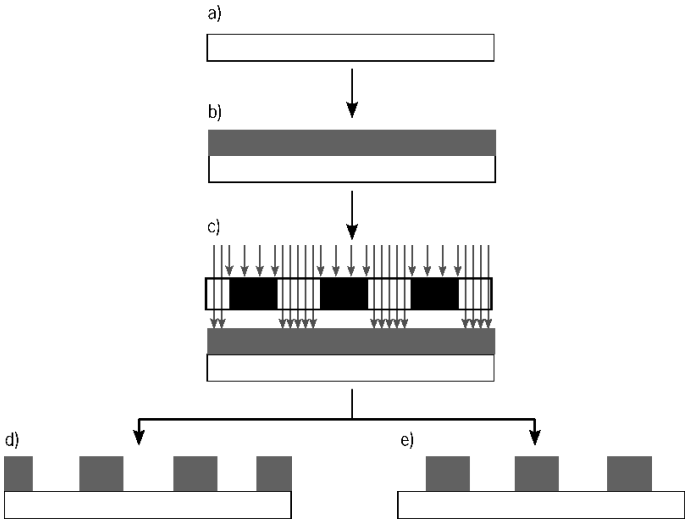

Figure A.5. Lithography process; a) Substrate preparation with Vapour Prime; b) Spin coating of photoresist; c) Exposure of the photoresist; d) Development of negative photoresist; e) development of positive photoresist (adapted from [95]).

There are two types of photoresists used, and their major difference is what happens after the exposure. In the exposure, a UV light is focused on the surface of the photoresist, this changes the structure of the material polymerizing it, than in the development step this material can be removed or stays solid on the substrate, depending on the type of photoresist that is being used. So with the same mask is possible to transfer the design of the counter mask (negative photoresist) or the mask itself (positive photoresist) to the substrate depending on the photoresist used on the coating step [94], [98]. After the lithography process, the photoresist can be used for addictive or subtractive steps, for example for lift-off process. A lift-off process (Figure A.6) consists in depositing

a desired layer on top of the patterned photoresist, then with a remover chemical, the photoresist is ripped off from the substrate, keeping the layer on the substrate patterned [95].

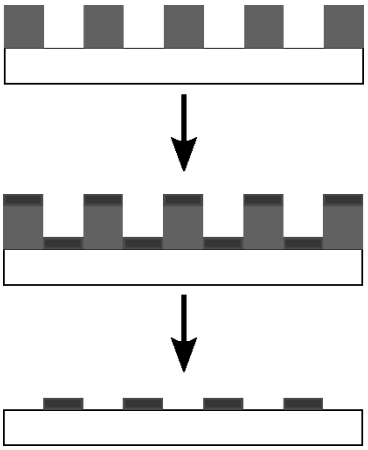

Figure A.6. Lift-Off process.

The four major steps of a lithography process will be described in the next separated chapters (adapted from [95]).

Wafer priming

Even being inside a cleanroom, before any coating of photoresist, the surface has to be activated, to promote the adhesion and clean the surface, since normal photoresists do not adhere well to silicon wafers. Generally, the native oxide present in the silicon wafers creates bonds with water molecules reacting with air. When the resist is poured on the surface, it adheres to this water molecules rather than the silicon surface [94].

Figure A.7. Vapour prime system.

In INL, a vapour prime oven is used for this purpose. In it, the chamber is in vacuum and a chemical called hexamethyldisilazane (HMDS) is injected to his atmosphere. Inside, temperature is risen to 130°C, and a full cassette of 25 wafers can be placed inside. With the reaction between the surface and the HMDS, the surface becomes more hydrophobic promoting the adhesion to photoresists. After this process the wafers are ready to coat photoresists [94], [95].

Spin coating and soft-bake

Spin coating is a really common technique to deposit thin films of photoresist, the process starts with placing the substrate on a spinning plate. Then the liquid photoresist is poured on top of the substrate (Figure A.8 – a)), this pouring step can be done in two different ways, with the substrate already rotating, or in a static position. The second step is the spread step, where the plate starts spinning at a low speed (Figure A.8 – b)) and the photoresist starts spreading all over the substrate.

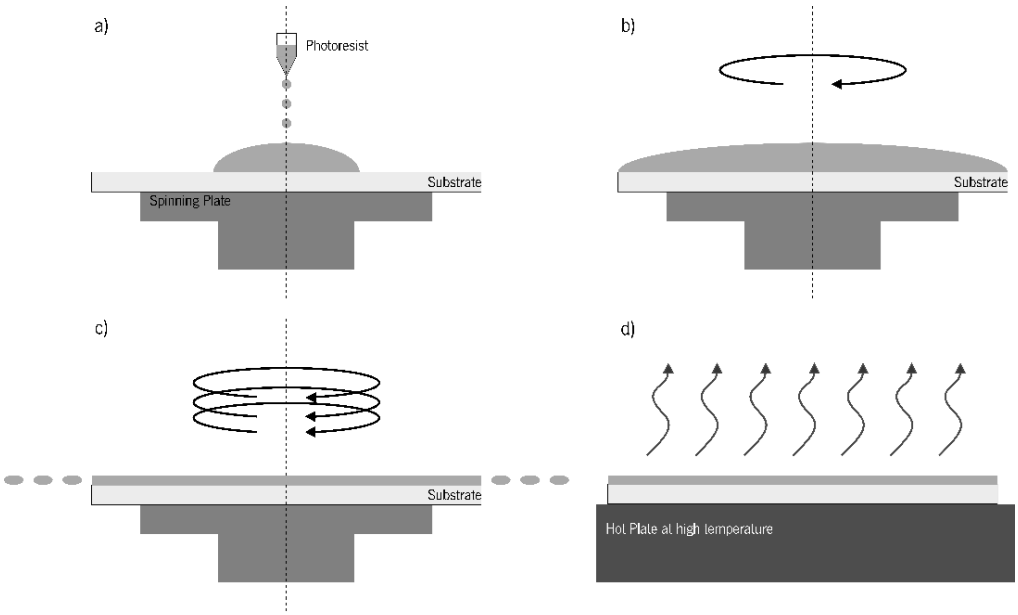

Figure A.8. Spin coating process.

Then the spinning plate go to the desired speed and the thickness of the photoresist is reduced to a desired value (Figure A.8 – c)). The parameters to get certain thickness are inherent to the photoresist itself, commercial available photoresists have their curve rpm vs thickness well defined. After spinning at the desired velocity for some seconds, the plate stops and the substrate goes to a soft bake, at a given temperature, evaporating the solvent and keeping the photoresist solid and stable with great uniformity (Figure A.8 – d)). Spin coating can deposit thin films from a

few nanometres to hundreds of microns of thickness. The major problems related with this process are the bubbles that get trapped on the photoresist layer and the “comets” that appear if any big particle is present on the substrate, this bubbles and comets can compromise the full lithography process [94], [95].

Figure A.9. SUSS Gamma Cluster.

At INL, this process is done in a SUSS® Gamma Cluster. This machine is able to run 25 wafers (8-inch diameter) in a batch. The system has a robot to grab the wafers and move them from the cassette to the spin coater, where a dispenser arm can deposit different photoresists. Then to the hot plate, where the soft-bake is performed, and finally return the wafers to their original position in the cassette. This automatic movement avoids any contact of the user with the wafer preventing the user from touching in the liquid resist before the soft-bake. The machine has also cleaning methods, with the use of EBR, to remove photoresist, clean the backside of the wafer or just remove the edge that is less uniform than the rest on the thin film.

Optical Exposure

The exposure step on the lithography process is the step where the pattern in transferred from a CAD design to a photoresist. There are two major options for the optical exposure used nowadays, the direct writing laser and the mask aligner exposure.

The mask aligner exposure is one of the most used in the industry, as the name implies, in this process a mask is required. These masks typically, one per layer that will be exposed, are made in quartz with a thin film of chromium, being the quartz the transparent material and the chromium

the opaque material to UV. The mask is placed on top of the substrate and a UV light source is focused on top of both. With a mask aligner normally it is possible to align different layers with the help of alignment marks (Figure A.10), using dedicated microscopes. The masks are moved to the correct alignment position, giving the possibility of patterning different layers on top of each other's. There are three types of exposures, the contact exposure, where the mask touches the substrate, the proximity exposure, where the mask and the substrate have a gap in between them, and the projection exposure where a lens is placed between the mask and the substrate to achieve smaller patterned structures [94], [95].

Figure A.10. Typical alignment mark used at INL.

The direct writing laser is a method where a physical mask is not required. A powerful laser with a wavelength in the UV band draws the design directly on the photoresist. Since it has to go through all the structures this process is slow, but can achieve smaller features when compared with the mask aligner process. This process can also do alignment between masks with the help of microscopes and computer software. The big advantage of these systems is the maskless process. Anytime during the process, the mask can be changed without costs, the same does not happen in the mask aligner process, where a mask needs to be fabricated all over again if something is changed on the design [94].

Figure A.11. Mask Aligner and DWL systems in INL cleanroom.

Typically, the DWL system is used to make masks for the mask aligner at INL. Exposing a full 8-inch wafer on DWL takes long times, so exposing a definitive mask and then use this mask to expose several wafers on the mask aligner is a common process. The system available at INL, a DWL2000 from Heidelberg has two different wavelengths: $405\ \mathrm{nm}$ and $375\ \mathrm{nm}$ for different photoresists. It can write in different materials like masks and silicon wafers, but its maximum speed is 105 square millimetres per minute, an 8-inch wafer has 31415 square millimetres, it will take a minimum of $5\ \mathrm{hours}$ to expose a full wafer. The minimum structure size is 600 nm but and as it was explained before it is useful for one-time experiences or mask fabrication. The mask aligner in INL is from SUSS®, has a low resolution when compared with the DWL, being the minimum feature 1 μm. It includes proximity exposure and contact exposure and can process dies and wafers from 1 to 8-inch. It has the capability of do front and back side alignment, meaning that the two sides of the wafer can be patterned in this system, making complex aligned 3D devices on wafers easily.

Development

Development is the dissolution of the unpolymerized photoresist, revealing on the end the transferred pattern from the exposure step. The development process can be done by a wet process where a liquid chemical dissolves the unpolymerized photoresist, and a dry process where a gas chemical removes the same material. The most used process is the wet chemical bath, where the substrate with the photoresist is dipped or rinsed with the remover chemical for a known time, then the substrate is rinsed with water and the lithography step is concluded. This time where the sample

is in contact with the developing chemical is critical, because with underdevelopment (less time than required) the unpolymerized photoresist will not be removed, and with overdevelopment, the walls of the photoresist that are polymerized start to be attacked by the chemical changing the desired shape of the structures. In high ratio (thickness-structure size) resists, the development is critical and a post processing step, called DESCUM is performed, this process cleans any undesired photoresist residues present after the development step. This DESCUM is based on cleaning the substrate with an oxygen plasma [94], [95].

d. Chemical Etch

In contrast with deposition techniques, etching is a subtracting technique used to build complex structures in microfabrication. There are two main etching techniques used in cleanroom fabrication process, dry etching and wet etching, and the major difference between them is the physical state of the etching material, gaseous state or liquid state.

Dry etching is more controlled and can be divided in two types, isotropic etching and anisotropic etching. Anisotropic etching in the gaseous medium is done on Deep Reactive ion etching (DRIE) machines, this machines work in vacuum and with a controlled injection of etching gases. Isotropic etching since can be done also in RIE machines but there are specialized machines with complex gases that selectively etch the desired materials.

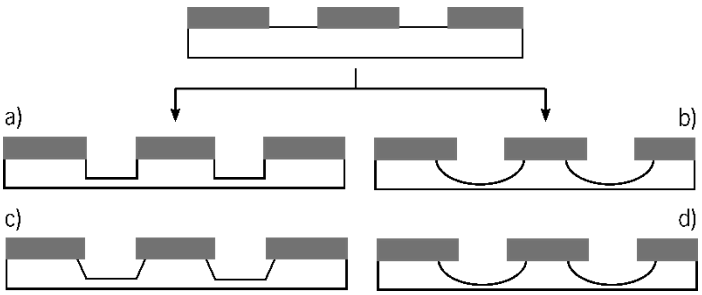

Figure A.12. Etching techniques: a) Anisotropic dry etching; b) Isotropic dry etching; c) Anisotropic wet etching; d) Isotropic wet etching.

Chemical wet etching is also really common in micromachining, generally used to remove layers completely because the isotropic technique is the most used. Generally is less expensive than the dry etching techniques, but it is more dirty to the samples, leaving particles everywhere. Anisotropic wet etch is quite common in silicon machining. The etching is directly related with the silicon orientation given a specific angle of etching, generally 54.74° [94].

Figure A.13. Wet benches at INL cleanroom; SPTS Primax; SPTS Xactix.

In INL the chemical wet etch is done in the wet benches where different chemicals can be used to etch different materials. For anisotropic etch of Silicon, TMAH is used, for isotropic etch it depends on the material, there are very selective chemicals to etch different metals and oxides. Dry etching, is done in a SPTS machine, INL has five of them, all with different proposes, three of them, DRIE machines to etch, silicon, metals and oxides respectively. The other two machines are isotropic etching machines. SPTS Primax etches SiO2 isotropically using Hydrofluoric acid (HF) vapour and is very selective, not etching any other materials. SPTS Xactix etches Si Isotropically, using Xenon difluoride (XeF_2) in vapour that only etches silicon, not affecting masking layers like SiO_2 or photoresists.

e. Dicing

In microfabrication the substrate that is most used is silicon. Silicon generally is bought in wafer format, and the machines are normally build in to accept this silicon wafers. Generally in a single silicon wafer, thousands and thousands of devices can be done at the same time. On the end this wafer has to be divided into single devices, in order to test them, use them or even integrate them with other devices. Dicing is the technique to divide a wafer in single dies, and is generally the last step of every process in the cleanroom.

Usually a diamond grain blade is used to cut these wafers, achieving velocities of 30000 rotations per minute. This blades can go through silicon and individualize the wafer in small devices. In INL a Disco® machine (DAD3500) is used to dice silicon wafers, glass wafers, and other different substrates. It can handle up to 4 different directions simultaneously and can have different kinds of

blades, the most used blades measure 254 μm and 30 μm of thickness, making precise cuts without destroying the samples. It also has automatic alignment to know where the cuts need to be done and can cut substrates up to 3 mm of thickness.

Figure A.14. Dicing machine in the grey area of the cleanroom.

f. Metrology

For measurement and characterization, metrology is absolutely necessary in every fabrication flow. After every step in most of the exploratory processes, knowing etched depths, the chemical composition, deposited thin films thicknesses, particles and residues present in the substrates, give the user the possibility to understand, control and increase is knowledge of the process.

Optical microscopy and electron microscopy (SEM) are very useful to get an overview of the process, understanding if everything is being done as expected. In contrast with SEM, optical microscopy is the fastest and easiest step to do, but only for seeing sub-millimetre structures, up to some microns. SEM achieves really higher magnifications, up to the nanometre scale and can do 3D imaging. A tool attached to the SEM machine that can be useful in particle detection and chemical composition, is EDX, which can precisely measure all the chemical elements present in a certain focus point. In INL three optical microscopes are always available for all the users to analyse their samples, they all have lenses from 1x to 100x magnification, giving the possibility to measure precisely features till 1 μm of width. From FEI, inside the cleanroom there is a SEM with EDX that can go to magnifications of more than 1000000x giving the possibility of measure features up to

some dozens of nanometres. EDX works at high powers and works simultaneously with the SEM imaging, creating spectrums of materials in selected focusing points.

Figure A.15. Optical Microscope (left); SEM with EDX (right).

Thickness measurements of thin films is extremely important to predict the final working device properties. Knowing these values allows the control of different parameters, like electrical and optical properties. Meaning that generally, thicknesses are never neglectable in microdevices. To measure these values, direct and indirect methods are available in the fabrication centres. Mechanical profilometer is a technique where a small needle is dragged on top of the substrate, if any slope appears the needle will detect that will measure this thickness change. With this direct technique, thin films with dozens of nanometres can be easily measure without any complications. Indirect techniques like optical profilometer, are also important, but less relevant on optical opaque layers, like metals. Sheet resistance measurements for metal layers can also provide very precise measurements of thicknesses, but can't be used in electrical isolating layers. In INL cleanroom, these three systems are available giving a full metrology capability to every process. The mechanical profilometer is from KLA. Has a resolution from a few nanometers to hundreds of micrometers, and can measure substrates from 1-inch to 8-inch wafer. The optical profilometer, NanoCalc, is very useful for non-contact measurement of thin layers, it allows 2D and 3D topographies of substrates, measuring precisely from some nanometres up to $250\ \mu m$. Sheet resistance measurements make a direct relation between thickness and resistance of the material, this contact technique is available at INL, and is mainly used for sputtered and electrodeposited metals measurement.

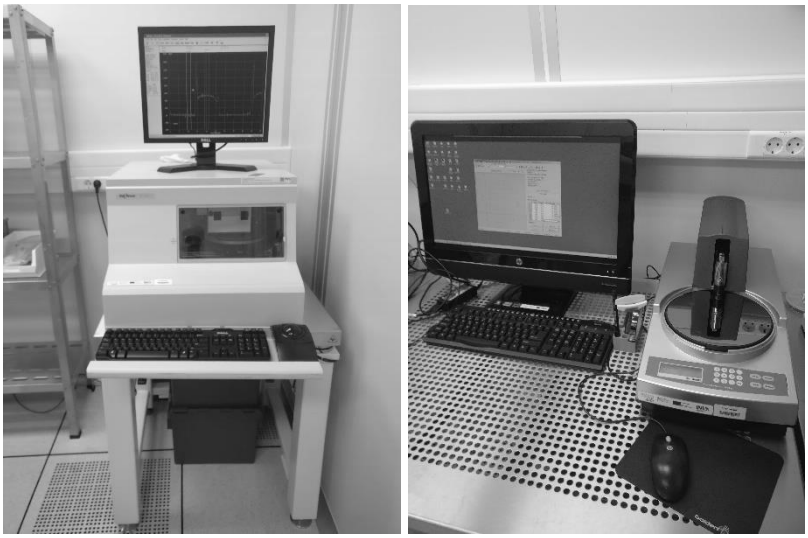

Figure A.16. Mechanical Profilometer (left); Sheet Resistance measurement system (right).

g. Electrodeposition

Electrodeposition (also known as electrochemical deposition or electroplating) is a process mainly used to electrodeposit metal films, from some microns to hundreds of microns thick. This technique is already used since the seventeen century, mainly to avoid corrosion, improve mechanical properties or even to create pieces of jewellery with gold coatings. Electrodeposition is based on electrochemical reactions that occur between different compounds generating the flow of ions between an anode and a cathode. These electrodes are dipped in an electrochemical solution and a current is injected between them, the metal ions will be reduced in aqueous, organic and salt solutions. To create this metal deposition, the substrate (cathode) needs to be conductive. In microelectronics, normally, a seed layer is deposited in order to create this conductive layer that will transport the electrons from the power source to the substrate. Since the solution is highly conductive, the electrons are released from the anode and go through it to finally bond in the cathode (Figure A.17). Two main reactions happen in this process (like a Redox reaction), one in the anode, where metal ions are released in the solution and another in the cathode, where the film is deposited. So, when selecting the electrolyte is important to have the metal ion already in solution. It is also important for this solution to react with the anode (pure metal) to oxidise it in order to compensate the ions that are attracted to the substrate [100], [101].

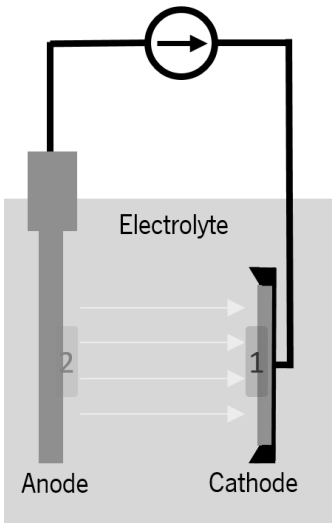

Figure A.17. Electrodeposition. In red is marked where the first reaction occurs, and in green the place where the second reaction takes place.

The electrodeposition process has a lot of variables, and every single one should be controlled for a better final deposit on the substrate. Injected current, distance between electrodes, temperature, agitation, concentration of ions in solution, conductivity of the seed layer and exposed area on the solution are the ones that will be considered in this project. Since the exposed conductive area will be directly related to the injected current, a main parameter will be used in this thesis called current density (A/cm^2). Then to know how our system works, we need the plating rate that will be given in ($\mu m/min$). This two parameters will be related and are described in detail in the chapter 3.2.

Unlike other fabrication techniques, electrodeposition generally does not get really high uniformities, but can go up to thicknesses that are not achievable in normal deposition processes like sputtering or thermal evaporation.

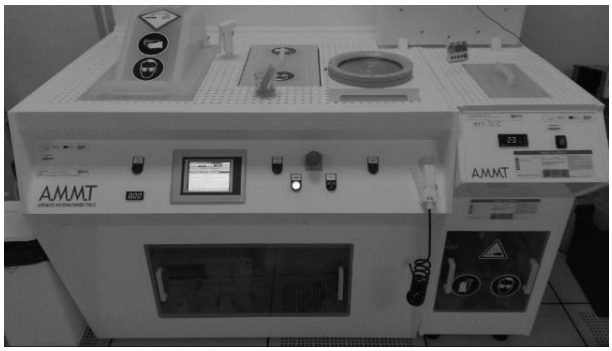

Figure A.18. A.M.M.T. Electrodeposition System.

At INL, a professional plating system from AMMT, Figure A.18, is used to electrodeposit copper, since we will not use copper plating in this project, this system will not be used. In INL, there are no equipment's to electrodeposit nickel and tin in full 8-inch wafers. Given this need to have different plated metals, a solution to electrodeposit different materials is presented on this thesis. Two electrodeposition setups, adapted to INL's cleanroom, were developed in house with milling processes in a 3 axis CNC Machine.

Appendix 2. Electrodeposition System Development

On Appendix 2, the extras that were needed on the fabrication of an electrodeposition setup are explained in detail. The solutions used as electrolytes, and their chemical compatibilities were analysed in detail, in order to avoid potential hazards and risks in the cleanroom. The chemical compatibility is also extremely important to understand what kind of substrates are compatible with this process. It is also presented a first electrodeposition setup that was designed but failed in functionality both for Ni and Sn.

a. Electrodeposition solutions

To electrodeposit metal films, an electrical potential is applied between and anode and a cathode that are dipped in a conductive electrolyte solution. The electrolyte is a solution that contains the ion of the desired metal that will be reduced on the surface of the substrate (cathode), creating thick films of metal. It is really important to select a good electrodeposition chemical in order to get good uniformity, good deposition rate, and a chemical that is not harmful for its users.

Nickel electrodeposition solution

Nickel electrodeposition is well implemented for more than 100 years. The first solutions appeared in the XVII century based on nickel nitrate solutions. On the next century they were improved, and Prof. Oliver Watts mixed nickel sulfate, nickel chloride and boric acid (Watts Solution), developing one of the most important solutions in the nickel plating history. After this developments the nickel sulfate was substituted by nickel sulfamate to improve the tensile stress of the deposits, but getting lower uniformities. Even so the Watts solution became quite popular and after a lot of development and research the semi bright solutions appeared. This solutions have the same chemical composition of the Watts nickel electrolyte, but they have organic additives that make the electrodeposited film more resistance to corrosion and more uniform. With such uniformity, Ni plating started being used for decorative applications. Other solutions like, nickel fluoborate are also used, but the main components of this solutions are always around nickel chlorides and nickel sulfates [100].

Two solutions were bought in this work, but both had quite similar results. The first solution from Caswell® [102], a company specialized in electroplating solutions that can be used anywhere. This solution is harmful for the environment and for the health of its user if is not correctly handled,

it is composed by Nickel salts (solid) that had to be diluted in distilled water. These Nickel salts are diluted in distilled water, as it is explained in the instructions. Caswell® also sells a Nickel Brightener containing organic additives that give better uniformity and better appearance to the electrodeposited thin films. This additive basically transforms this Watts solution in a Semi-bright solution.

Table 7. Caswell Nickel Plating Electrolyte

Chemical	Percentage (%)
Nickel Sulfate	17
Nickel Chloride	4
Boric Acid	1
Water	78

To prepare the solution, the distilled water should be heated up to 76 °C, then the nickels salts are poured in the water and the solution is mixed till it gets a homogenous appearance. After 12 hours of resting, the solution is ready to use. The manufacturer recommends to use 1100 mA per 100 cm^2, giving 11 mA/cm^2 of current density. With this current density, the expected values are 5 μm of thickness in 12 min, meaning that the plating rate will be 25 μm/h.

Another commercial electrolyte was bought afterwards. From Alfa Aeser® [103] called "Nickel plating solution semi bright finish". This solution is a lot similar with the previous one, the main reason to buy a new solution was mainly related with bureaucratic procedures. The main difference between this solution and the previous one is that the solution is already prepared and ready to use, without the need for mixing different components.

Table 8. Alfa Aesar Nickel Plating Electrolyte

Chemical	Percentage (%)
Nickel Sulfate	25
Nickel Chloride	6
Boric Acid	4
Water	65

The percentages are a little bit different, meaning that this solution is less concentrated than the Caswell® one. The manufacturer in this case does not give any information about the usage, the plating rate and the recommended current densities. So the same current densities should be considered for this electrolyte. Both solutions present a strong green colour, they are odourless and should be handled with gloves and a respiratory mask.

Tin electrodeposition solution

Tin electrodeposition is available worldwide, and is really important in the electronics, to enhance corrosion resistance and to increase solderability in PCB's manufacturing. The electrodeposition of such material is done in acidic and alkaline solutions, the acidic baths offer fast deposition rates while alkaline baths work without additives but with a slow deposition rate [97]. Since the findings that Lead is harmful for the human body, Sn based solders became the major components for electronics solderability. Automatic production of electronic circuit boards and semi-conductors, created the necessity for controlled electrodeposition of Sn. Pads with solder for easier solderability or ball grid arrays of Sn became a common process within the manufacturers. Since then, some chemistry brands started the production of electroless and electrodeposition eletrolytes that are nowadays commercially available [97].

Caswell was again the chosen company to buy the electrolyte solution for the Sn electrodeposition. This solution is operated at room temperature, and is constituted by the following chemicals:

Table 9. Caswell Tin concentrate Solution

Chemical	Percentage (%)
Stannous Sulphate	19
Sulfuric Acid	2
Water	79

In the datasheet it is written to mix this solution with Sulfuric Acid concentrated at 15%. For that, a solution of 15 mL of H_2SO_4 – 99% with 75 mL of H_2O was prepared. The final electrolyte should be constituted by 79% of this solution with 21% of Tin concentrate. After mixing both, the solution has a whitish colour and is odourless, but since is constitution is mainly sulphuric acid, the pH is really low.

In the datasheet is advised to use 1 A for each 65 cm^2, meaning that the current density of this solution is 15 mA/cm^2 giving a plating rate of 15 $\mu m/h$.

b. Materials selection

To build a compatible and reliable electroplating setup, the construction materials should be chosen wisely to avoid material incompatibilities that can cause dangerous incidents in the cleanroom. The A.M.M.T. system is a good example of which materials should be used in a system

like this. The full system and all of the plastic parts that constitute the main chamber are made in polypropylene. Polypropylene is compatible most of the chemicals including strong acids and bases. The seals are made out of EPDM and the basket lid that contains copper is made with titanium covered with platinum. This two metals are ideal to use in plating system because they are not corroded by the electrolytes. In the A.M.M.T. system they are used to make the electrical connection between the raw material and the power source. The elevated price of this materials could be a constrain in a possible final solution, so one of the first ideas is to avoid the metal contact with the electrolyte chemical. The wafer holder is made of polyether ether ketone (PEEK), another chemical resistant polymer that can also handle a lot of mechanical stress. This material is used in high performance demanding applications, ultra-high vacuum applications and even in medical solutions. Since the wafer holder is always being opened and closed, the robustness of the material is really important to have a strong part that can handle being screwed and unscrewed multiple times, and still make a good clamp between the wafer and the holder after thousands of iterations.

Electrodeposition of nickel (Ni) and electrodeposition of tin (Sn) are the two solutions that will be used in this process. For nickel, most of the available baths are acidic solutions (pH bellow 7) constituted by sulfamates and chlorides, dissolved in a high percentage of water. For tin plating, there are both acidic and alkaline solutions, being the first ones the most common. Normally they are constituted by sulfuric acid or fluoboric acid mixed with pure tin powders. After presenting the most aggressive chemicals to a supplier, three main polymers were suggested to use in this setups. Polyethylene (PE), Polypropylene (PP) and Polyether ether ketone (PEEK). Comparing the 3 polymers presented, PEEK would be the better in terms of chemical compatibility and mechanical properties, but is also the more expensive one. The chemical formula of this polymer is $C_{21}H_{18}O_3$, the melting point is high (343°C) and is yellowish in its raw form. Polypropylene is also really good in chemical resistance but with lower performance in mechanical properties when compared with PEEK. The chemical formula is C_3H_6, and the melting point 130°C. The raw material has also a yellowish appearance. Polyethylene is the worst one in mechanical properties, but as in this system there are no mechanical movements the mechanical properties can be ignored. The chemical resistance of this material is not as good as the last two, but it can be good enough for the proposed solution. The chemical formula of PE is C_2H_4, has a melting point around $115°C$ and the raw material is white. The main advantage of this material is the price (less than a quarter when compared with PP), and it's the easiest to mill with the CNC. For the sealing between parts in the system, Nitrile, Viton and EPDM rubbers are the most common in this kind of systems. Nitrile is the

cheapest one and is mostly used in water based applications, Viton is better than Nitrile in terms of chemical resistances, but is worse than EPDM. EPDM should be the better solution for systems leading with chemical components like acids and bases. For other parts like connections for tubing, and tubing itself, PVC, Teflon and ABS are the most common materials available for this applications. Teflon tape will also be very useful in the tubing interconnections, so this material should also be compatible with this chemical electrolytes.

Knowing the chemical compatibility between materials and strong chemicals is a really important matter when building a system like this one. When working in a cleanroom, and inside an environment shared with dozens of different users, any chemical release, or spill can be very dangerous and should be avoided at any cost. So investigating and understanding the risks and problems, when working with dangerous chemicals, is a big responsibility and all the measures, procedures of safety and control need to be considered.

c. Nickel electrodeposition chemical compatibility

Regarding the nickel electrodeposition setup it's important to verify all the nickel related chemical components to verify if they are compatible with all of the materials. Since one of the main objectives was the development of a full system that can electrodeposit on 8-inch wafers, the chamber of the system should be big, and the chosen dimensions were $500 \times 500\ \mathrm{mm}$ with a thickness of $100\ \mathrm{mm}$. So the first challenge was to find a supplier that could sell different plastic parts of different materials to mill in CNC with the required dimensions. PolyLanema® was chosen company, this company offers a big catalogue of different materials in different dimensions. Polyethylene and Polypropylene were the only polymers available in the supplier that could fit our needs. Comparing the prices of the different polymers available to mill, polyethylene was the one that could fit our needs and at the same time have a reduced price. Before buying the material, a chemical analysis was made to both polymers, in order to understand if it they can be reliable, and durable in such system. Since the system will deal with liquids and their flow between different places, it is extremely important to define the seals that will be used to avoid spills and leaks of the electrolyte. Normally this seals are made in grooves with an insertion of rubber materials that are squeezed. EPDM, Viton and Nitrile are three common materials used in this subject. For different connections and tubbing on the system, materials like polyethylene and polypropylene are not so common, other materials are available for this applications, like PVC and Teflon. This two materials are easy to find because they are used in water applications. Unfortunately that does not mean that

they can work in this system regarding the chemical compatibilities. In Table 10, the classification used for the materials is shown, and in

Table 11, the materials are classified for each chemical.

Table 10. Chemical compatibility classification.

S	**Suitable to use** – Can be used in every condition without any effects.
M	**Medium usage –** Can affect the material with high concentrations of certain materials and when temperature or pressure increases.
H	**Hazardous material –** Not suitable, compromises the full system, creating severe damage in the material

Table 11. Chemical compatibility for Ni plating solutions.

Materials	Nickel Sulfate	Ref.	Other Ni Salts	Ref.	Sulfuric Acid	Ref.	Boric Acid	Ref.	Other Acids	Ref.
Polypropylene	S	[104], [105]	S	[104], [105]	S	[104], [105]	S	[104], [105]	S	[104], [105]
Polyethylene	S	[104]–[106]	S	[104]–[106]	M	[104], [105]	S	[104], [105]	M	[104], [105]
EPDM	S	[107]–[109]	S	[107]–[109]	M	[107]–[109]	S	[107]–[109]	M	[107]–[109]
Viton	S	[107]–[109]	M	[107]–[109]	H	[107]–[109]	S	[107]–[109]	M	[107]–[109]
Nitrile	S	[107], [108]	S	[107], [108]	H	[107], [108]	S	[107], [108]	M	[107], [108]
PVC	S	[104], [105], [110]	S	[104], [105], [110]	S	[104], [105], [110]	S	[104], [105], [110]	S	[104], [105], [110]
Teflon	S	[104], [108], [111]	S	[104], [108], [111]	M	[104], [108], [111]	S	[104], [108], [111]	M	[104], [108], [111]

Polyethylene like said before, is not the best material for mechanical resistance but has high compatibility with nickel plating solutions confirmed with three references from companies that deal with chemical materials and chemical resistances. Regarding the o-rings in the system all the materials should work with nickel plating baths, but nickel baths with Sulfuric Acid should be avoided. This acid is harmful for the selected materials, so if this solution ends up being used, these seals can only be made of EPDM. If the solution does not contain strong acids, Nitrile is a cheaper

calculation, because, since it will be submerged in the electrolyte his volume should be subtracted to the inner chamber volume. Considering the wafer holder a perfect cylinder, the volume is approximately 1363 cm^3. Making the simple calculation of total volume on the inner chamber, the final volume of electrolyte that the main chamber can handle is approximately 5.1 L, the maximum overflow that the outer chamber handles is 0.85 L. So the maximum litters of electrolyte that the system can handle is 5.9 L. Considering this maximum volume, for a electroplating setup, 5.5 L of electrolyte are enough to work with this system, 5.1 L will stay on the inner chamber and 0.4 L will overflow to the outer chamber, filling only 50% of the total volume that the outer chamber can handle. To perform this recirculation, a chemical diaphragm pump was added to the system with the inlet in the outer chamber, and the outlet in the inner chamber. Some PVC adapters were added to interconnect the tube from the pump to the chambers, also in this interconnection, teflon tape and one o-ring were added to prevent any leakage that can possible occur here.

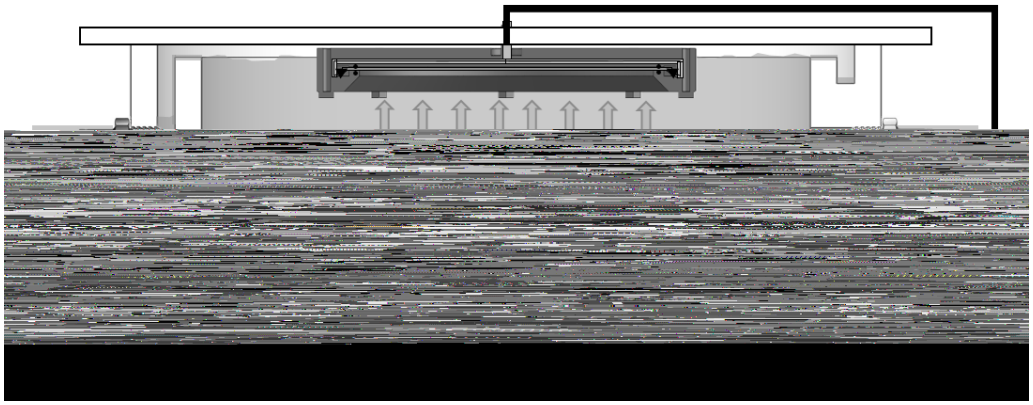

Figure A.20. Cross Section A-A' from Figure 3: Full system.

The full system is represented in Figure A.20. A small pump was selected to circulate the liquid in the chamber. This pump was selected to be compatible with most chemical baths, and to have a low circulation flow, it was important to verify that the wet parts of the pump are all made out of polymers and not metals, since this electrolytes are very corrosive to most of the metals. The selected pump from Xylem® (RLF122202D) has an output flow of 3.8 litres/minute for 12V of input voltage, this voltage can be adjusted to lower values for different flow rates. A power supply of 9 V was used, giving the pump a capacity of 2.8 litres/minute. With this flow, the full amount of liquid circulates in approximately 2 minutes. This low flow rate can give us a more stable deposition on the electrodeposition process. To control the current injected between the cathode and anode a Keysight® power meter was connected to the top and bottom of the chamber, the cathode is on the wafer holder (substrate) and the anode on the bottom of the chamber (metal plate). The power

meter can be regulated to the microampere scale, promoting a very stable electrodeposition in time. The distance between the anode and cathode was fixed at 6 cm by milling constrains. The temperature used in the first tests will be room temperature, 21°C. In the future, if needed, a temperature controller with a chemical resistant resistor could be added for heating the solution. In the end the only two variables that will be changed in the process will be time and injected current.

After selecting and buying the materials, 3 plates of PE were bought with the following dimensions, one plate with 500 x 500 mm and a thickness of 100 mm to make the main chamber, two plates of 500 x 500 x 30 mm to make the cover and the ring for the cathode. Another plate was bought later with 700 x 400 x 25 mm to make other necessary parts, like the feet of the system. The CNC machine used to mill the parts required, was the Flexicam Viper. This system is constituted by a table of 600 x 600 mm of work area, and can handle 5 different tolls at a time, being able to interchange them without the help of the user. The machine works with G-Code like common 3D printers. The software used to design the paths, commands and to generate the files for the CNC machine was ArtCAM®, this CAD software generates toolpaths according to the milling paths that we want to achieve. Every tool has five parameters that have to be defined on the software. This parameters are: Stepover - mm (the lateral step that the tool will make to mill the next line in X and Y); Stepdown - mm (the down step that the tool will make to mill the next entire layer in Z); Feed Rate – mm/sec (The velocity that the tool moves in X and Y); Plunge Rate – mm/sec (The velocity that the tools moves in Z); Spindle – r.p.m. (The velocity that the tools is rotating). For each tool this five parameters need to be well defined because, breaking a tool, or destroying the part that the machine is milling is easy. Since we are mechanically ablating the polymer, the forces exerted on the tool are very strong, especially on the X and Y movement. Since the system only works in 2D all the designs need to be drawn on the top plane. ArtCAM has three main toolpaths that can be used to make different structures, “Profile Toolpath” – were the tool will follow a line and mill around it, “Area Clearance Toolpath” – were the tool cleans an entire area between limits, “Drilling Toolpath” – were the tool drills a hole in Z depending only on the diameter of the tool.

Figure A.21. Detailed ArtCAM process.

As an example in Figure A.21 it's shown the main chamber milling process design on ArtCAM. The toolpaths are seen from above, and the drilling heights are defined in each toolpath. For each part of this system different toolpaths were generated for the different geometries. The used tools in this process, ordered by size were the following: EndMill 1 mm; EndMill 4 mm; EndMill 8 mm. The biggest tool (8 mm) was used for bigger area clearances, the small tool (1 mm) for thinner details on the system, like the o-rings and corners, the 4 mm tools were used to make drills for the screws that will fix the fixing ring of the metal plate. The parameters for each tool are shown in Figure A.22. Tool number 4 was used only to drill so the Stepover is not a parameter that the tool needs.

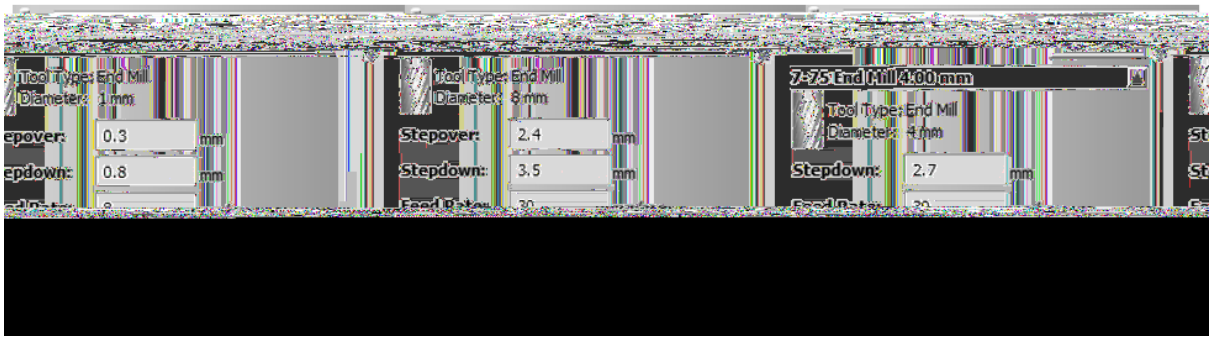

Figure A.22. Parameters used in the tools for the main chamber.

After calculating everything and defining every toolpath, the setup is ready to be done. To machine the main chamber a block with 500 x 500 x 100 mm was glued with double side tape to the machine stage. The EndMill tools were placed in position 1, 3 and 5, and the process is done with water flowing to the tip of the tool. The water provides cooling to the contact between the plastic and the tool. If no water or lubricant is poured, the plastic melts and the final result will not be what was designed. The process took more than 30 hours to machine, and the final result is shown on the next figure.

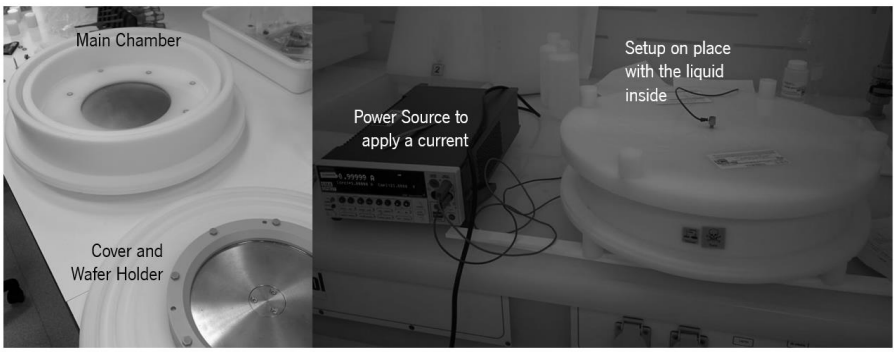

Figure A.23. Machined system and first tests of the system with an electrolyte and power source.

Before processing final wafers on the system, an 8-inch dummy wafer was placed on the wafer holder. This wafer made of silicon, had an adhesion and a seed layer, deposited with sputtering. The adhesion layer of tantalum has 10 nm of thickness and the seed layer 200 nm of copper. The current, like said before and explained in 3.3, is injected in the border of the wafer. The maximum current that the power source can give is 1 A, injecting this current on a full wafer, which has approximately 305 cm^2, gives a current density of 3.27 mA/cm^2. This value is low when compared with the datasheet recommendation, but this is the maximum value that our system can handle for such a big area. In the future using masking materials, this area will be hundred times lower, meaning that the current density will be hundreds of times bigger.

To characterize the system, a current is injected continuously for two hours long. To characterize the thin film on the end, the four point probe - sheet resistance and the mechanical profilometer metrology systems can give us the thickness of the thin film, and with that, the deposition rate can be determined. With the deposition rate the full system can be adapted to each situation and the plating rates, current densities and times can be calculated to obtain the desired thicknesses.

Unfortunately after a couple of tries, it was found that the system was not conducting current between the cathode and the anode. For the power source it was an open circuit giving the max available voltage of 21 V and passing 0 A between the two sides. Leaving the wafer dipped on the electrolyte is also not good for the seed layer that starts to be etched by this liquid. This problem was not solvable because the system was badly designed in the positioning of the cathode. Being directly above the anode, when the cover is placed in the system, a layer of air stays between the wafer and the liquid, retained on the wafer holder. Even with the pump working at the maximum rate, the air does not leave and the electrodeposition process does not occur, meaning that this system is not capable of doing electrodeposition. Looking at the A.M.M.T. professional system, the cathode is above the anode, but it is tilted 45°. This feature was ignored when designing this system to be easier to mill in the CNC. Unfortunately this fatal error makes the system useless for this microfabrication processes.

f. Tin electrodeposition system – Rectangular Approach

Since the Nickel electrodeposition setup presented in chapter 3.2, worked really well to electrodeposit nickel in 8-inch wafers, for the tin plating system, the same, design, conditions and materials were used. In this case the O-rings were checked, and the pump had to be different regarding the chemical compatibility with sulfuric acid. A new pump was acquired, with the same flow, but different materials inside and a different mechanism of pumping. This new pump from Flojet® works connected to $230\ \mathrm{V}$, has a flow of 3 litres/minute and has a magnetic coupling between the motor and the moving parts of the pump. This magnets are covered by polypropylene that has a really good chemical resistance to strong acids. The design is the same that was used in 3.2.1, regarding the ArtCAM all the files were also already ready to machine, this are the same presented in the previous chapter, and described in 3.2. The materials were bought in the same company and after one week of work the system was ready to be placed and start electrodepositing tin.

The system was filled with approximately 7 litres of Sn electrolyte solution. The current between the two electrodes was $1\ \mathrm{A}$ (maximum current that could be applied with the power source), for $60\ \mathrm{min}$ straight. The results were not satisfactory, the thin film didn't look uniform after taking the wafer off and some places in the wafer looked like copper. This had to be analysed in the microscope to check how the grain of electrodeposited tin, his size and uniformity.

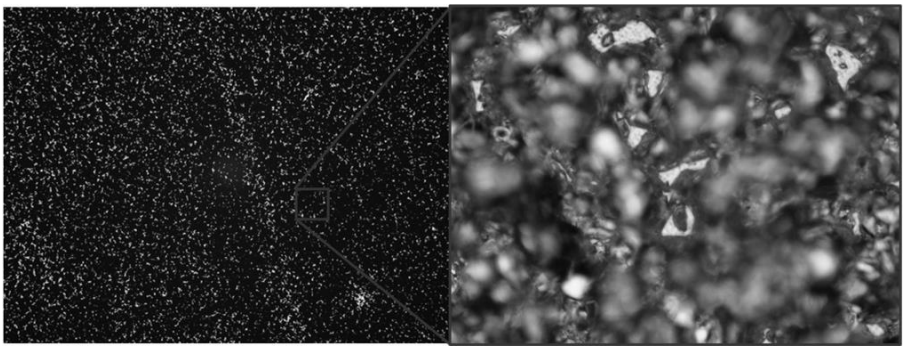

Figure A.24. Electroplated Sn thin film on an 8-inch wafer.

The wafer didn't had an electrodeposited thin film, but a big group of small islands of tin grains. This accumulation was far from perfect and a lot of places didn't had any tin at all. At first the main thought that came was the higher current density which gave priority to some places, and then the big grains accumulated only in some places, this makes the resistance lower on this places, making the current flow only through the Sn that was previously deposited. The current was lowered to half and the time was the same. So a process with $500\ \mathrm{mA}$ in one hour was processed and the results were almost the same ones as shown in Figure A.24. After analysing again the datasheet from the chemical, the recommended current density is more or less $15\ \mathrm{mA/cm^2}$, 5 times more than the maximum current that our power source can inject. This could be the major problem for a not correct current distribution in the full wafer, and therefore, the thin film is not uniform on the surface. Since we were not able to do electrodeposition in a full 8-inch wafer, the next test was to electrodeposit on a predefined mask, to test if the structures can be filled in Sn. The mask that was used had $1.1\ \mathrm{cm^2}$ of exposed area. Considering that the minimum current density should be $15\ \mathrm{mA/cm^2}$, the injected current for that exposed area should be $16\ \mathrm{mA}$. The results once again were not satisfactory and after some days recirculating the electrolyte became white when it was transparent before.

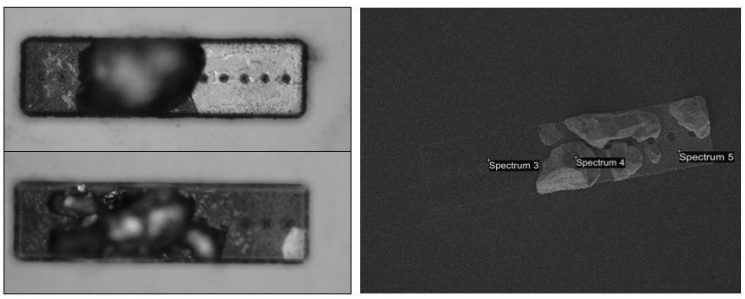

Figure A.25. Structures no entirely filled with Sn deposits. EDX spots were the spectrums were measured.

In Figure A.25 is observable that not every place was filled with Sn in the electrodeposition, and similar to the full wafer, only in some places the Sn grains grew, and in this places they achieved really thick heights (approximately $50\ \mu m$). Since it was hard to distinguish from the colours the different components in the image, an EDX analysis was made to determine what material was there. The resist was removed, the wafer was placed on SEM and the EDX was measured on one of the structures that had this 3 different colours.

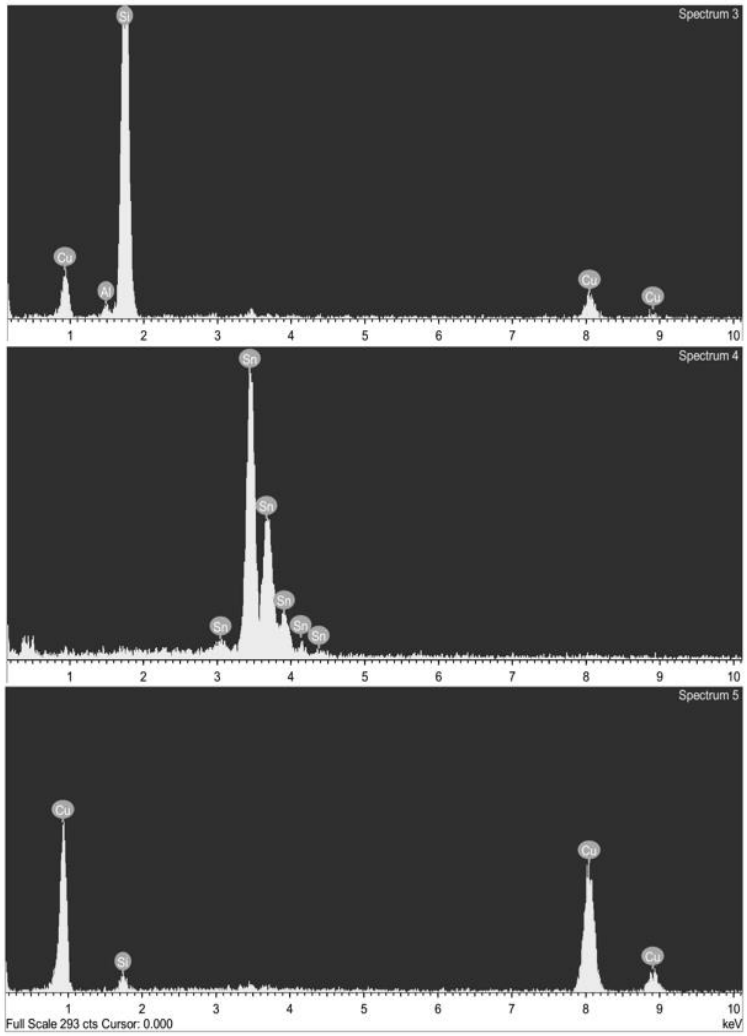

Figure A.26. EDX for spectrum 3, 4 and 5. Same Y scale in every spectrum.

After analysing the spectrums it is clear that in area 3 (Figure A.26), the copper is there but most of it was etched, giving a big spike on silicon and two small spikes in copper. There's also a small spike in Al because the passivation layer between the copper and the Silicon was Al_2O_3. In area 5 (Figure A.26), the copper is still there (probably the $200\ nm$ of the seed layer), because two big spikes appeared for copper and only a small one for Silicon. In area 4 (Figure A.26), we are

now sure that the deposition is in fact Sn, and no other alloys of Sn. If the solution etched everyplace that was not covered by Sn, area 5 should be etched also, but that was not verified. Unfortunately this is a really hard result to interpret, maybe since we have really small structures, in some places some air bubbles can be blocking the deposition, but the liquid was flowing, so this shouldn't be happening. Even so with this test we were able to verify that in some places the Sn is there, meaning that the electrolyte is depositing the correct material.

Three more tests were made in order to verify how the area is covered in each die. For that calculation a Wolfram Mathematica® script was made in order to process the images and calculate the area that was filled in each case. This script compared the result that was supposed to be obtained with the 12 images taken by the automatic microscope in three different wafers with different parameters. The following table shows the parameters used in each wafer.

Table 13. Parameters used in 3 control wafers

Wafer	Time (min)	Injected Current (mA)	Current Density (mA/cm^2)
1	16	20	18,18
2	8	40	36,36
3	4	80	72,72

With double currents in between the three wafers, and half of the time, the expected thickness should be the same. Measuring in the profilometer, this assumption was verified and most of the samples had an average 50 µm of thickness.

The script made in Mathematica separates everything that is Sn deposits from other components in the optical photo. In Figure A.27 a) the objective values are shown, the black parts are the exposed areas where we want Sn to be deposited. So to have a perfect electrodeposition, the number pixels in black shown in a) should be the same on the other images. In b), c) and d) it's observable the original and the converted image annexed to the percentage of Tin covered in the exposed area. With a Mathematica® script it becomes easy to understand that with an increase of current, the covered area also increases in percentage, but 80 mA where not enough to electrodeposit everywhere, and in 4 minutes, we already had 50 µm of thickness. Since our objective is 15 to 25 µm, 2 minutes would be enough on this current and not every place would be covered by Sn. Meaning that in terms of time range to electrodeposit Sn we would be confined to some seconds, and since this system is not that precise, the results would not work for this process.

The following table shows the percentages that the script calculated for each die in the three wafers. In wafer 1 the filled percentage is around 25%, in wafer 2 is 30%, and in wafer 3 is 53%.

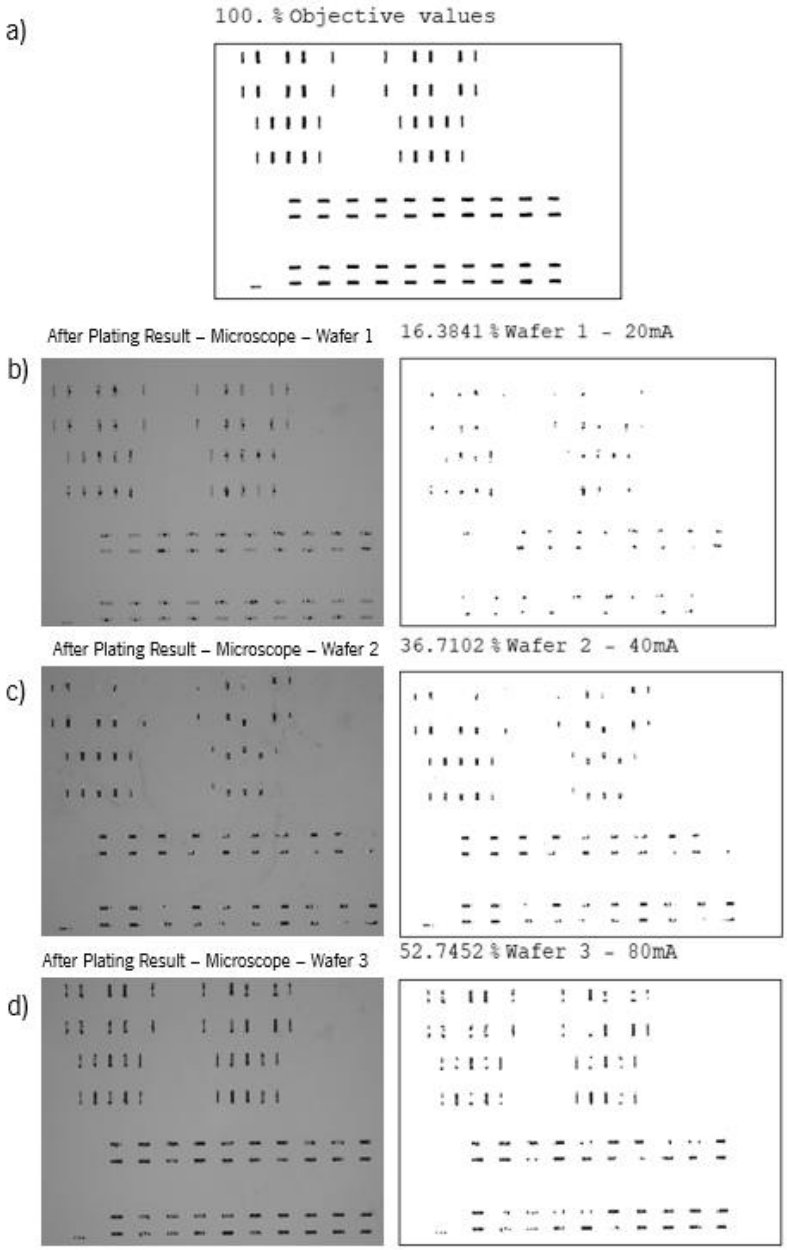

Figure A.27. a) 100% filling in exposed substrate; b) Die 4 in wafer 1, microscope image versus Mathematica output; c) Die 4 in wafer 1, microscope image versus Mathematica output; d) Die 4 in wafer 3, microscope image versus Mathematica output.

Table 14. Results in thickness in the 3 control wafers

Die	1	2	3	4	5	6	7	8	9	10	11	12
W01 %	17.25	22.65	24.28	16.38	26.28	31.69	32.11	28.61	25.71	26.93	24.24	25.53
W02 %	25.12	23.67	29.62	36.71	24.52	20.60	33.63	37.17	37.60	31.91	28.39	34.22
W03 %	53.77	52.07	47.92	52.74	47.32	56.02	49.32	50.67	57.129	60.80	59.94	56.30

With this three wafers, we conclude that this area covered by Sn is not directly proportional to the injected current, meaning that nothing will guarantee that injecting 160 mA (double the current from wafer 3) we will cover 100% of the exposed area. Even if this happens (with 160 mA), 1 minute would be enough to deposit 25 μm of Tin. Since this manual system is not that precise in time and that we cannot take it out of the bath in milliseconds, it is impossible to control the electrodeposition by the second. Concluding that this manual plating system for Sn deposition does not work properly like expected. The problem is directly related with the manual milled setup, and because we have an exposed area of $1.1\ \mathrm{cm}^2$ in a $300\ \mathrm{cm}^2$ wafer. The current is not being equally distributed on the wafer making defects in almost all of the exposed structures.

Appendix 3. Recipes of different techniques

On this appendix the recipes used in the different equipments is presented.

a. Al2O3 Deposition – Timaris FTM

Recipe Process Parameter (INL Al2O3 100nm 1500W 200sccm)	Settings
Deposition rate	6.66 nm/min
Process time	30 min
Passages	70
Ar flow	200 sccm
ADC Power	1500 W
Base Pressure	5E-5 mbar
Stage movement speed	15 mm/sec

b. Adhesion and Seed Layer Deposition - Kenosystec

Recipe Process Parameter (1-Man_C02_Ta_RF100W_20sccm)	Settings
Deposition rate	9.1 nm/min
Process time	1min6s
Ar flow	20 sccm
ADC Power	100 W
Base Pressure	5.1E-7 mbar
Wafer rotation speed	28 rpm

Recipe Process Parameter (1-Man_C09_Cu_DC100W_20sccm)	Settings
Deposition rate	4.26 nm/min
process time	47
Ar flow	20 sccm
ADC Power	100 W
Base Pressure	5.1E-7 mbar
Wafer rotation speed	10 rpm

c. a-Si CVD Deposition – SPTS PECVD

Recipe Process Parameter (Low-T a-Silicon 550mTorr)	Settings
Deposition Rate	12.44 nm/min
process time	40min11s
SiH_4-5 flow	35.5 sccm
H_2 Flow	52.5 sccm
HF Generator	30 W
Lower Electrode Inner	150 °C
Upper Electrode	150 °C
Chamber	75 °C
Base pressure	6 mTorr
Process pressure	550 mTorr

d. First Lithography – SUSS Gama Cluster + SUSS Mask Aligner MA6B6

Vapor prime recipe process parameters (4)	Settings
Oxygen and water vapor removal	heat and vacuum pump
Material	HMDS
Temperature	150 °C
HMDS exposure Time	5 minutes/300 s
Recipe total time	31 minutes

Spin coating Recipe process parameter (Coat AZ9260 for 8inch 3000 NOEBR)	Settings
Media temperature	22 °C
Photoresist	AZ9260 (MicroChemicals/ AZ Electronic Materials)
Thickness	8 µm
Dispense speed	300 rpm
Spread speed	3000 rpm

Soft bake recipe process (110C-60sec)	Settings
Type of hotplate	contact
Temperature	110 °C
Time	165 s

Exposure Recipe process parameters	Settings
Light source	Super High Pressure UV lamp 350 W
Filter	Broadband
Exposure dose	1763.2 mW/cm^2 (target)
Light intensity broadband	39.4 mW/cm^2 (measured)
Light intensity non-uniformity	1.34 % (measured)
Total exposure time	44.75s (dose/intensity – calculated)
Exposure mode	Hard Contact
Alignment Gap	20 µm

Recipe process parameters (120s Dev AZ 400K Puddle 8-inch)	Settings
Media Temperature	23 °C
Media	AZ 400K Developer (MicroChemicals/ AZ Electronic Materials)
Pre-wet	DI water for 3 s
Developer Dispense technique	puddle for 6 s
Washing	DI water for 20 s
Drying	4000 RPM for 30 s

e. a-Si etching – SPTS Pegasus

Recipe process parameters (PEG10)	Settings
Etch Rate	250 nm/min
Process time	180 s
Platen	HF (Low Frequency)

Mode	Continuous
Pressure	15 mTorr
C_4F_8 dep flow	160 sccm
SF_6 etch flow	120 sccm
O_2 etch flow	0 sccm
13.56MHz Coil Power	2000 W
380Kkz Platen Power	45 W
Coil matching unit	Full auto - load 50 - Tune 50
Platen Matching unit	Manual - load 50 - Tune 50
Platen chiller	20 °C
backside cooling pressure	10000 mTorr

f. Second and Third Lithography - SUSS Gama Cluster + SUSS Mask Aligner MA6B6

Vapor prime recipe process parameters (4)	**Settings**
Oxygen and water vapor removal	heat and vacuum pump
Material	HMDS
Temperature	150 °C
HMDS exposure Time	5 minutes/300 s
Recipe total time	31 minutes

Spin coating Recipe process parameter (2x Coat AZ9260 for 8inch 1000 NOEBR)	**Settings**
Media temperature	22 °C
Photoresist	AZ9260 (MicroChemicals/ AZ Electronic Materials)
Thickness	20 µm
Dispense speed	300 rpm
Spread speed	1000 rpm

Soft bake recipe process (110C-60sec)	**Settings**
Type of hotplate	contact
Temperature	110 °C
Time	95 s

Exposure Recipe process parameters	**Settings**
Light source	Super High Pressure UV lamp 350 W
Filter	Broadband
Exposure dose	3762 mW/cm^2 (target)
Light intensity broadband	39.4 mW/cm^2 (measured)
Light intensity non-uniformity	1.34 % (measured)
Total exposure time	95.48 (dose/intensity – calculated)
Number of cycles	5
Exposure time per cycle	19.1 s
Exposure mode	Hard Contact
Alignment Gap	20 µm

Recipe process parameters (2x 120s Dev AZ 400K Puddle 8-inch)	**Settings**
Media Temperature	23 °C
Media	AZ 400K Developer (MicroChemicals/ AZ Electronic Materials)
Pre-wet	DI water for 3 s

Developer Dispense technique	puddle for 6 s
Washing	DI water for 20 s
Drying	4000 RPM for 30 s

Appendix 4. Runsheets

The runsheets were everything is noted and every parameter is explained in INL cleanroom is showed on this appendix. In every runsheet the process is described step-by-step, and the cleanroom administrators have access to them. With it, becomes easy to track problems or identify where the process failed.

a. Mask Runsheet at INL Cleanroom

Runsheet
MEMS_Folded3D-FabricationOfHardMasks
(released on 30/07/2018)

Verified/approved by
João Gaspar

PS NO.	PROCESS STEP	PROCESS OVERVIEW	PROCESS DETAILS
0	Cr Hard Mask Blank	System: Not applicable Engineer: JoseF / Eurico M Date completed: 08/10/2017	Wafer(s) name: M01-M03 Material: Cr_Mask_Blank Wafer thickness: 900 microns Number of substrates: ___3___ (Specify number of substrates to process) Substrate size: 7x7x0.90 SL LRC 5M 1518 5K Supplier: Nanofilm - MB Whitaker Substrate type: CR HARDMASK BLANK Layers: Sodalime/CrO/Cr/CrO/Resist Type: LRC Lot No: _____ Resist / thickness: AZ1518 / 530nm Pre-bake: 103ºC 30 MIN Glass grade: Master Overall process description: Conventional mask fabrication (litho on glass / Cr with resist / manual development / resist strip / mask cleaning) (* Insert additional process parameters or details here *)
1	Lithography 0.53um AZ1518 on Cr Mask Blanks using DWL	System: Multiple Engineer: JoseF / Eurico M Date completed: 08/10/2017	Substrate(s) name: M01-M03 Side to be processed: FS (* Insert additional process parameters or details here *)

1.1	Exposure	System: Heidelberg DWL 2000 (LIMS-ID 00000917) Engineer: JoseF / Eurico M Date completed: 08/10/2017 - 09/10/2017	Wafer(s) name: M01-M03 Side to be processed: FS Material to expose: Resist Exposed material: ResistExp Mask file: INL_MEMS078_Folded3D_V03.dxf Conversion job: INL_MEMS078_Folded3D_L01C / INL_MEMS078_Folded3D_L02C / INL_MEMS078_Folded3D_L03C Layer converted: L01C / L02C / L03C Counts Nr: 1 CD bias ZX / CD bias ZY: NA Exposure map: INL_MEMS078_Folded3D_L01C / INL_MEMS078_Folded3D_L02C / INL_MEMS078_Folded3D_L03C No. rows / no. columns: 1 / 1 Field zero: 1 Field width x height: 172800 x 172800 um x um X offset (um) / Y offset (um): (0 / 0) Align each die automatically? No (Ali empty) Notch position: Down (towards -Y) Alignment coords: NA Focus: -80 Energy:60 Exposure time: _____ (* Insert additional process parameters or details here *)
1.2	Manual Development	System: Wet Bench 1 for Resist Strip Processes (LIMS-ID 00000898) Engineer: JoseF / Eurico M Date completed: 08/10/2017 - 09/10/2017	Wafer(s) name: M01-M03 Material to be removed: ResistExp Side to be processed: FS Resist / thickness to develop: AZ1518 / 0.53um Developer: AZ400K Sequence: Immersion in develloper / DI rinse / N2 dry Time/Temp/Agitation in developer: 90sec / RT / mild agitation Additional time: _____ sec Time/Temp in DI H20 + dry: Rinse + 10 min / RT + N2 blow dry (* Insert additional process parameters or details here *)
1.3	Optical Inspection	System: Optical Microscope Nikon Eclipse L200N (LIMS-ID 00000911 or 00000912) Engineer: JoseF / Eurico M Date completed: 09/10/2017 - 10/10/2017	Sampling: _____ (All wafers / every 2nd wafer / other) Magnification: _____ (x1 / x2 / x5 / x10 / x20 / x50 / x100 / other) Inspection sites: _____ (C L R N ON / map / other) Monitor alignment: _____ (Yes / No) (* Insert additional process parameters or details here *)

1.4	Wet Cr Etch	System: Wet Bench 4 for HF / Etching Processes (LIMS-ID 00000896) Engineer: JoseF / Eurico M Date completed: 09/10/2017 - 10/10/2017	Wafer(s) name: M01-M03 Side to be processed: FS Material(s) to etch: {Cr} Thickness to etch: 0.5 microns Substrate: Mask Target material / etch depth: Cr / ca. 0.5 um - etch through Mask layer / thickness: AZ1518 / 0.53 um Etch stop layer / thickness: Glass substrate / 0.9 um Overetch: _____ % Wet chemical etchant: ETCH18 Cr Etchant Time/Temp/Agitation in etchant: Exactly ca. 1m40s / RT / mild agitation Additional time: _____ min Time/Temp in DI H20 + dry: Rinse + 10 min / RT + N2 blow dry (* Insert additional process parameters or details here *)
1.5	Optical Inspection	System: Optical Microscope Nikon Eclipse L200N (LIMS-ID 00000911 or 00000912) Engineer: JoseF / Eurico M Date completed: 09/10/2017 - 10/10/2017	Sampling: _____ (All wafers / every 2nd wafer / other) Magnification: _____ (x1 / x2 / x5 / x10 / x20 / x50 / x100 / other) Inspection sites: _____ (C L R N ON / map / other) Monitor alignment: _____ (Yes / No) (* Insert additional process parameters or details here *)
1.6	Resist Strip using Microstrip 3001	System: Wet Bench 2 for Lift-Off Processes (LIMS-ID 00000899) Engineer: JoseF / Eurico M Date completed: 09/10/2017 - 10/10/2017	Wafer(s) name: M01-M03 Material to be removed: Resist Side to be processed: FS Substrate: Mask Resist / thickness to strip: AZ1518 / 0.53um Chemical/stripper: Microstrip 3001 Time/Temp/Agitation in stripper: ca. 5min / RT / mild agitation Additional time: _____ min Time/Temp in IPA: Rinse + 10 min / RT Time/Temp in DI H20 + dry: Rinse + 10 min / RT + N2 blow dry (* Insert additional process parameters or details here *)
1.7	Optical Inspection	System: Optical Microscope Nikon Eclipse L200N (LIMS-ID 00000911 or 00000912) Engineer: JoseF / Eurico M Date completed: 09/10/2017 - 10/10/2017	Sampling: _____ (All wafers / every 2nd wafer / other) Magnification: _____ (x1 / x2 / x5 / x10 / x20 / x50 / x100 / other) Inspection sites: _____ (C L R N ON / map / other) Monitor alignment: _____ (Yes / No) (* Insert additional process parameters or details here *)

1.8	Plasma Resist Strip - SPTS_Cont_LowT_RStrip_5min	System: Tepla Plasma Asher (LIMS-ID 00000876) Engineer: JoseF / Eurico M Date completed: 09/10/2017 - 10/10/2017	Wafer(s) name: M01-M03 Material to be removed: Resist Run #: 13141/13142/13143 Recipe: SPTS_Cont_LowT_RStrip_5min Etch time: 5 min Nr of runs: 1 O2 flow: 200 sccm CF4 flow: 20 sccm Ar flow: 200 sccm Power: 230 W Initial pres.: 0.2 mbar Pressure: 0.657 / 0.655 / 0.656 Max. Temp.: 51.8 /50.0 /50.0 Wafer(s) location in boat: Mask on top of sup wafer (* Insert additional process parameters or details here *)
1.9	Optical Inspection	System: Optical Microscope Nikon Eclipse L200N (LIMS-ID 00000911 or 00000912) Engineer: JoseF / Eurico M Date completed: 09/10/2017 - 10/10/2017	Sampling: _____ (All wafers / every 2nd wafer / other) Magnification: _____ (x1 / x2 / x5 / x10 / x20 / x50 / x100 / other) Inspection sites: _____ (C L R N ON / map / other) Monitor alignment: _____ (Yes / No) (* Insert additional process parameters or details here *)
1.1	Mask Cleaning	System: Multiple Engineer: JoseF / Eurico M Date completed: 09/10/2017 - 10/10/2017	Substrate(s) name: M01-M03 Side to be processed: FS (* Insert additional process parameters or details here *)
1.11	Piranha Cleaning	System: Wet Bench 3 for HF / Etching Process (LIMS-ID 00000896) Engineer: JoseF / Eurico M Date completed: 09/10/2017 - 10/10/2017	Substrate(s) name: M01-M03 Side to be processed: FS Chemical: Piranha (250 ml of H2O2 30% then sample then 250 ml of H2SO4 98% - only glassware and Teflon no plastics!) Time / Temp / Agitation in Piranha: 10 min / RT / mild agitation Quenching: H20 rinse / 5 min (* Insert additional process parameters or details here *)
1.12	Thourough Water Rinse and Drying	System: AMMT uGalv 200 (LIMS-ID 00000901) Engineer: JoseF / Eurico M Date completed: 09/10/2017 - 10/10/2017	Substrate(s) name: M01-M03 Side to be processed: FS Time in running H20: >10 min N2 blow dry: check (* Insert additional process parameters or details here *)
1.13	End of Run	Engineer: JoseF / Eurico M Date completed: 09/10/2017 - 10/10/2017	(* Use this area to insert process remarks *)

b. Runsheet used in INL Cleanroom on the last process

Runsheet
20180730_MEMS_Folded
3D-Test8 (released on
30/07/2018)

Verified/approved by
J. Gaspar

PS NO.	PROCESS STEP	PROCESS OVERVIEW	PROCESS DETAILS
0	Silicon Substrate (SSP)	System: Not applicable Engineer: JF Date completed: 30/07/18	Wafer(s) name: W09 - W18 Material: Si Wafer thickness: 725 microns Number of substrates: 10 (Specify number of substrates to process) Substrate size: 200 mm (4-inch / 6-inch / 200mm / other) Finishing: SSP (SSP / DSP / other) Other data: _____ (Provider / part number / geometrical factors / other) (* Insert additional process parameters or details here *)
2	Sputter Deposit Al2O3	System: Singulus Timaris FTM (LIMS-ID 00000889) Engineer: JF Date completed: 30/07/18	Wafer(s) name: W09 - W18 Side to be processed: FS Material to be deposited: Al2O3 Target thickness: 100 nm Recipe: INL MEMS Al2O3 100nm Pre etch: None No. passages: 70 Speed (mm/sec): 15 Power: 1500 W Ar flow (sccm): 200 N2 flow (sccm): 0 (* Insert additional process parameters or details here *)
3	Sputter Deposit Ta/Cu	System: Kenosystec (LIMS-ID 00000002) Engineer: JF Date completed: 02/08/18	Wafer(s) name: W09 - W18 Material to deposit: Ta / Cu Target thickness: 10nm / 200nm Recipe: C04 - Ta_250mA_20sccm Recipe2: C09 - Cu_250mA_20sccm Ar flow: 20 sccm Current: 250 mA Wafer rotation speed: 28 rpm Time: 126 sec / 2857 sec

4	PECVD HF-Si 150ºC	System: SPTS CVD (LIMS-ID 00000880) Engineer: JF Date completed: 03/08/18	Wafer(s) name: W09 - W18 Side to be processed: FS Material to be deposited: HF-Si Thickness: 0.5 microns Predep 150C; Run: _____ (Yes / No - Do before 1st dep. - do not exceed 6um) Dep. recipe: 150deg\Low-T\Low-T Silicon 550mTorr 500nm Temperature: 150ºC Run #: on the right side Dep. time: 40 (using 12.44 nm/min)) Chiller resist.: _____ Mohm.cm 2 um 150C Timed 1750mtorr Etchback: 6 um (* Insert additional process parameters or details here *)
5	Lithography FS AZ9260 8um with EBR on MA - 200mm Size	System: Multiple Engineer: JF Date completed: 03/08/18	Wafer(s) name: W09 - W18 Side to be processed: FS (* Insert additional process parameters or details here *)
5.1	Vapor Prime	System: Vapor Prime Oven (LIMS-ID 00000915) Engineer: JF Date completed: 03/08/18	Program: #4 HMDS oven temp: 150ºC (* Insert additional process parameters or details here *)
5.2	Spin Coating + EBR	System: E-beam Resist Track (LIMS-ID 00000014) Engineer: JF Date completed: 03/08/18	Wafer(s) name: W09 - W18 Side to be processed: FS Material to spin coat: Resist Thickness: 8 microns Recipe: 1005-Coat AZ9260 8-inch 3000 NOEBR Media: AZ9260 EBR Recipe: 6002-AZ9260 EBR 3mm EE 8-inch EBR Distance: 3mm Recipe steps: Coating / EBR (* Insert additional process parameters or details here *)

5.3	Exposure	System: Karl Suss MA6BA6 (LIMS-ID 00000012) Engineer: JF Date completed: 03/08/18	Wafer(s) name: W09 - W18 Side to be processed: FS Material to expose: Resist Exposed material: ResistExp Mask: INL_MEMS078_Folded3D_V03_L01C DWL polarity: Clear Alignment: First layer (first layer / alignment to previous mask / other) Exposure dose: 1763.2 mJ/cm^2 Light intensity: 34.50 mW/cm^2 Light intensity non-uniformity: _____% Total exposure time: 51.1s (dose/intensity) Multiple exposure: No Alignment gap: 25um Exposure type: **Type A - Hard Contact (HC wait of 15s)** WEC type: Cont WEC Offset: OFF Filter: none (Broadband) (* Insert additional process parameters or details here *)
5.4	Development	System: Karl Suss Optical Track (LIMS-ID 00000909) Engineer: JF Date completed: 03/08/18	Wafer(s) name: W09 - W18 Material to be removed: ResistExp Recipe: **2 x** 0014-120s Develop AZ400K 8-inch Media: AZ400K Time: **2 x** 120s Additional Time: no sec Recipe steps: Puddle development / DI H20 rinse (* Insert additional process parameters or details here *)
5.5	Optical Inspection	System: Optical Microscope Nikon Eclipse L200N (LIMS-ID 00000911 or 00000912) Engineer: JF Date completed: 03/08/18	Wafer(s) name: W09 - W18 (All wafers / every 2nd wafer / other) Magnification: user choice (x1 / x2 / x5 / x10 / x20 / x50 / x100 / other) Inspection sites: user choice (C L R N ON / map / other) Monitor alignment: _____ (Yes / No) (* Insert additional process parameters or details here *)

6	SPTS Pegasus - Deep Silicon Etcher	System: SPTS Pegasus (LIMS-ID 00000021) Engineer: JF Date completed: 03/08/18	Wafer(s) name: W09 - W18 Side to be processed: FS Material(s) to etch: {Si} Thickness to etch: 0.5 microns 1 min TDESC Clean: Yes (Yes/No) Etch recipe: INL Small Bite\PEG10 Run #: on the side (hh:mm S00####) Substrate: Wafer (No wafer / only wafer / handle / other) Target material / etch depth: Si / 0.5 um Mask layer / thickness: AZ9260 / 8um Etch stop layer / thickness: Cu Overetch: _____ Etch time: 180 s Backside leak up rate: 30 mTorr/min (* Insert additional process parameters or details here *)
7	Nickel Electroplating	System: MEMS Ni Electoplating (LIMS-ID 00000XXX) Engineer: JF Date completed: 03/08/18	Wafer(s) name: W09 - W18 Exposed seed layer area, cm^2: _____ Current density, mA/cm^2: 2.5 Estimated plating rate, um/h: 1,1475 Target thickness, um: 0,5 Electrolyte flow, l/min: **pump deactivated** Electrolyte temperature, ºC: RT Wafer rotation speed, %: not appliable Current, A: 0,019 Plating time: 1569 sec (32 min) Total plating time, sec (* Insert additional process parameters or details here *)
7.1	Mechanical Profilometer Measurement	System: KLA Tencor P-16+ (LIMS-ID 00000873) Engineer: JF Date completed: 03/08/18	Wafer(s) name: W09 - W18 Side to be characterized: _____ (FS / BS) Location points: C L R N ON Feature to measure: _____ (trench / mesa / other) Conditions: _____ Note: Values should be measured after removing photoresist with acetone This values should be the difference between amourphous Si and plated Ni (perfect result would be zero) (* Insert additional process parameters or details here *)
8	Sputter Deposit Ta/Cu	System: Kenosystec (LIMS-ID 00000002) Engineer: JF Machine time [hrs]: _____ Engineer time [hrs]: _____ Date completed: 07/08/18	Wafer(s) name: W09 - W18 Material to deposit: Ta / Cu Target thickness: 10nm / 200nm Recipe: C04 - Ta_250mA_20sccm Recipe2: C09 - Cu_250mA_20sccm Ar flow: 20 sccm Current: 250 mA Wafer rotation speed: 28 rpm Time: 126 sec / 2857 sec

9	Lithography FS AZ9260 40um with EBR on MA - 200mm Size	System: Multiple Engineer: JF Date completed: 07/08/18	Wafer(s) name: W09 - W18 Side to be processed: FS (* Insert additional process parameters or details here *)
9.1	Vapor Prime	System: Vapor Prime Oven (LIMS-ID 00000915) Engineer: JF Date completed: 07/08/18	Program: #4 HMDS oven temp: 150ºC (* Insert additional process parameters or details here *)
9.2	Spin Coating + EBR	System: E-beam Resist Track (LIMS-ID 00000014) Engineer: JF Date completed: 07/08/18	Wafer(s) name: W09 - W18 Side to be processed: FS Material to spin coat: Resist Thickness: 40 microns Recipe: 1013-Coat AZ9260 8-inch 1000_40u 1st / 1014-Coat AZ9260 8-inch 1000_40u 2nd Media: AZ9260 EBR Recipe: 6002-AZ9260 EBR 3mm EE 8-inch EBR Distance: 3mm Recipe steps: Coating / EBR **Wait time after coating: 45 min** (* Insert additional process parameters or details here *)
9.3	Exposure	System: Karl Suss MA6BA6 (LIMS-ID 00000012) Engineer: JF Date completed: 07/08/18	Wafer(s) name: W09 - W18 Side to be processed: FS Material to expose: Resist Exposed material: ResistExp Mask: INL_MEMS078_Folded3D_V03_L02C DWL polarity: Clear Alignment: First layer (first layer / alignment to previous mask / other) Exposure dose: 3762 mJ/cm^2 Light intensity: 34.50 mW/cm^2 Light intensity non-uniformity: _____% Total exposure time: 109 s (dose/intensity) Multiple exposure: Yes; 5x Step exposure time: 21.8 s (wait time: 10s) Alignment gap: 25um Exposure type: **Type A - Hard Contact (HC wait of 15s)** WEC type: Cont WEC Offset: OFF Filter: none (Broadband) **Wait time after exposure: 1h15min** (* Insert additional process parameters or details here *)

9.4	Development	System: Karl Suss Optical Track (LIMS-ID 00000909) Engineer: JF Date completed: 07/08/2018	Wafer(s) name: W09 - W18 Material to be removed: ResistExp Recipe: 2 **x** 0024 - 2x 120s Develop AZ400K 8-inch + 1001 30s Develop AZ400K 8-inch Media: AZ400K Time: 4 **x** 120s + 30s Additional Time: no sec Recipe steps: Puddle development / DI H20 rinse (* Insert additional process parameters or details here *)
9.5	Optical Inspection	System: Optical Microscope Nikon Eclipse L200N (LIMS-ID 00000911 or 00000912) Engineer: JF Date completed: 07/08/2018	Wafer(s) name: W09 - W18 All wafers / every 2nd wafer / other) Magnification: user choice (x1 / x2 / x5 / x10 / x20 / x50 / x100 / other) Inspection sites: user choice (C L R N ON / map / other) Monitor alignment: _____ (Yes / No) (* Insert additional process parameters or details here *)
10	SPTS Pegasus - Deep Silicon Etcher	System: SPTS Pegasus (LIMS-ID 00000021) Engineer: JF Date completed: 08/08/18	Wafer(s) name: W09 - W18 Side to be processed: FS Material(s) to etch: AZ9260 resist flakes 1 min TDESC Clean: Yes (Yes/No) Etch recipe: INL O2 Strip Run #: _____ (hh:mm S00####) Substrate: Wafer (No wafer / only wafer / handle / other) Mask layer / thickness: AZ9260 / 40um Etch stop layer / thickness: Cu Overetch: _____ Etch time: 15s Backside leak up rate: 36.8 mTorr/min (* Insert additional process parameters or details here *)
11	Nickel Electroplating	System: MEMS Ni Electoplating (LIMS-ID 00000XXX) Engineer: JF Date completed: 08/08/18	Wafer(s) name: W09 - W18 Exposed seed layer area, cm^2: _____ Current density, mA/cm^2: 20 Estimated plating rate, um/h: 4,59 Target thickness, um: 10 Electrolyte flow, l/min: pump activated at 9V Electrolyte temperature, ºC: RT Wafer rotation speed, %: not appliable Current, A: 0,040 Plating time: 93 min Total plating time, sec (* Insert additional process parameters or details here *)

11.1	Mechanical Profilometer Measurement	System: KLA Tencor P-16+ (LIMS-ID 00000873) Engineer: JF Date completed: 08/08/18	Wafer(s) name: W09 - W18 Side to be characterized: FS (FS / BS) Location points: all (C L R N ON / map / other) Feature to measure: anchored antenna and released antenna (trench / mesa / other) Conditions: _____ Note: Values should be measured after removing photoresist with acetone This values should 10um of Ni (* Insert additional process parameters or details here *)
12	Lithography FS AZ9260 40um with EBR on MA - 200mm Size	System: Multiple Responsible engineer: JF Date completed: 09/08/2018	Wafer(s) name: W09 - W18 Side to be processed: FS (* Insert additional process parameters or details here *)
12.1	Vapor Prime	System: Vapor Prime Oven (LIMS-ID 00000915) Engineer: JF Date completed: 09/08/18	Program: #4 HMDS oven temp: 150ºC (* Insert additional process parameters or details here *)
12.2	Spin Coating + EBR	System: E-beam Resist Track (LIMS-ID 00000014) Engineer: JF Date completed: 09/08/18	Wafer(s) name: W09 - W18 Side to be processed: FS Material to spin coat: Resist Thickness: 40 microns Recipe: 1013-Coat AZ9260 8-inch 1000_40u 1st / 1014-Coat AZ9260 8-inch 1000_40u 2nd Media: AZ9260 EBR Recipe: 6002-AZ9260 EBR 3mm EE 8-inch EBR Distance: 3mm Recipe steps: Coating / EBR Wait time after coating 45min (* Insert additional process parameters or details here *)

12.3	Exposure	System: Karl Suss MA6BA6 (LIMS-ID 00000012) Engineer: JF Date completed: 09/08/18	Wafer(s) name: W09 - W18 Side to be processed: FS Material to expose: Resist Exposed material: ResistExp Mask: INL_MEMS078_Folded3D_V03_L03C DWL polarity: Clear Alignment: First layer (first layer / alignment to previous mask / other) Exposure dose: 3762 mJ/cm^2 Light intensity: 33.63 mW/cm^2 Light intensity non-uniformity: _____% Total exposure time: 111.86 s (dose/intensity) Multiple exposure: Yes Step exposure time: 22.37 s Alignment gap: 25um Exposure type: **Type A - Hard Contact (HC wait of 15s)** WEC type: Cont WEC Offset: OFF Filter: none (Broadband) Wait time after exposure: 1h15min (* Insert additional process parameters or details here *)
12.4	Development	System: Karl Suss Optical Track (LIMS-ID 00000909) Engineer: JF Date completed: 09/08/18	Wafer(s) name: W09 - W18 Material to be removed: ResistExp Recipe: **3 x** 0014-120s Develop AZ400K 8-inch Media: AZ400K Time: **3 x** 120s Additional Time: no sec Recipe steps: Puddle development / DI H20 rinse (* Insert additional process parameters or details here *)
12.5	Optical Inspection	System: Optical Microscope Nikon Eclipse L200N (LIMS-ID 00000911 or 00000912) Engineer: JF Date completed: 09/08/18	Wafer(s) name: W09 - W18 (All wafers / every 2nd wafer / other) Magnification: user choice (x1 / x2 / x5 / x10 / x20 / x50 / x100 / other) Inspection sites: user choice (C L R N ON / map / other) Monitor alignment: _____ (Yes / No) (* Insert additional process parameters or details here *)

13	SPTS Pegasus - Deep Silicon Etcher	System: SPTS Pegasus (LIMS-ID 00000021) Engineer: JF Date completed: 10/08/18	Wafer(s) name: W09 - W18 Side to be processed: FS Material(s) to etch: AZ9260 resist flakes 1 min TDESC Clean: Yes (Yes/No) Etch recipe: INL O2 Strip Run #: S014569 (hh:mm S00####) Substrate: Wafer (No wafer / only wafer / handle / other) Mask layer / thickness: AZ9260 / 40um Etch stop layer / thickness: Cu Overetch: _____ Etch time: 15s Backside leak up rate: _____ mTorr/min (* Insert additional process parameters or details here *)
14	DAD 3350 Dicing Saw	System: Automatic Dicing Saw (LIMS-ID 00000036) Engineer: JF Date completed: 10/08/18	Wafer(s) name: W09 - W18 Recipe: JoseF\001 Die witdh: 30 mm Die height: 30 mm Nr of cuts X: Automatic (to fit 200 mm) Nr of cuts Y: Automatic (to fit 200 mm) Post dicing curing: 200s
15	Sn Electroplating	System: MEMS Sn Electoplating (LIMS-ID 00000XXX) Engineer: JF Date completed: 10/08/18 - 15/08/2018	Wafer(s) name: W09 - W18 Exposed seed layer area, cm^2: 1,1 Current density, mA/cm^2: 27,265 Estimated plating rate, um/h: 20 Target thickness, um: 30 Electrolyte flow, l/min: without pump Electrolyte temperature, ºC: RT Wafer rotation speed, %: not appliable Current, A: 0,0025 Plating time: 90 Total plating time, sec: _____ (* Insert additional process parameters or details here *)
15.1	Mechanical Profilometer Measurement	System: KLA Tencor P-16+ (LIMS-ID 00000873) Engineer: JF Date completed:10/08/18 - 15/08/2018	Wafer(s) name: W09 - W18 Side to be characterized: FS Location points: C L R N ON Feature to measure: _____ (trench / mesa / other) Conditions: _____ Note: Values should be measured after removing photoresist with acetone This values should be 40um (* Insert additional process parameters or details here *)

16	Copper Wet Etch	System: Wet Bench 2 for Lift-Off Processes (LIMS-ID 00000899) Engineer: JF Date completed:10/08/18 - 15/08/2018	Wafer(s) name: W09 - W18 Side to be processed: FS Layer to be Etch: Cu Thickness: 200nm Undercut Etch: 15 um Etchant: 49-1 Copper Etchant Temp: 55C Time/Temp/US in etchant 2: 3 min / mild US (0.8A) Time/Temp in DI H20 + dry: Rinse + 10 min / RT + N2 blow dry **(Do not use IPA for cleaning)**
17	XeF2 Isotropic Si etcher	System: SPTS Pegasus (LIMS-ID 00000021) Engineer: JF Date completed:10/08/18 - 15/08/2018	Wafer(s) name: W09 - W18 Side to be processed: FS Material(s) to etch: Ta + Si Etch recipe: 100c030s050x000n Thickness to be etched: 10 nm + 500 nm Number of cycles: 50 Etch time per cycle: 30 s XeF2 pressure, Torr: 5 N2 pressure, Torr: 0 Undercut Etch: 15 um Etch stop layer / thickness: Cu XeF2 consumed, g: 1.56 XeF2 remaining after process, g: 935.5 (* Insert additional process parameters or details here *)
18	Copper Wet Etch	System: Wet Bench 2 for Lift-Off Processes (LIMS-ID 00000899) Engineer: JF Date completed:10/08/18 - 15/08/2018	Wafer(s) name: Wafer(s) name: W09 - W18 Side to be processed: FS Layer to be Etch: Cu Thickness: 200nm Undercut Etch: 15 um Etchant: 49-1 Copper Etchant Temp: 55C Time/Temp/US in etchant 2: 2 min / RT / no US Time/Temp in DI H20 + dry: Rinse + 10 min / RT + N2 blow dry **(Do not use IPA for cleaning)** **(Do not use Ultrasounds)**

19	Folding Step	System: Wet Bench 5 (LIMS-ID 00000XXXX) Engineer: JF Date completed:10/08/18 - 15/08/2018	Wafer(s) name: Wafer(s) name: W09 - W18 Side to be processed: FS Chemicals: Solder Flux 10mL / Benzyl Ether 100mL Step 1: - Heat to 100C - Wait 5 min Step 2: - Heat to 200C - Wait 5 min Step 3: - Heat to 260C - Wait till folding occurs Time in IPA: 2 min Time in DI H20: 2 min Blow very gently with N2 **(Do not use IPA for cleaning)** **(Do not use Ultrasounds)**
20	End of Run	Responsible engineer: JF Date completed: 16/08/2018	(* Use this area to insert process remarks *)