On-Chip, Efficient and Small Antenna Array for Millimeter-Wave Applications

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***Abstract*— The high path losses experienced by wireless applications at millimeter wavelengths may be mitigated using high gain antennas. The intrinsic small wavelengths makes very attractive to develop solutions with on-chip integrated antennas. However, due to silicon high losses, on-chip antenna elements on RFCMOS technology have reduced efficiency. This paper proposes a solution to obtain an on-chip integrated antenna array based on 3D efficient antenna elements. A 4 element antenna was designed to operate at 57.5 GHz central frequency, with maximum gain of 5.8 dB, and maximum expected efficiency of 45%.**

Keywords—integrated antenna, on-chip antenna, antenna array, 60 GHz.

I. INTRODUCTION

It is expected that systems using millimeter-wave bands will offer new possibilities for systems requiring the use of radio links [1]. The millimeter-wave systems offer new solutions: from wireless sensors to short-range high-speed mobile data rate. However, such systems are complex to design and price reduction will depend on the ability to increase the integration level, desirably using RFCMOS technologies [2]. One element requiring integration is the antenna, preferably an antenna array. Many solutions have been proposed (e.g., [3-9]) for antenna integration, but they are either complex to design, or non-CMOS compatible, or both.

One way towards design complexity and price reduction is system integration using CMOS technology, where the antenna may be considered for on-chip placement due to its intrinsic small size. One challenge when considering on-chip integration is to obtain good antenna efficiency [9]. The solution to increase the antenna efficiency is to rely on new integration approaches. The use of self-folding technology to obtain 3D on-chip structures allows the fabrication of on-chip 3D antennas [10].

In this paper we propose and analyse the expected performance for an antenna array fabricated with an innovative integration methodology, that allows the design of on-chip array antennas on RFCMOS compatible technology.

II. SYSTEM DESIGN

The main concept is based on the use of a 3D element [10], allowing an antenna that is floating on top of the substrate.

A. Integration Methodology

Fig. 1 shows the proposed antenna integration concept. The four antenna elements are obtained using 3D self-folding methodology [11].

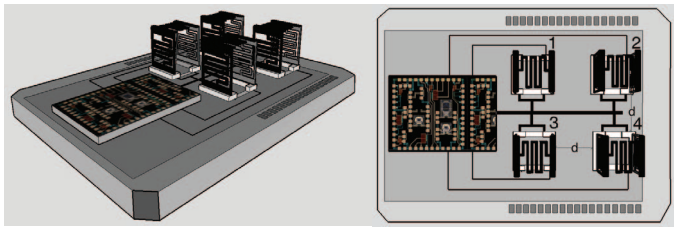


Fig. 1. Proposed solution to obtain an on-chip antenna array (artistic view).

After obtaining the antenna array on top of a silicon wafer, the integration with the remaining system my be obtained using wafer level chip scale packaging methodologies, multi-chip methodologies, or by using a post-processing module applied to the RFCMOS wafer.

B. Antenna Element

Fig. 2 shows the HFSS antenna model. It shows the four-antenna element, with a close-up to one single antenna. The antennas are placed on top of a silicon wafer, with electrical permitivitty, $\varepsilon_r = 4.25$, and loss tangent, $\tan\delta = 0.15$ [12].

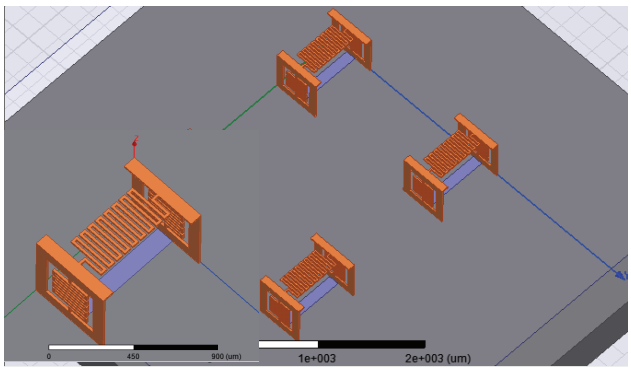


Fig. 2. Ansys HFSS model single antenna element and antenna array.

It was assumed that the wafer bottom was grounded and no isolation layer, like SiO_2 was placed on top of the wafer, between antennas and silicon wafer.

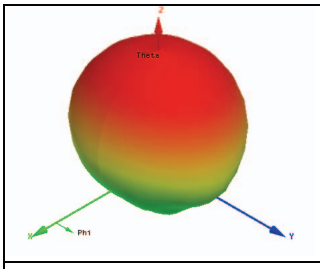
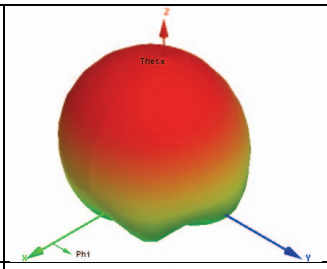
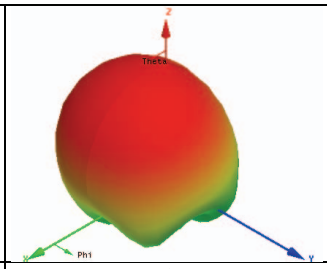
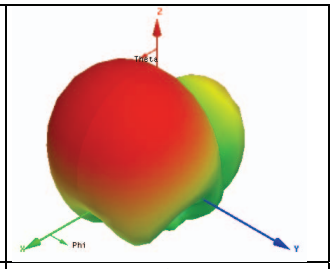
III. RESULTS AND DISCUSSION

Fig. 3 shows the antenna operating central frequency and bandwidth.

A. Antenna Properties

Using the antenna array model from Fig. 2, the results shown in table 1 were obtained for a distance between

TABLE I. SIMULATED RADIATION PATTERN CONTROL USING DIFFERENT PHASE SHIFT FOR THE DIFFERENT ANTENNA ARRAY ELEMENTS.

			
D_{max} = 5.8 dB, η = 45% ϕ_1=0; ϕ_2=0; ϕ_3=0; ϕ_4=0	D_{max} = 5.7 dB, η = 42% ϕ_1=45; ϕ_2=45; ϕ_3=0; ϕ_4=0	D_{max} = 5 dB, η = 34% ϕ_1=90; ϕ_2=90; ϕ_3=0; ϕ_4=0	D_{max} = 4.3 dB, η = 28% ϕ_1=120; ϕ_2=120; ϕ_3=0; ϕ_4=0

antennas of d = 1.15 mm Since we have four antennas, the radiation pattern may be controlled using the phase shifts.

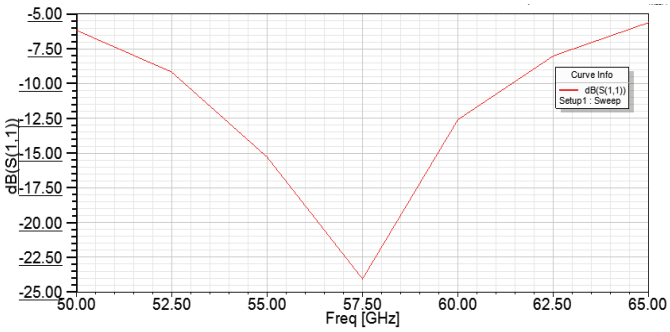


Fig. 3. Ansys HFSS computed S11 array operating characteristics.

From table 1, we can see that the maximum efficiency was η = 45% and max gain was G = 5.8 dB. The gain and efficiency changes as we change the radiation pattern. The values shown in table 1 may not seem very high, but when compared with values from [9], we may conclude that this new approach is very competitive, since it gives almost the same values without the need of extra room required by the artificial materials. Moreover, this new approach does not require any complex antenna design methodology.

B. Measurement Setup

To test the proposed antenna integration methodology, the setup shown in Fig. 4 was implemented.

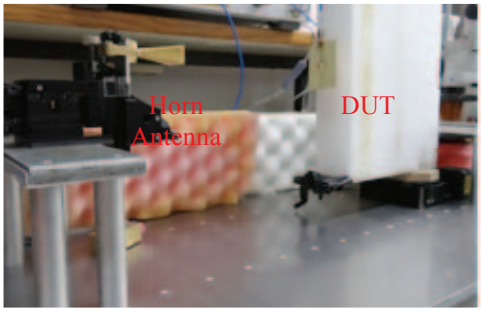


Fig. 4. Measurement setup to characterize the on-chip antenna array.

The left transmitting side is comprised by a signal generator, a frequency multiplier (minicircuits ZX90-2-24+), followed by the HXI frequency multiplier (HAFMV4-187), and a horn antenna (Q-par QSH-SL-50-75-V-20). The right receiving side (DUT) is comprised by the silicon chip with the 3D antennas mounted on it.

IV. CONCLUSIONS

In this work we propose the integration of 3D antennas on top of a silicon wafer. A solution was proposed towards the development of fully integrated RFCMOS transceivers at millimetre-wave band, with improved efficiency.

ACKNOWLEDGMENT

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