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Control Algorithms Based on the Active and Non-Active Currents for a UPQC without Series Transformers

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***Abstract*—This work presents control algorithms for a new Unified Power Quality Conditioner (UPQC) without the series transformers that are frequently used to make the insertion of the series converter of the UPQC between the power supply and the load. The behavior of the proposed UPQC is evaluated in presence of voltage imbalances, as well as under non-sinusoidal voltage-and current conditions. The presented algorithms derive from the concepts involving the active and non-active currents, together with a PLL circuit. Based on these real-time algorithms, and considering the proposed hardware topology, the UPQC is able to compensate the harmonic components of the voltages and currents, correct the power factor, and keep the load voltages regulated, all of this in a dynamic way, responding instantaneously to changes in the loads or in the electrical power system. The control algorithms were distributed in a two-DSP digital control architecture, without any communication between them. Consequently, can be increased the sampling frequency of the acquired voltages and currents and improve the UPQC performance. Furthermore, some constraints of the proposed UPQC are evidenced, particularly when the main voltages are imbalanced. Simulation and experimental results are presented to verify the UPQC performance under transient and steady state conditions.**

***Index Terms*— Power System Harmonics, Power Electronics, Real-Time Systems, Active Filters.**

I. INTRODUCTION

The Unified Power Quality Conditioner (UPQC) is a custom power device that combines a series and a shunt power conditioners in a single equipment [1]-[9], capable to compensate most of the power quality problems in distribution grids.

Conventionally, as indicated in Fig. 1a, series conditioners are connected to the power grid through power transformers. To provide active filtering, the series conditioners produce harmonic voltages at the power transformers, resulting in an increment of the power losses, audible noise, overheating, and undesirable voltage drops in internal elements. Consequently, these power transformers need to be oversized. To overcome this drawback, a UPQC topology without series transformers, as shown in Fig. 1b, is more suitable. This topology is similar to those introduced in [9][10][11]. It leads to some advantages as, for example, the elimination of the transformers to connect the series converter to the grid and the possibility to employ more simple switching techniques based on the PWM unipolar switching mode. On the other hand, with the hardware topology based on three single-phase back-to-back converters, it is not possible to provide an energy exchange among the phase circuits and, as a consequence, it is not more possible to compensate imbalanced current or even to keep them balanced when the series conditioner compensates imbalanced voltages.

Another issue corresponds to the employed control algorithms. Essentially, most of the control methods for active power conditioners are based on instantaneous power theories, once they offer a more robust basis to control power electronics devices, both in steady-state and transient conditions. They are usually defined in α-β-0 reference frame [12]-[14] or in d-q-0 reference frame [4] [15]-[17]. However, to employ this reference frame it is mandatory the use of Clarke or Park transformations, which demands an increment of the computational effort. An alternative to overcome this drawback consists in applying control algorithms based on active and non-active currents [18]-[25], together with a minimization method and a PLL circuit to provide,

accurately, active filtering and voltage regulation [15] [26]-[28]. It is important to note that in most of the papers observed in literature, control algorithms based on the active and non-active currents are evaluated only by simulation results or by experimental results with shunt active or hybrid filters, which are much less complex when compared with a UPQC. In this work, the introduced control strategy was evaluated with a non-conventional UPQC prototype, which presents a complex hardware, with 24 IGBTs.

Summarizing, the approach presented in [19]-[21] is here improved to deal with the hardware topology illustrated in Fig. 1b. Moreover, the proposed algorithms were distributed in a two-DSP architecture, running independently from each other. These aspects, including a mathematical analysis considering a scenario with the UPQC compensating imbalanced voltages, constitute the major contributions of this work. Simulation -and experimental-results were introduced to evaluate the UPQC performance under transient and steady state conditions.

II. Hardware Configuration

The electrical diagram of the developed UPQC is illustrated in Fig. 1b. It consists of three single-phase modules, each one comprehended by two full-bridge converters connected in back-to-back, one of the series conditioner and the other of the shunt conditioner. To command these full-bridge converters, it was employed a PWM unipolar technique with a switching frequency of 8 kHz, such that the produced voltages present three-level resolution, with a resultant switching frequency of 16 kHz. The control algorithms employed to determine the reference voltages that are compared with the triangular carriers are similar to the ones introduced in [20]-[21].

The power transformers employed to connect the shunt conditioners with the power grid are to provide galvanic isolation. Such characteristic cannot be considered as a problem, since these transformers are submitted to voltages that are balanced, regulated and with a very low harmonic distortion. A three-phase diode rectifier composes the load, with a RLC circuit (inductor in series with a parallel RC branch) at its dc-side, and three single-phase transformers (115 V//57.5 V) connect the shunt conditioner to the electrical power grid.

Circuit breakers are applied to connect the UPQC to the power grid or to remove it in case of possible short-circuits or malfunction of the power converters. Together with the use of the circuit breakers there are also other protections that minimize possible damages to the power converters, improving the UPQC reliability. Based on the converter topology, the worst malfunction occurs when IGBTs of the same branch (S_{1k}, S_{3k}, for example) are commanded at the same time. In this case, there is a drive protection that disables this command. If this malfunction occurs with the series conditioner, for example, the circuit breakers CB_{a1}, CB_{b1}, CB_{c1} are closed and, in sequence, CB_{a4}, CB_{b4}, CB_{c4} are opened. Moreover, while the circuit breakers are not driven, the grid currents (i_{Sa}, i_{Sb}, i_{Sc}) flow through the anti-parallel diodes. Another issue related to the UPQC reliability consists on its response when a short circuit occurs, once it is not suitable to compensate short-circuit currents, due to the high currents –

and voltage – levels. In this case, the UPQC is entirely removed from the power grid. It is done by closing CB_{a1}, CB_{b1}, CB_{c1} and opening CB_{a3}, CB_{b3}, CB_{c3}, considering that CB_{a2}, CB_{b2}, CB_{c2} are already open.

Passive filters (RLC circuits) are applied to minimize high-frequency switching harmonics generated by the PWM power converters. For the shunt conditioners, the passive filters are mounted with $L_{P1} = 0.6$ mH, $R_P = 4.7\ \Omega$, $C_P = 4.4\ \mu F$ and $L_{P2} = 0.45$ mH. For the series conditioner, the values are: $L_S = 0.6$ mH, $R_S = 13.2\ \Omega$, and $C_S = 8.8\ \mu F$. In [29] is introduced an approach to design passive filters for grid connected inverters, in [30] is presented a design of passive filters together with active filters, and in [31] is proposed a solution for low switching frequency inverters with limited passive filter bandwidth.

III. UPQC CONTROLLER

The UPQC algorithms that determines, in real-time, the reference voltages and currents produced by the PWM converters are represented by block diagrams in Fig. 2a and Fig. 2b, respectively. A synchronizing circuit PLL (Phase-Locked-Loop) was included in each DSP, since the PLL output signals are employed in the series-and shunt control algorithms. It is worth to mention the infeasibility to embed the entire control system into a single DSP, due to the need of producing 24 PWM signals to drive the IGBTs, and also because of the large number of acquired signals of currents and voltages. However, this constraint resulted in a contribution of this work due to the capability of the shunt –and series – conditioners to be independently commanded from each other, enabling the use of two DSPs running autonomously from each other. It resulted in some advantages as, for example, a decrement of the computational efforts in each DSP, and therefore, the possibility to increase the sampling frequency of the acquired currents and voltages.

A. Active and Non-Active Currents

As introduced in [18] the non-active current corresponds to the current-component that does not produce any active power, although it increases the current amplitude and the losses in the power cables. The non-active current is determined through minimization methods as, for example, the Lagrange multiplier technique [19]. For this formulation, it is assumed that a hypothetical load current i_{Lk}, $k = (a, b, c)$, is comprehended by an active component (i_{Lpk}) plus a non-active component (i_{Lqk}). These current components, with their normalized amplitude, are given by:

$$\hat{i}_{Lk} = \hat{i}_{Lpk} + \hat{i}_{Lqk} \quad . \tag{1}$$

Based on the Lagrange multiplier technique as the minimization method, together with the control signals generated by the PLL, the normalized active-current component can be determined as follows:

$$\begin{pmatrix} \hat{i}_{Lpa} \\ \hat{i}_{Lpb} \\ \hat{i}_{Lpc} \end{pmatrix} = \frac{\overline{p'}}{\sqrt{pll_a^2 + pll_b^2 + pll_c^2}} \cdot \begin{pmatrix} pll_a \\ pll_b \\ pll_c \end{pmatrix} \quad ; \tag{2}$$

where the control signal $\overline{p'}$ is given by:

$$\overline{p'} = \frac{1}{T} \cdot \int_0^T (pll_a \hat{\imath}_{La} + pll_b \hat{\imath}_{Lb} + pll_c \hat{\imath}_{Lc}) dt \quad ; \tag{3}$$

and the generated signals by the PLL circuit correspond to:

$$\begin{aligned} pll_a(\omega t) &= \sin(\omega t) \\ pll_b(\omega t) &= \sin\left(\omega t - (2\pi/3)\right) \\ pll_c(\omega t) &= \sin\left(\omega t + (2\pi/3)\right) \quad . \end{aligned} \tag{4}$$

Note that $\overline{p'}$ corresponds to the normalized value of the average active power drawn by the load, and the square sum of the output PLL signals is constant and equal to 1.5.

B. Voltage–Reference Algorithm

Based on this control algorithm it is expected that the series conditioner be capable to provide active filtering, voltage regulation and system stability. As illustrated in Fig. 2 the normalized reference voltage ($\hat{v}_{ref_{kn}}$), for $k = a, b, c$, is given by:

$$\hat{v}_{ref_{kn}} = pll_k + \hat{v}_{Sqkn} - \hat{v}_{Skn} \quad . \tag{5}$$

Note that the PLL output signals are the reference voltages that should be delivered to the load. Indeed, being all of the input signals (voltages and currents) normalized, such that, a unity amplitude represents their nominal values, a directly comparison involving the PLL output (pll_k) together with the other signals indicated in equation (4) can be done.

The controlled voltage v_{Sqkn} is applied to provide system stability, avoiding possible resonance phenomena between the UPQC passive elements with the system impedance [1]. The goal is to add a virtual series resistance to the non-active components that may arise in the source currents, i_{Sk}, forcing them to flow through the shunt converter, improving the overall UPQC functionality.

The concepts involving the active and non-active currents can be easily applied, considering that the controlled voltages produced by the damping algorithm are proportional to the non-active components of the grid currents, and they are determined as follows:

$$\begin{pmatrix} \hat{\imath}_{Sqa} \\ \hat{\imath}_{Sqb} \\ \hat{\imath}_{Sqc} \end{pmatrix} = \begin{pmatrix} \hat{\imath}_{Sa} \\ \hat{\imath}_{Sb} \\ \hat{\imath}_{Sc} \end{pmatrix} - \begin{pmatrix} \hat{\imath}_{Spa} \\ \hat{\imath}_{Spb} \\ \hat{\imath}_{Spc} \end{pmatrix} \quad ; \tag{6}$$

where,

$$\begin{pmatrix} \hat{\imath}_{Spa} \\ \hat{\imath}_{Spb} \\ \hat{\imath}_{Spc} \end{pmatrix} = \frac{\overline{p'_s}}{1.5} \cdot \begin{pmatrix} pll_a \\ pll_b \\ pll_c \end{pmatrix} \quad ; \tag{7}$$

and,

$$\overline{p'_s} = \frac{1}{T} \cdot \int_0^T (pll_a \hat{\imath}_{San} + pll_b \hat{\imath}_{Sbn} + pll_c \hat{\imath}_{Scn}) dt \quad . \tag{8}$$

Once determined the non-active component from the grid current, it is multiplied by a gain K_S, as indicated in Fig. 2, to

determine v_{Sqkn} (for $k = a, b, c$). A methodology to determine K_S is explained in [1], which is based on a commitment to be large enough to damp to the non-active currents that may arise in the grid currents, without compromising the flow of their fundamental positive-sequence current.

C. Current–Reference Algorithm

This control algorithm determines the non-active component from the load currents, and a controlled current to provide dc-link voltage regulation. The non-active currents are determined from the difference between the load currents from their active components, which one was obtained through equations (2) and (3). The controlled currents labelled in Fig. 2 as i_{dc_a}, i_{dc_b}, i_{dc_c}, are determined through a control algorithm denominated as "dc-link voltage regulator" as indicated as follows:

$$\begin{aligned} i_{\mathrm{dc\_a}}(\omega t) &= I_{dc\_a}\sin(\omega t) \\ i_{dc\_b}(\omega t) &= I_{\mathrm{dc\_b}}\sin\big(\omega t - (2\pi/3)\big) \\ i_{dc\_c}(\omega t) &= I_{\mathrm{dc\_c}}\sin\big(\omega t + (2\pi/3)\big) \quad ; \end{aligned} \tag{9}$$

where,

$$\begin{pmatrix} I_{\mathrm{dc\_a}} \\ I_{\mathrm{dc\_b}} \\ I_{\mathrm{dc\_c}} \end{pmatrix} = \left(k_{p_{dc}} + \frac{k_{i_{dc}}}{S}\right) \cdot \begin{pmatrix} v_{dc_{ref}} - v_{dc_1} \\ v_{dc_{ref}} - v_{dc_2} \\ v_{dc_{ref}} - v_{dc_3} \end{pmatrix} \quad . \tag{10}$$

These PI parameters ($k_{p_{dc}}$, $k_{i_{dc}}$) were tuned through off line simulations, based on a compromise to achieve the fastest transient response with the constraint that the rms values of I_{dc_a}, I_{dc_b}, I_{dc_c} do not exceed 10 A, as explained in section VI. In literature there are other approaches to determine the PI parameters as the ones introduced in [32] [33].

IV. UPQC Constraints Based on the Analyzed Topology

It is usual to consider the UPQC as a dynamic conditioner capable to compensate most of the power quality disturbances, which includes voltage-and current-imbalances. These aspects, considering a conventional topology of UPQC, were deeply discussed in the literature [1], [4]-[8].

However, due to the structure of the developed UPQC, based on three single-phase back-to-back converters, the transfer of energy between the phases is not possible. It leads to some drawbacks as, for example, the grid currents become imbalanced when the series converter compensates imbalanced voltages. Indeed, consider a power grid with the voltages presenting positive- and negative-sequence components, at the fundamental frequency, and the load is balanced and resistive. Furthermore, the IGBT losses were neglected and the high frequency components produced the series –and shunt – converters were not considered, once these aspects were not important in the analysis of this issue. Based on these conditions and constraints, the grid voltages are given by:

$$\begin{aligned} v_{Sa}(\omega t) &= V_1^{+}\sin(\omega t) + V_1^{-}\sin(\omega t) \\ v_{Sb}(\omega t) &= V_1^{+}\sin\big(\omega t - (2\pi/3)\big) + V_1^{-}\sin\big(\omega t + (2\pi/3)\big) \end{aligned} \tag{11}$$

$$v_{Sc}(\omega t) = V_1^{+}\sin\left(\omega t + (2\pi/3)\right) + V_1^{-}\sin\left(\omega t - (2\pi/3)\right) \quad ;$$

where the first term on the right side corresponds to the fundamental positive-sequence component and the second to the fundamental negative-sequence component. Furthermore, based on the electrical scheme illustrated in Fig. 1b, it was established the following equations:

$$\begin{cases} v_{Lk} = v_{Fk} + v_{Sk} \\ i_{Sk} = i_{Fk} + i_{Lk} \end{cases} ; \tag{12}$$

where v_{Lk} corresponds to the load voltage, v_{Sk} to the grid voltage and v_{Fk} to the series-conditioner voltage. Similarly, i_{Lk} corresponds to the load current, i_{Sk} to the grid current and i_{Fk} to the shunt-converter current. Once it is expected that the load voltages are comprised by the fundamental positive sequence of the grid voltages, the series converter produces the following voltages:

$$\begin{aligned} v_{Fa}(\omega t) &= -(V_1^{-})\sin(\omega t) \\ v_{Fb}(\omega t) &= -(V_1^{-})\sin\left(\omega t + (2\pi/3)\right) \\ v_{Fc}(\omega t) &= -(V_1^{-})\sin\left(\omega t - (2\pi/3)\right) \quad . \end{aligned} \tag{13}$$

Therefore, due to the compensation of the imbalanced components by the series converter, the load currents are given by:

$$\begin{aligned} i_{La}(\omega t) &= \frac{(V_1^{+})}{R}\sin(\omega t) \\ i_{Lb}(\omega t) &= \frac{(V_1^{+})}{\mathrm{R}}\sin\left(\omega t - (2\pi/3)\right) \\ i_{Lc}(\omega t) &= \frac{(V_1^{+})}{R}\sin\left(\omega t + (2\pi/3)\right) \quad . \end{aligned} \tag{14}$$

There are also the produced currents by the shunt converter to keep regulated the dc-link voltage. These currents correspond to:

$$\begin{aligned} i_{Fa}(\omega t) &= I_{dc\_a}\sin(\omega t) \\ i_{Fb}(\omega t) &= I_{dc\_b}\sin\left(\omega t - (2\pi/3)\right) \\ i_{Fc}(\omega t) &= I_{dc\_c}\sin\left(\omega t + (2\pi/3)\right) \quad ; \end{aligned} \tag{15}$$

where I_{dc_a}, I_{dc_b}, I_{dc_c} are determined by the respective dc-link voltage controllers.

Note that when the series conditioners produce the controlled voltages described in (13), it results on an active-power demand from each dc-link to the respective ac-side of the series conditioners. Thus, the average active power produced at each series-conditioner terminals (P_{SC_k}, for $k = a, b, c$) is given by:

$$\begin{aligned} P_{SC\_a} &= \frac{1}{2\pi}\int_0^{2\pi}\left[v_{Fa}(\omega t)\cdot\left(i_{La}(\omega t) + i_{Fa}(\omega t)\right)\right]\mathrm{d}(\omega t) = -\frac{(V_1^{-})}{2}\left[\left(\frac{V_1^{+}}{R}\right) + I_{\mathrm{dc\_a}}\right] \\ P_{SC\_b} &= \frac{1}{2\pi}\int_0^{2\pi}\left[v_{Fb}(\omega t)\cdot\left(i_{Lb}(\omega t) + i_{Fb}(\omega t)\right)\right]\mathrm{d}(\omega t) = -\frac{(V_1^{-})}{2}\left[\left(\frac{V_1^{+}}{R}\right) + I_{\mathrm{dc\_b}}\right]\cos(2\pi/3) \end{aligned} \tag{16}$$

$$P_{SC\_c} = \frac{1}{2\pi}\int_0^{2\pi}\left[v_{Fc}(\omega t)\cdot\left(i_{Lc}(\omega t)+i_{Fc}(\omega t)\right)\right]\mathrm{d}(\omega t) = -\frac{(V_1^-)}{2}\left[\left(\frac{V_1^+}{R}\right)+I_{dc\_c}\right]\cos(2\pi/3)$$

The negative signals at the average powers P_{SC_a}, P_{SC_b}, P_{SC_c} indicate an energy flow from the dc-link voltages to the power grid, and because of that, the dc-link voltages decrease. Due to this condition, to keep the dc-link voltages regulated, the shunt conditioners consume an average active power equal to the one produced by the series conditioners. Based on the electrical scheme illustrated in Fig. 1b, the average active power at each shunt-conditioner terminals (P_{PC_k}, for $k = a, b, c$) corresponds to:

$$\begin{aligned}
P_{PC_a} &= \frac{1}{2\pi}\int_0^{2\pi}\left[v_{La}(\omega t)\cdot i_{Fa}(\omega t)\right]\mathrm{d}(\omega t) = -\frac{(V_1^+)}{2}I_{dc_a}\\
P_{PC_b} &= \frac{1}{2\pi}\int_0^{2\pi}\left[v_{Lb}(\omega t)\cdot i_{Fb}(\omega t)\right]\mathrm{d}(\omega t) = -\frac{(V_1^+)}{2}I_{dc_b}\\
P_{PC_c} &= \frac{1}{2\pi}\int_0^{2\pi}\left[v_{Lc}(\omega t)\cdot i_{Fc}(\omega t)\right]\mathrm{d}(\omega t) = -\frac{(V_1^+)}{2}I_{dc_c}
\end{aligned} \tag{17}$$

Based on equations (16) and (17), and since the IGBT losses were neglected, the average active powers at the shunt -and series terminals are equal, and I_{dc_k} were determined as follows:

$$\begin{aligned}
P_{SC_a} = P_{PC_a} &\therefore I_{dc_a} = -\frac{(V_1^+)}{R}\left[\frac{(V_1^-)}{((V_1^+)+(V_1^-))}\right]\\
P_{SC_b} = P_{PC_b} &\therefore I_{dc_b} = -\frac{(V_1^+)}{R}\left[\frac{(V_1^-)\cos(2\pi/3)}{((V_1^+)+(V_1^-)\cos(2\pi/3))}\right]\\
P_{SC_c} = P_{PC_c} &\therefore I_{dc_c} = -\frac{(V_1^+)}{R}\left[\frac{(V_1^-)\cos(2\pi/3)}{((V_1^+)+(V_1^-)\cos(2\pi/3))}\right]
\end{aligned} \tag{18}$$

Based on the results achieved in (18), I_{dc_b} and I_{dc_c} are equal. However, they are different from I_{dc_a}. Thus, it can be verified that when the series conditioners compensate a fundamental negative-sequence voltage, the grid currents become imbalanced.

Another aspect derived from this analysis corresponds to the fact that this proposed UPQC cannot compensate negative- or zero-sequence currents at the fundamental frequency. Indeed, in previous works observed in the literature that deals with a UPQC presenting similar topology [9], the compensated voltages and currents were only comprised by a fundamental positive-sequence component, plus harmonics. To overcome this drawback it would be necessary to have energy sources connected to the dc-link voltages, or modifications on the hardware topology, as proposed in [20], resulting in a UPQC without series transformers with capability to compensate negative –and zero-sequence components in a three-phase four-wire system. Nevertheless, due to the considerable number of power switches, this solution may not be economically feasible nowadays.

V. Simulation Results

A test case presenting different transient events where the UPQC is turned on with the grid voltages and load currents without imbalanced components is introduced. Initially, the series and shunt conditioners are turned off, with the circuit breakers CB_{a1}, CB_{b1}, CB_{c1} bypassing the series conditioner, and all of the other circuit breakers are opened.

The shunt conditioner is the first to be connected, with the circuit breakers CB_{a2}, CB_{b2}, CB_{c2} closed, and the dc-link capacitors

are partially charged. In sequence, CB_{a3}, CB_{b3}, CB_{c3} were closed, and the shunt converter was turned on at $t = 0.25\ s$, as illustrated in Fig. 3a, with a transient increment of the fundamental positive-sequence component of i_{Sa}, once the dc-link voltage is below its reference. At steady state, with the dc-link voltages regulated, the amplitude of i_{Sa} decreases and becomes close to the amplitude of the fundamental positive-sequence component of the load current, i_{La}. In sequence, it was initialized the start-up procedure to connect the series conditioner. All of the upper IGBTs (S_{1k}, S_{2k} for $k = a, b, c$) were turned on, and the circuit breakers CB_{a4}, CB_{b4}, CB_{c4} were closed. In sequence, CB_{a1}, CB_{b1}, CB_{c1} were opened. Finally, as indicated in Fig. 3b, the series conditioner was turned on at $t = 0.35\ s$, and the start-up sequence of the UPQC was complete.

Fig. 3c and Fig. 3d show the first introduced transient event, at $t = 1.0$ s, such that the grid voltages become imbalanced. In this transient the load voltage v_{Lb} presents its magnitude (peak value) decreased from 170 V to 120 V, v_{Lc} presents a small increment, from 170 V to 185 V, and v_{La} remains with the same magnitude. Consequently, to keep the dc-link voltages regulated in each one of the back-to-back power modules, the amplitude of i_{Sc} presents an increment (peak value) from 13 A to 20 A, i_{Sb} decreases from 13 A to 11 A, and i_{Sa} remains with the same magnitude.

Fig. 3e and Fig. 3f show the second introduced transient event, at $t = 1.5$ s, such that the imbalanced components at the main voltages were extinguished. Due to this new condition, the amplitudes of the grid currents were again the same, just as before the first transient event. In all of these transients the load voltages remain balanced, regulated and with a low harmonic distortion (below 2%). Thus, it can be concluded that the compensated voltages were not influenced by the constraints of this topology. On the other hand, during the entire simulation, the compensated currents remain with low harmonic distortion (below 3%) and in phase with the fundamental positive-sequence component of the main voltages.

VI. Experimental Results

The experimental results were obtained from four test cases different from those of the simulation results of section V with the start-up sequence similar as the one described in section V.

The implemented laboratorial prototype was designed to operate with 115 V line voltages and 15 A of compensation currents, to be applied in a 5 kVA three-phase system. An important issue corresponds to the limits of the developed UPQC for compensating voltage sags and swells. Considering equal the active powers at the terminals of the shunt –and series-converters, as indicated in equation (18), the rms value of the current applied to keep the dc-link voltage regulated I_{dc_k} ($k = a, b, c$) is given by:

$$P_{SC\_k} = P_{PC\_k} \ \therefore \ I_{dc\_k} = \frac{V_{F\_k} \cdot I_{S1\_k}}{V_{L\_k}} \ ; \tag{19}$$

where V_{L_k} corresponds to the load voltage at the shunt converter side, indicated in Fig.1b as V_{1P}; I_{S1_K} is the fundamental positive-sequence component of the grid current; and V_{F_k} the rms value of the series converter voltage. Considering that more than 90%

of the registered sags presented a voltage drop inferior to 40% of the nominal voltage [35], the compensation capability of the equipment was limited to that value. Considering the imposed limit of 46 V (40% of 115 V) to V_{F_k}, with the rms values of V_{L_k} and I_{S1_K} equal to 115 V and 24.15 A (maximum grid current in a 115 V-5 kVA with the grid voltage presenting a 40% sag), respectively, it results in a I_{dc_k} equal to 9.66 A. To accommodate the UPQC operation losses, it was assumed a maximum value of I_{dc_k} equal to 10 A.

A. Test-Case 1

In this test case the load voltages are balanced with a harmonic distortion of 5% and with a voltage sag of 20%, considering a 115 V nominal voltage. The load corresponds to a three-phase diode rectifier, with currents that presents a total harmonic distortion (THD) of 29.2%. In Fig. 4a are illustrated the load voltages and grid currents with shunt and series conditioners of the UPQC turned off. In this condition, the power factor is equal to 0.9.

Fig. 4b illustrates the grid currents and the load voltages at the transient when the series conditioner is turned on. In less than one cycle period the load voltages increase to their rated value, and as consequence, the grid currents also increase due to the addition of an average active power drawn by the shunt converters to regulate the dc-link voltages.

In sequence, Fig. 4c shows the grid currents and the load voltages with the UPQC under steady-state condition. In this scenario, the load voltages present their amplitudes increased to the rated value, and the harmonic voltage distortion was reduced from 5.0% to 2.2%. Furthermore, the grid currents remain balanced and the THD decreased from 29.2% to 5.5%. It can also be noted an increment of the grid currents amplitudes, due to the active current of the shunt conditioners, which is necessary to regulate the dc-link voltages. TABLE I summarize the UPQC behavior, presenting the rms values of the main and load voltages and currents, as well as the THD values, with the UPQC turned on under steady-state condition.

TABLE I - UPQC PERFORMANCE – TEST CASE1 WITH UPQC TURNED ON (RMS VALUES OF VOLTAGES AND CURRENTS)

Grid Voltages	Grid Currents	Load Voltages	Load Currents
V_{Sa} = 93.3 V	I_{Sa} = 14.9 A	V_{La} = 115.5 V	I_{La} = 11.5 A
V_{Sb} = 93.0 V	I_{Sb} = 14.8 A	V_{Lb} = 115.2 V	I_{Lb} = 11.5 A
V_{Sc} = 93.2 V	I_{Sc} = 14.9 A	V_{Lc} = 115.6 V	I_{Lc} = 11.5 A
THD = 5.0%	**THD = 5.5%**	**THD = 2.2%**	**THD = 29.2%**

B. *Test-Case* 2

In this test case the load voltages (v_{La}, v_{Lb}, v_{Lc}) are imbalanced with a THD of 5%. Fig. 5a illustrates the load voltages and grid currents with the UPQC conditioners turned off. In this condition, the grid currents are also imbalanced with a THD of 29.2% and lightly delayed from the load voltages, once the power factor is equal to 0.92 inductive.

Fig. 5b illustrates the grid currents and the load voltages at the transient when the series conditioner is turned on. Again, as occurred in ***test case* 1**, in less than one cycle period the load voltages become balanced, regulated and with low harmonic distortion. On the other hand, the grid currents remain imbalanced, with different amplitudes from the ones before this transient,

due to action of the dc-link voltage controller. However, it is important to point out that the UPQC remains stable at the entire test case, with the load voltages correctly compensated.

In Fig. 5c are illustrated the load voltages and grid currents with all of the UPQC conditioners turned on under steady state condition. In this condition, as expected, the load voltages are balanced and their THD decreased from 5.0% to 2.2%. Moreover, the grid currents also present a harmonic distortion reduction from 29.2% to 5.5%. However, they remain imbalanced due to the compensation of the imbalanced voltages by the series conditioner. TABLE II summarizes the UPQC behavior in this test case, presenting the rms values of the load and grid voltages and currents, as well as the THD values, with the UPQC turned on under steady state condition. As expected, the UPQC series conditioner compensated the harmonic -and imbalanced-components, with the grid currents remaining imbalanced. Moreover, it can also be noted that i_{Sa} and i_{Sc} present lower amplitudes in comparison with i_{Sb}. It occurs because the load voltages v_{La} and v_{Lc}, with all of the UPQC conditioners turned off, present lower amplitudes in comparison with v_{Lb}. Furthermore, in this test case, the rms value of the fundamental negative-sequence component reduces from 3.7 V to 0.2 V, which means that 94.5% of this imbalanced voltage was compensated.

TABLE II - UPQC PERFORMANCE – TEST CASE 2 WITH UPQC TURNED ON (RMS VALUES OF VOLTAGES AND CURRENTS)

Grid Voltages	Grid Currents	Load Voltages	Load Currents
V_{Sa} = 103.9 V	I_{Sa} = 13.4 A	V_{La} = 115.2 V	I_{La} = 11.5 A
V_{Sb} = 116.2 V	I_{Sb} = 12.0 A	V_{Lb} = 115.5 V	I_{Lb} = 11.5 A
V_{Sc} = 106.7 V	I_{Sc} = 12.9 A	V_{Lc} = 115.0 V	I_{Lc} = 11.5 A
THD = 5.0%	**THD = 5.5%**	**THD = 2.2%**	**THD = 29.2%**

C. Test Case 3

A third test case was performed to determine the UPQC power losses. In this test, the active power consumed by the UPQC is to suppress their losses only, once the load currents are balanced and, furthermore, the main voltages are balanced and regulated. Based on the experimental results illustrated at Fig. 6a and Fig. 6b, the active power consumed by the load corresponds to 3.65 kW. With the UPQC turned on, and operating at steady state (Fig. 6c and Fig. 6d), the active power increases to 3.87 kW. Thus, the active power consumed by the UPQC corresponds to 5.68% of the overall active power provided by the power grid, resulting in efficiency equal to 94.32%. However, it is important to highlight that this is the value of efficiency for a particular case, which will vary according to the operating conditions of the UPQC.

D. Test Case 4

In the case it was verified the robustness of the UPQC control algorithms considering two step-change tests. Initially both conditioners are turned off and the dc-link voltages were pre-charged to 81 V, approximately, as indicated by $\boldsymbol{v_{dc\_1}}$ in Fig.7a. In sequence, the shunt conditioner is turned on and the dc-link voltages go up to their rated value of 150 V. At this time transient, the shunt conditioner has drawn a controlled current, with its amplitude limited to 20 A, to provide an energy exchange from the AC side to the DC side of the power converters. Furthermore, as illustrated in Fig.7a, it was taken almost 400 ms to the $\boldsymbol{v_{dc\_1}}$

reach its new steady-state condition. In sequence, with both conditioners turned on at steady-state condition, the nonlinear load is connected with the power grid. According to the corresponding experimental result Fig.7b, when this transient occurs v_{dc_1} go down to 140 V and it took almost 350 ms to reach its rated value. Based on these step-change tests it can be note an adequate performance of the UPQC reaching different steady-state conditions without losing its stability.

VII. Conclusions and Suggestions for Further Works

This paper introduced a UPQC without series transformers, controlled by algorithms based on the active and non-active currents together with PLL circuits. The simulation –and experimental – results confirmed the good performance of the UPQC controlled by the introduced algorithms, compensating almost all of the power quality problems. Furthermore the power quality indices of the compensated voltages and currents are in accordance with the IEEE Standard 519-2014 [34]. Thus, the proposed control algorithms are promising, effective and they can be applied not only to custom power conditioners, but also to control any power converter connected to the electrical grid for different purposes as, for example, FACTS devices.

Considering the topology of the developed UPQC, despite of its advantages described in section I, it does not have the capability to compensate imbalanced currents or even to keep the grid currents balanced when the series conditioner compensates imbalanced voltages. As it was explained in section IV, and highlighted through simulation -and experimental-results, the active power in each single-phase series converter presents different average values when the series conditioner compensates imbalanced voltage-components. Therefore, the active currents produced by the shunt conditioners present different amplitudes from each other. It must be referred that in this situation, usually the negative sequence components have amplitudes lower than the positive sequence components, so the unbalances in this situation are negligible. Also, once most of the power quality problems involving the load voltages are related to voltage sags or swells, this UPQC topology is still feasible and capable of improving the power quality indices of an industry.

Another important aspect of this work consists on the control system architecture of the developed UPQC laboratorial prototype, which is based in 2 DSPs, where the control algorithms of the shunt and series compensator are distributed, with the DSPs running independently from each other, without any communication between them. This proposed control architecture could be easily applied to UPQCs with different topologies. For example, a UPQC connected to a medium-voltage system would probably present multilevel power conditioners, and in this case it could be applied this control system architecture of 2 DSPs to determine the reference voltages and currents, together with CPLDs (Complex Programmable Logic Device) to generate the PWM signals to drive the IGBTs.

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FIGURES

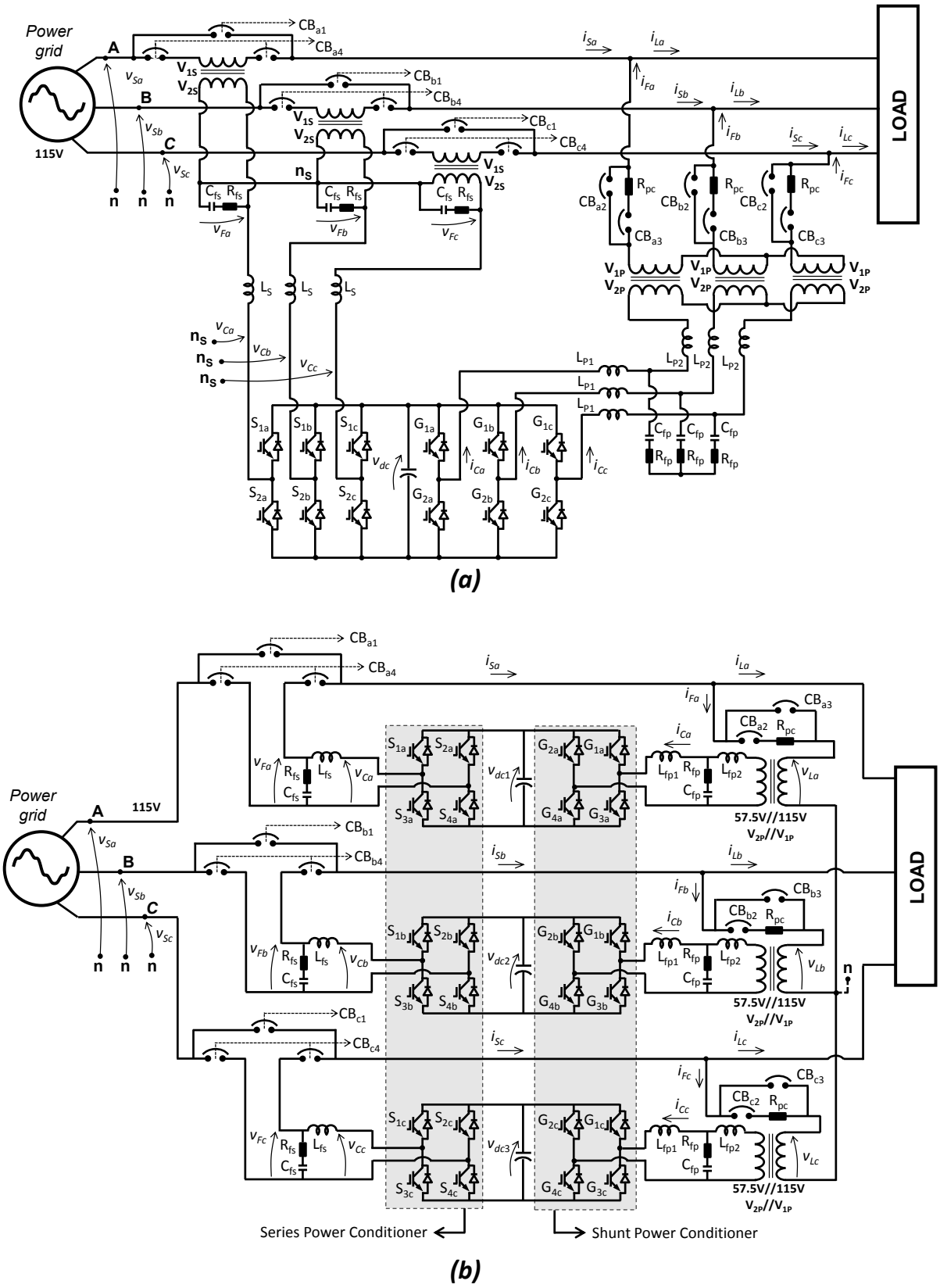

Fig. 1 – Electrical scheme of the Unified Power Quality Conditioner; (a) Conventional topology based on three-phase three-wire back-to-back converters; (b) Developed topology, without series transformers, based on three single-phase back-to-back converters.

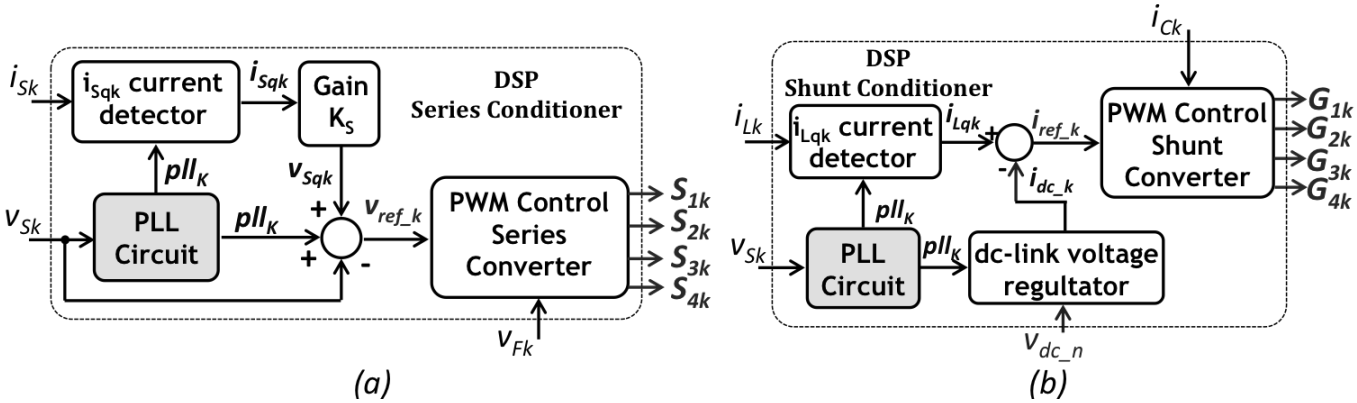

Fig. 2 – Control blocks of the UPQC algorithms: (a) For the series conditioner; (b) For the shunt conditioner.

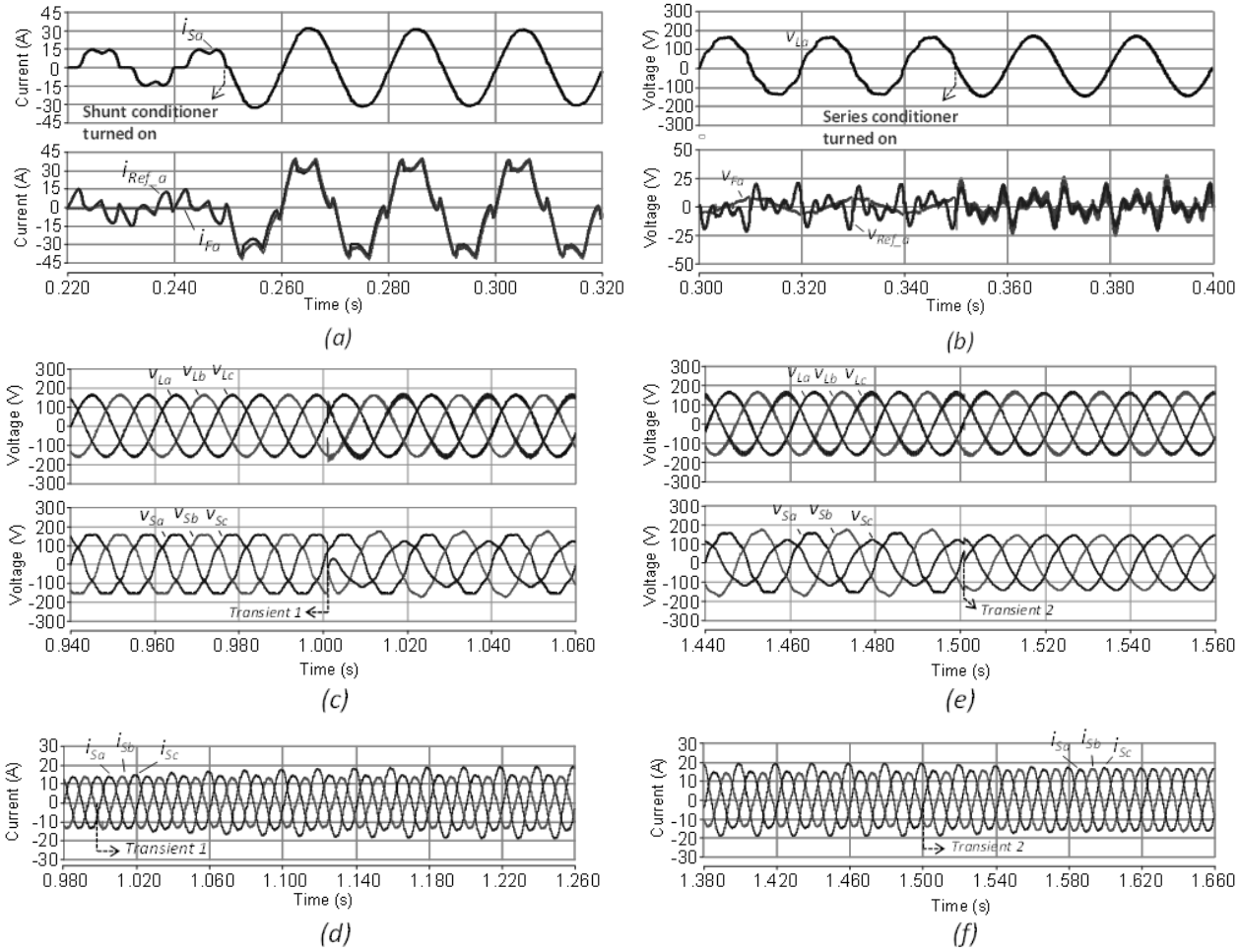

Fig. 3 – Simulation results of transients: (a) When the shunt conditioner is turned on; (b) When the series conditioner is turned on; (c) Load (v_{La}, v_{Lb}, v_{Lc}) and main voltages (v_{Sa}, v_{Sb}, v_{Sc}) when the main voltages become imbalanced (transient 1); (d) Main currents (i_{Sa}, i_{Sb}, i_{Sc}) when the main voltages become imbalanced (transient 1); (e) Load (v_{La}, v_{Lb}, v_{Lc}) and main voltages (v_{Sa}, v_{Sb}, v_{Sc}) when the imbalance at the main voltages is extinguished (transient 2); (f) Main currents (i_{Sa}, i_{Sb}, i_{Sc}) when the imbalance at the main voltages is extinguished (transient 2).

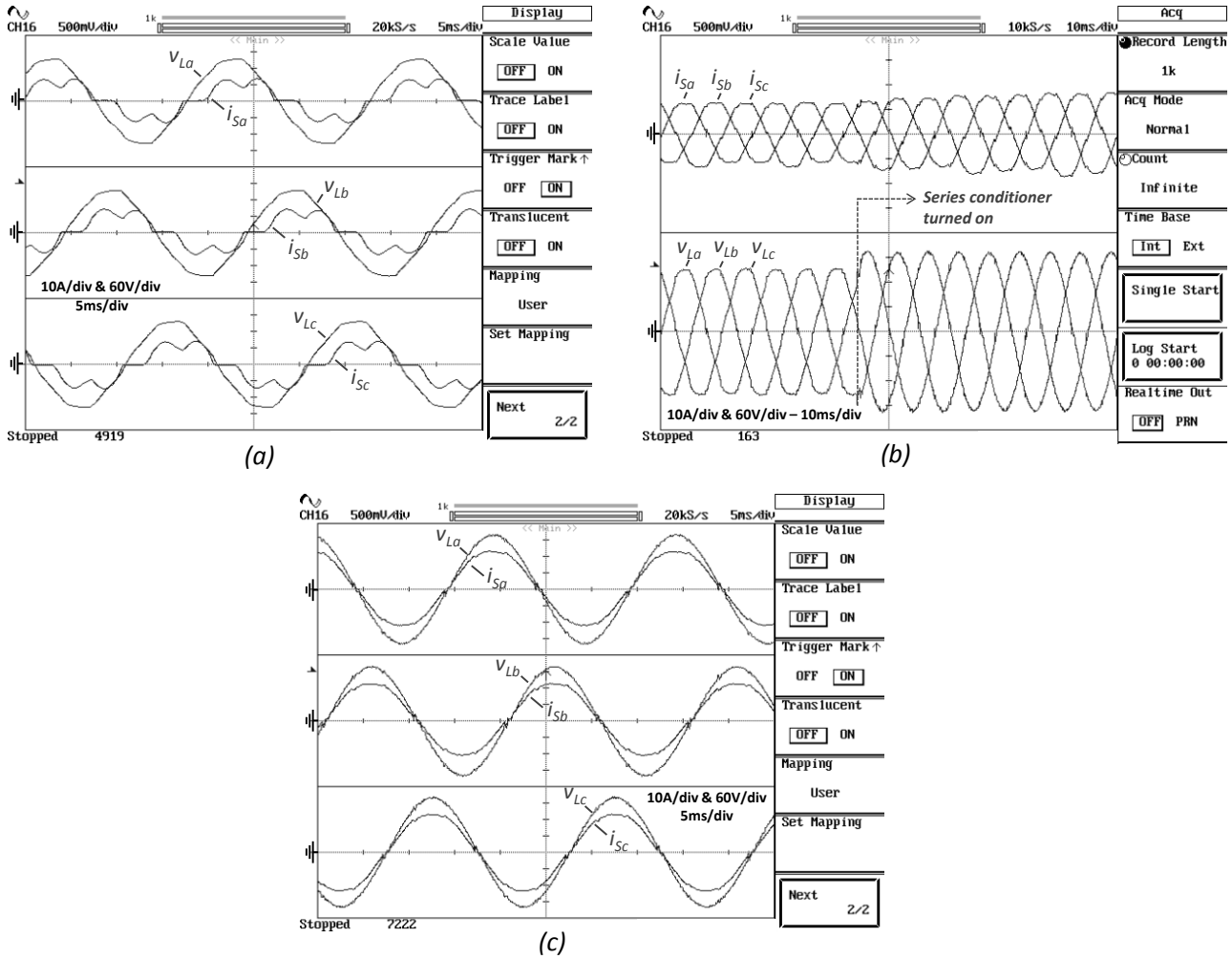

Fig. 4 – Experimental results of the load voltages (v_{La}, v_{Lb}, v_{Lc}) and main currents (i_{Sa}, i_{Sb}, i_{Sc}) for Test Case 1: (a) With both of the UPQC conditioners turned off; (b) At the transient when the series conditioner is turned on; (c) At steady state condition - (50V/div, 10A/div, 5ms/div).

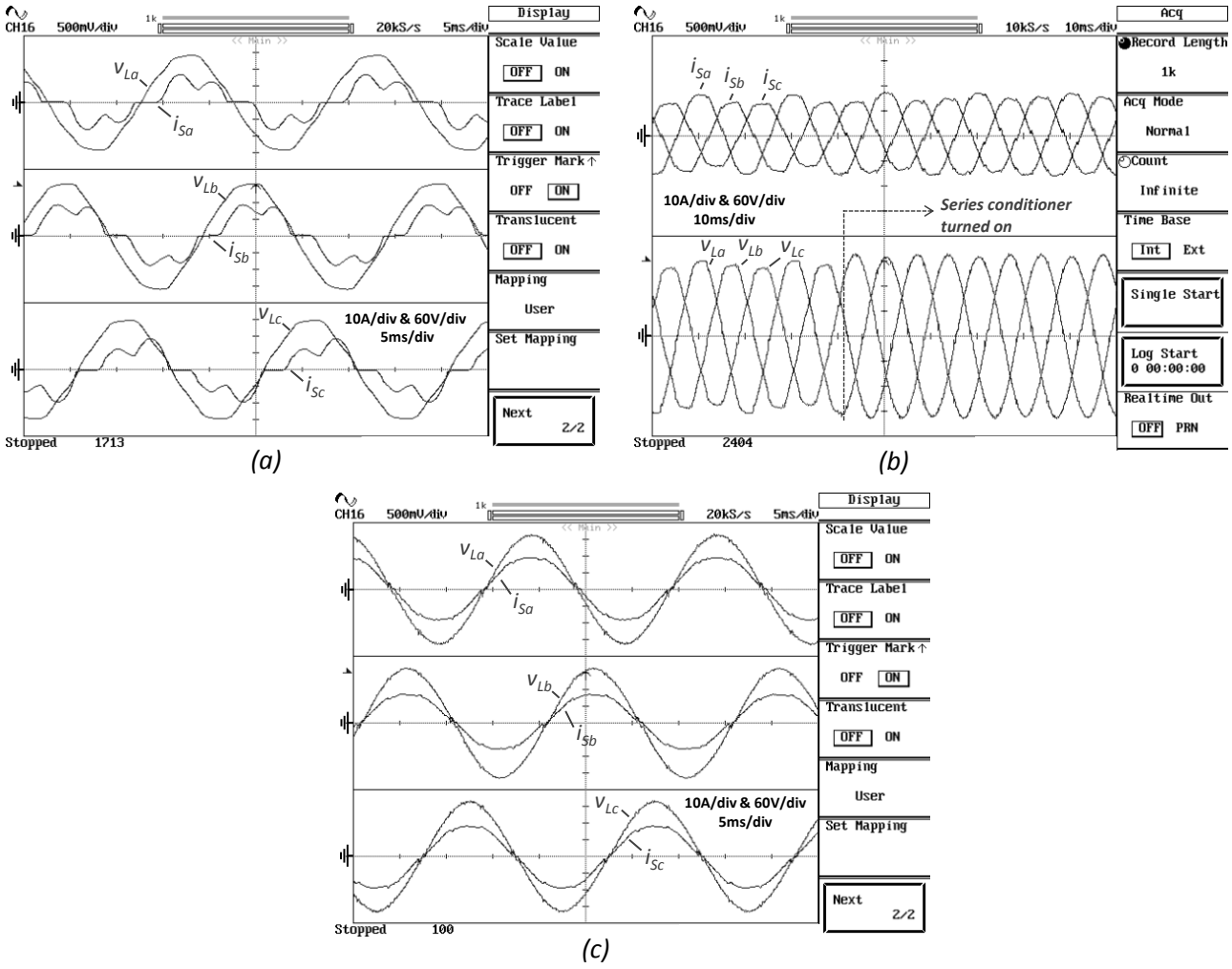

Fig. 5 – Experimental results of the load voltages (v_{La}, v_{Lb}, v_{Lc}) and main currents (i_{Sa}, i_{Sb}, i_{Sc}) for Test Case 2: (a) With both of the UPQC conditioners turned off; (b) At the transient when the series conditioner is turned on; (c) At steady state condition - (50V/div, 10A/div, 5ms/div).

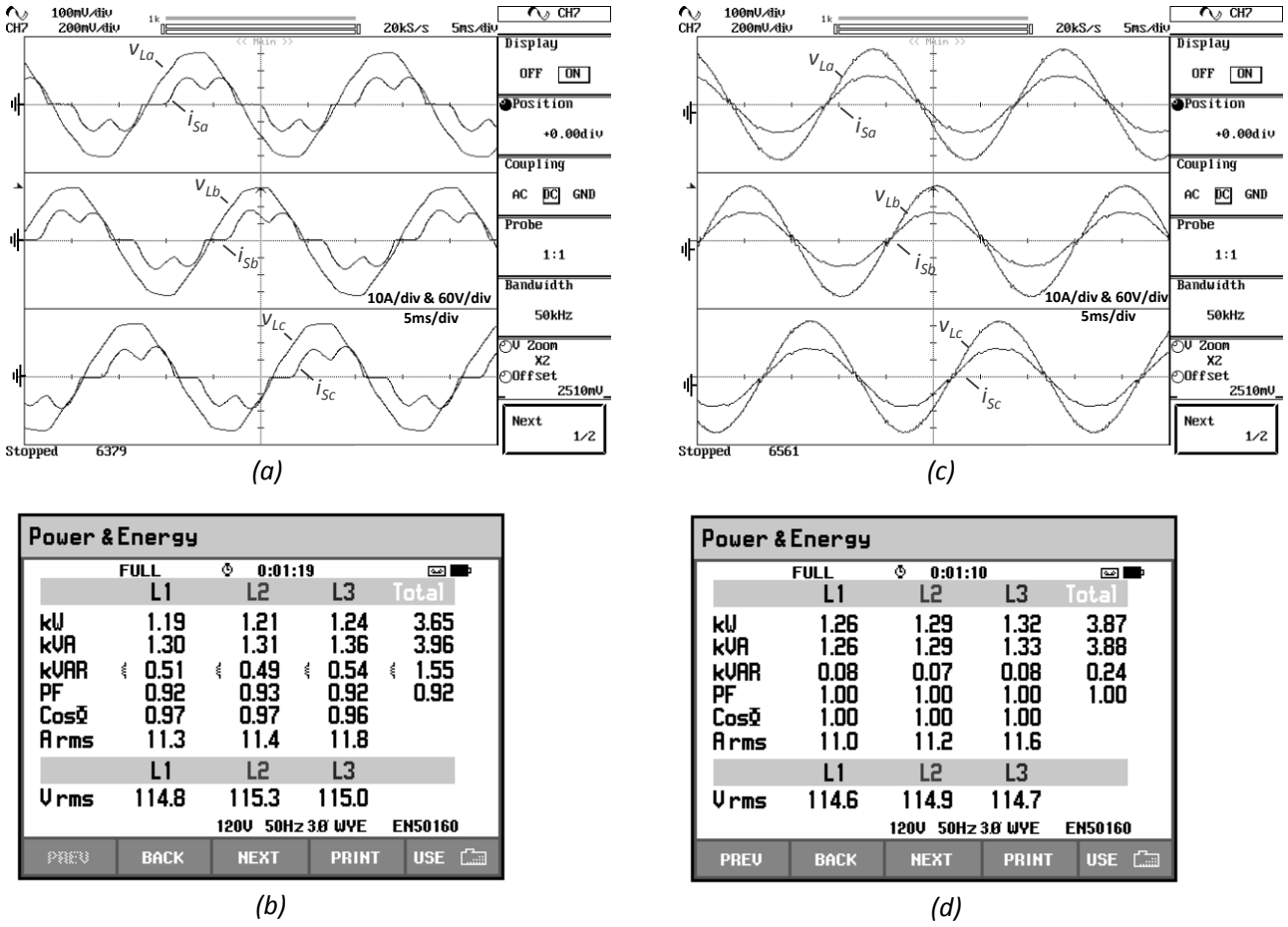

Fig. 6 – Experimental results of the test case 3: (a) Load voltages (v_{La}, v_{Lb}, v_{Lc}) and main currents (i_{Sa}, i_{Sb}, i_{Sc}) with both of the UPQC conditioners turned off; (b) Rms values of the active, reactive and apparent powers, load voltages and main currents with both of the UPQC conditioners turned off; (c) Load voltages and main currents with UPQC turned on at steady state condition; (d) Rms values of the active, reactive and apparent powers, load voltages and main currents currents with UPQC turned on at steady state condition.

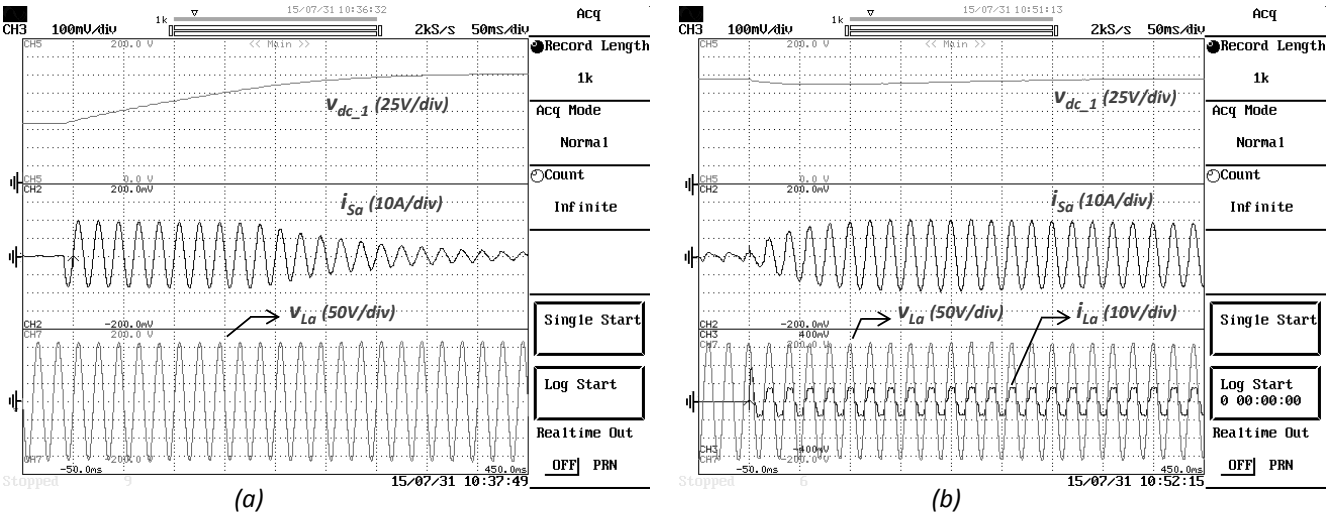

Fig. 7 – Experimental results of the test case 4: (a) dc-link voltage (v_{dc_1}), main current (i_{Sa}), and load voltage (v_{La}) at the time transient when the shunt conditioner is turned on; (b) dc-link voltage (v_{dc_1}), main current (i_{Sa}), load current and load voltage (i_{La}, v_{La}) at the time transient when the load is connected with the power grid.