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Embedded Real-Time Processor for MEMS Applications
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Escola de Engenharia

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Embedded Real-Time Processor for MEMS Applications

Tese de Doutoramento
Plano Doutoral em Engenharia Eletrónica e Computadores

Trabalho efetuado sob a orientação de
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Professor Doutor Luís Alexandre Machado Rocha
STATEMENT OF INTEGRITY

I hereby declare having conducted my thesis with integrity. I confirm that I have not used plagiarism or any form of falsification of results in the process of the thesis elaboration.

I further declare that I have fully acknowledged the Code of Ethical Conduct of the University of Minho.

University of Minho, 28 of March, 2017

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Signature: Nuno André Mano Brito
The PhD is quite often an individual endeavor with several challenges to one’s capacity to overcome multiple psychological and technological obstacles. I consider myself very fortunate to have avoided most of those pitfalls, not due to my level of experience or my capacity to resist when the results are not positive, but solely due to the people I have been around with. Because of it, I will regard this period as one of self-discovery, from which I believe to have gained a more humble attitude towards work and specially, towards people. It would simply not be possible to have finished this journey without the help of my supervisor, professor Luís Rocha, whose experience, advices and guidance were fantastic. I am very grateful to you.

I also want to state my gratitude to many students from the ESRG and CMEMS groups, many of which were and became my friends, sharing good laughs and great moments: Carlos Ferreira, Carlos Silva, Davide Guimarães, Eurico Moreira, Fábio Leitão, Fábio Martins, Filipe Alves, Filipe Salgado, Hélder Silva, MR Gomes, Paulo Garcia, Pedro Macedo, Sandro Pinto, Tiago Gomes and Vasco Lima.

I would also like to offer my deepest gratitude to professors João Monteiro and Jorge Cabral for all their support and for convincing me a few years ago to embrace in such an endeavor and give me the opportunity to learn new technologies that I was not even aware of the impact they have in modern days.

Thank you Embedded Systems Research Group for providing the environment and the conditions to perform the research work with so many great students and investigators.

Last, but not least, I want to offer a big word of gratitude to my parents and specially to my wife, Bruna, for all the patience, support and love that goes well beyond this stage of my life.

This thesis was supported by a PhD scholarship from Fundação para a Ciência e
Abstract

Embedded Real-Time Processor for MEMS Applications

The evolution and widespread of MEMS (Micro Electro Mechanical Systems) devices over the last decades created a new field of study and leveraged the creation of whole new applications and businesses at a worldwide level. The improvements on the manufacturing precision and reliability, allowed some of these devices to be used in mission-critical equipment, such as in airbag systems. The relative low price made it available to home consumer markets, resulting in a paradigm-shift in many application areas.

The test and characterization of each individual manufactured MEMS structure is of major importance, both from the economic and quality standpoints. The dissimilarity of MEMS devices applications and physical principles creates an obstacle, since no single system can fit all the devices singularities, as opposite to what occurred in the Integrated Circuits (IC) industry. Also, new studies have sprung over the recent years that improve our understanding of the underlying fundamental physical phenomena and characteristics of the microsystems.

The Design for Test (DFT) paradigm is becoming an increasing trend and is placing more pressure on the designers to overcome the test costs and reduce the time-to-market by applying embedded mechanisms fully dedicated for testing purposes. This thesis attempts to contribute to the maturity of MEMS testing and control systems development by proposing a flexible digital architecture for real-time control and analysis of structure movements. By the development of an hardware assisted processing platform with basic actuation and sensing mechanisms, real-time and determinism are guaranteed by design to ensure a flexible and adaptable system.

The proposed architecture is evaluated on two applications: First, a fast characterization platform is developed over the base system to enable a time-wise full-wafer
characterization, where the speed and accuracy are optimized and conclusions about manufacturing issues are evaluated. The second application is based on a multi-order sigma-delta closed loop operation, where configurability and feedback delay are critical to allow a high-level algorithm to operate and perform an automated parameter optimization.

In both applications, the major issues are identified and a change in the base platform is performed to fit to each applications goals. In each case, several structures were tested, the results were evaluated and some improvements over the current state-of-the-art methodologies and timings were achieved.
Resumo

Processador embebido de tempo-real para aplicações MEMS

A evolução e disseminação de dispositivos MEMS (Micro Electro Mechanical Systems) ao longo das últimas décadas criou um novo campo de estudo e proporcionaram a criação de novas aplicações a nível mundial. As melhorias na precisão e fiabilidade do processo de fabrico permitiram que alguns destes dispositivos pudessem ser utilizados em equipamento crítico, tal como sistemas de airbag. O preço relativamente baixo habilitou o seu uso em mercados de consumo, provocando uma alteração de paradigma em múltiplas áreas específicas.

O teste e caracterização de cada estrutura individual são ambos problemas de grande importância, tanto do ponto de vista económico, como de qualidade. A diversidade de aplicações e princípios físicos inerentes a este tipo de dispositivos cria um importante desafio, porque não é possível criar um sistema que responda à unicidade de cada um tipo de dispositivo, ao contrário do que sucede na indústria de Circuitos Integrados (ICs). Para além disso, os estudos das últimas décadas acrescentaram um valioso conhecimento sobre os princípios físicos e características fundamentais dos microdispositivos.

Verifica-se recentemente uma tendência de alteração do paradigma de desenvolvimento orientado ao teste (DFT) por forma a optimizar os custos com testes e reduzir o tempo global de desenvolvimento, através da inclusão de mecanismos embebidos no próprio desenho da estrutura. Este trabalho pretende contribuir para o desenvolvimento de testes e controlo de dispositivos MEMS, propondo uma arquitectura digital flexível dedicada ao controlo e análise dos movimentos das estruturas em tempo real. Através do desenvolvimento de uma plataforma de processamento assistida por hardware com mecanismos básicos de actuação e leitura, o determinismo e as características de tempo-real são intrinsecamente asseguradas, resultando num sistema flexível e adaptável.
A arquitectura proposta é avaliada em duas aplicações: A primeira baseia-se no desenvolvimento de uma plataforma de caracterização desenvolvida sobre a plataforma base para permitir a caracterização de uma wafer completa, no qual o tempo de análise e a precisão são optimizados e onde um caso real é avaliado, identificando os possíveis problemas de fabrico. A segunda aplicação consiste no desenvolvimento de um controlador em malha fechada baseado num modulador sigma-delta de ordem múltipla, no qual a configurabilidade e o atraso de malha de realimentação são factores críticos para permitir a optimização automatizada dos parâmetros através de um algoritmo de alto nível.

Em ambas as aplicações, os maiores desafios são identificados e são acrescentadas as funcionalidades da aplicação necessárias à plataforma de base. Em ambos os casos, foram utilizadas várias estruturas, avaliados os resultados e identificadas melhorias no estado-da-arte, quer ao nível das metodologias, quer ao nível da velocidade de análise.
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<th>Description</th>
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<tr>
<td>ADC</td>
<td>Analog-to-Digital Converter</td>
</tr>
<tr>
<td>AFM</td>
<td>Atomic Force Microscopy</td>
</tr>
<tr>
<td>AHB</td>
<td>Advanced High-performance Bus</td>
</tr>
<tr>
<td>AM</td>
<td>Amplitude Modulation</td>
</tr>
<tr>
<td>AMBA</td>
<td>Advanced Microcontroller Bus Architecture</td>
</tr>
<tr>
<td>APB</td>
<td>Advanced Peripheral Bus</td>
</tr>
<tr>
<td>ASIC</td>
<td>Application-Specific Integrated Circuit</td>
</tr>
<tr>
<td>ASIP</td>
<td>Application-Specific Instruction-set Processor</td>
</tr>
<tr>
<td>BPF</td>
<td>Band-Pass Filter</td>
</tr>
<tr>
<td>BRAM</td>
<td>Block Random Access Memory</td>
</tr>
<tr>
<td>BUFG</td>
<td>Global Buffer (Xilinx FPGA component)</td>
</tr>
<tr>
<td>COTS</td>
<td>Commercial off-the-shelf</td>
</tr>
<tr>
<td>CPLD</td>
<td>Complex Programmable Logic Device</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analog Converter</td>
</tr>
<tr>
<td>DDR</td>
<td>Double Data Rate (memory)</td>
</tr>
<tr>
<td>DFT</td>
<td>Design For Test</td>
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<tr>
<td>DRG</td>
<td>Disc Resonance Gyroscope</td>
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<tr>
<td>DRIE</td>
<td>Deep Reactive Ion Etching</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital-signal Processor</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
</tr>
<tr>
<td>FF</td>
<td>Flip-Flop</td>
</tr>
<tr>
<td>FIR</td>
<td>Finite Impulse Response</td>
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<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>FPU</td>
<td>Floating-point unit</td>
</tr>
<tr>
<td>Fr</td>
<td>Resonant Frequency</td>
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<tr>
<td>GPIO</td>
<td>General Purpose Input/Output</td>
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<tr>
<td>HPF</td>
<td>High-Pass Filter</td>
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<tr>
<td>Abbreviation</td>
<td>Full Form</td>
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<tr>
<td>IC</td>
<td>Integrated Circuit</td>
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<tr>
<td>IIR</td>
<td>Infinite Impulse Response</td>
</tr>
<tr>
<td>INL</td>
<td>Iberian Nanotechnologies Laboratory</td>
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<tr>
<td>IRQ</td>
<td>Interrupt Request</td>
</tr>
<tr>
<td>ISA</td>
<td>Instruction Set Architecture</td>
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<td>JTAG</td>
<td>Joint Test Action Group</td>
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<td>LPF</td>
<td>Low-Pass Filter</td>
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<tr>
<td>LUT</td>
<td>Look-Up Table</td>
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<tr>
<td>MEMS</td>
<td>Microelectromechanical Systems</td>
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<tr>
<td>MPSoC</td>
<td>Multiprocessor System-on-Chip</td>
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<tr>
<td>Q</td>
<td>Quality Factor</td>
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<tr>
<td>RAM</td>
<td>Random Access Memory</td>
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<tr>
<td>ROM</td>
<td>Read-Only Memory</td>
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<tr>
<td>RTOS</td>
<td>Real-Time Operating System</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscopy</td>
</tr>
<tr>
<td>SEU</td>
<td>Single Event Upset</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
</tr>
<tr>
<td>SoC</td>
<td>System on Chip</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon On Insulator</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial Peripheral Interface</td>
</tr>
<tr>
<td>SQNR</td>
<td>Signal Quantization Noise Ratio</td>
</tr>
<tr>
<td>UART</td>
<td>Universal Asynchronous Receiver/Transmitter</td>
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<tr>
<td>Vpi</td>
<td>Pull-in Voltage</td>
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<td>(\Sigma\Delta)</td>
<td>Sigma-Delta</td>
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Chapter 1

Introduction

Microelectromechanical Systems (MEMS) are devices that use both the electrical and mechanical properties of Silicon. They have one or more moving masses, springs, dampers, cavities, special sensitive areas, etc, fabricated on a silicon die and can be used to detect and measure displacements and their respective forces such as acceleration, gravity, angular motion, magnetic field, pressure, etc. A real picture of a MEMS inclinometer wire-bonded to its package is shown in Figure 1.1.

![MEMS accelerometer picture](image)

Figure 1.1: MEMS accelerometer picture with wirebonding detail and placed on a ceramic DIL package.

Commercial MEMS devices are often composed of both the physical silicon structure and the signal processing circuit dies, bonded together inside a single package. The output interface can be either analog or digital, but the tendency is for the output to be digital in order to improve the output noise immunity and include signal pre-processing. In the last couple of decades the world witnessed the expansion of micro-electro-mechanical systems from an academic research environment to become a multi-billion dollar industry, with several companies backing the development of new sensors to explore new possibilities for electronic systems to
interact with the physical world [5]. These fascinating devices, although many times ‘invisible’ to our perception, contribute to our continuously improved life comfort, and are responsible for saving countless lives, by improving safety mechanisms, such as airbag systems, gas detectors, etc.

Traditionally, MEMS devices have encountered some problems inherent to the technology: the manufacturing variations result in an uncertainty of the device exact parameters. Also, initial MEMS systems had a low signal to noise ratio and a poor dynamic range, since miniaturized structures are susceptible to various noises and disturbances [6].

Although some of these features have been significantly improved over the last years, there is still room for improvement. For instance, the measurement of each individual device real characteristics is a time consuming process that can be improved by the development of new techniques, in order for that important information to be given back to the designers to fine tune and improve the manufacturing process. Also, recent studies [7] show a big industry interest on the necessity for the development of improved test techniques and design methodologies to overcome the testing cost of devices that have been reported to reach over 60% [8]. Also, as shown by [7], the big divergence on the devices working principles makes it impossible to use the same techniques on the majority of devices. This confirms that the borrowed IC industry testing techniques are insufficient for the challenges presented by the singular MEMS nature and that very often, the existent techniques must be adapted to each specific device.

The industry quest for an ever reduced manufacturing cost has driven the designers to include test mechanisms in the structure itself, in a Design for Test (DFT) paradigm shift. Besides the test challenges, recent studies on non-linearities in MEMS devices [9] show the possibility for significant improvements by exploring new transduction mechanisms based in time measurements [10]. This presents an opportunity to develop new methodologies to sense, automatically characterize MEMS structures and to measure and compensate its degradation over time. Other studies such as [11] propose new theories for control methodologies that require the application in real structures.

An answer to the necessity for a dynamic solution capable of addressing all these modern challenges is presented in this thesis. In order to perform the necessary measurements and control loops, a real-time, low-jitter system, capable of performing demandable digital filters and mathematical intensive control algorithms
is required. This kind of applications requires an efficient digital signal processor architecture that was very expensive to develop in the past. A few years ago, the development of a System On-Chip (SoC) was a possibility only available to a few companies and universities around the world with a good economic situation. The improvement of the Field Programmable Gate Array (FPGA) technology over the last decades brought to the masses what was once a field of study limited to a few organizations.

The possibility to develop hardware and software on a single chip allows the combination of both the high speed processing of hardware with the flexibility of software. Along with these characteristics, the hardware-software co-design brings the possibility to create hard real-time systems by delegating to hardware, the time-critical components of the system. The architecture of a digital system is a crucial factor for the success of any real-time embedded application. The design space exploration of a specific embedded system constitutes a ground worth of exploring [12].

1.1 Scope

This thesis focuses on controlling and testing capacitive MEMS devices with built-in electrostatic actuation mechanisms using the electrical response. The digital circuit is developed on a field programmable gate array (FPGA), minimizing the physical peripheral necessary for the system to operate. The work aims to fulfill the following challenges:

- Processing speed: The system must output results as fast as possible to enable time-wise application such as a full-wafer analysis in a reasonable time frame;
- Flexibility: The system must be easily adapted to new control schemes without losing the basic performance and predictability characteristics;
- Real-Time behavior: There should not be any post-processing of data such as post-evaluation of frequency value; The system must address the real-time output at an architecture level;
- Predictable: The system must determine a read value on each actuation cycle.
Cost: The system should be developed using low cost commercial off-the-shelf (COTS) products whenever possible.

Debugging: The system must provide debug tools to ease the development and the identification of system bugs.

This work focuses on the creation of the several building blocks necessary for the development of such a system. The information stream between the several blocks are optimized to delegate to hardware the most demanding tasks while enabling an easy synchronization of the data flow using a processor as a configuration and supervisor node.

1.2 Motivation and Objectives

The development of a flexible and high-level programmable digital architecture can enhance the testing and validation of new control methodologies and help acquiring new fundamental knowledge that can lead to improved reliability of fabricated devices. In particular, the proposed architecture can be extended to different sensors and has the potential to play an important role in the evaluation of new physical phenomena at the micro domain.

The control of a feedback operated MEMS sensor or actuator is a complex system that involves several areas of expertise: The study of the MEMS device characteristics and physical properties, the analog circuitry necessary to sense the mass displacement and actuate the structure, the tailored digital controller and the software engineering are, all together, parts of a platform to improve performance, develop new concepts and test new features on these kind of devices.

Currently, the measurement of structure parameters must be performed in an advanced laboratory, usually by the manufacturer itself, and although the structure manufacturing process can be very accurate, the fine knowledge of each device specific parameter enables measurement improvements and compensation of drifts in both the manufacturing process and variations that come with its ageing. The traditional approaches to create feedback operated MEMS devices are based on processor-less FPGA implementation, using Application-Specific Integrated Circuits (ASICs) or discrete electronics hardware modules, and although the performances are quite good, they come at a significant price of lack of flexibility.
One major objective of this thesis is to create an application specific processor, with DSP capabilities, tailored for the development of MEMS applications (sensing and actuation) that explore feedback operation, including pull-in based transduction mechanisms. In order to optimize the processor and its associated toolchain to fit the application, we must first identify and understand the performance bottlenecks, the real-time requirements of the system, and identify parts of algorithms that can be developed as hardware blocks (hardware/software co-design), thus improving the processor performance, while maintaining the software flexibility, relative simplicity and development productivity. The creation of a tailored MP-SoC for the control of MEMS devices based on the pull-in phenomenon requires the study and understanding of several topics:

- FPGA development;
- Computer architectures;
- MEMS design and control.

Any of the enumerated topics are nowadays an object of intense study with constant performance improvements, that goes in hand with the increased complexity of the underlying concepts involved.

The symbiosis of all these modern technologies presents a very interesting set for pushing the state of the art performances, but also brings with it a major challenge in understanding the inherent difficulty of each technology as well as the great complexity of mixing all these topics to create a very efficient and novel concept. The implementation difficulties to overcome both the expected and unexpected digital, analog and mechanical issues that are implicit to such an endeavor creates a challenge that very easily increases the difficulty to identify, analyze and solve individual problems in a system that must operate as a whole.

The scientific contributions will be on the development of specific hardware and software blocks optimized for MEMS applications and its use in the characterization of MEMS devices, by applying a set of algorithms to electromechanically actuate on the structure and through that process, infer the device physical parameters, and in testing control algorithms for MEMS sensors and actuators. In order to achieve this goal, a set of milestones must be met:

- Development of a customized processor-centric platform with dedicated hardware to guarantee deterministic execution and performance;
Integrate this platform within the MEMS’s readout circuitry;

• Develop a control algorithm to extract the observable device behavior;

• Hardware/Software Co-design of the control algorithm;

• Implement and test control algorithms for pull-in based MEMS sensors.

A flexible, yet robust and fast development platform will enable exploration of new sensing and actuation principles for MEMS devices opening a new paradigm for MEMS: adaptive MEMS. In the current work, a processor-centric approach is developed to achieve a more flexible platform, allowing performing dynamic characterization of MEMS devices (estimated dimensions and parameters manufacturing drifts) and exploring new sensing and actuation MEMS principles using sigma-delta (ΣΔ) controller as an example.

### 1.3 Research questions and Methodology

It is expected that a dedicated digital architecture towards MEMS development will be beneficial for the testing, validation and development of new control methodologies. According to the established objectives, the following questions are postured:

• Is it possible to establish a set of common elements that can be added in the design phase to simplify the control system development through hardware/software reuse?

• How can these elements be exploited without sacrificing the software flexibility?

• What performance and processing system simplicity can the system attain?

• How can this architecture be exploited to maximize scalability and high level programming?

The following methods were performed to answer the above questions:

1. Design a solution capable of performing the necessary intensive digital signal processing algorithms in real-time;

2. Identification of the basic building blocks for the generic base system to which
extensions can be developed with minimal hardware and software intrusion;
3. Propose changes to the MEMS designs that enable the injection and control of electrostatic forces;
4. Development of use case applications to evaluate the platform necessities, flexibility and performance.

1.4 State of the art

In this section, the state of the art on control systems used for characterization, test and control of MEMS devices is reviewed. The modern requirements and an ever quest to improve the technology and reduce manufacturing costs demands the development of specialized tools that in it’s turn poses a pressure to build more processing intensive and integrated solutions.

As an example, the characterization and evaluation of devices manufacturing deviations is still frequently performed using classical integrated circuits (IC) technology, which includes several advanced optical technologies. As this technology stands as the base for characterization of MEMS, a brief review of the classic methods is reviewed in this chapter, with the advantages and limitations of these approaches.

The electrostatic control of sensors that are by design capable of actuation is not recent, but opens the possibility for other approaches with several advantages and challenges such as the implementation of a feedback loop. The state of the art is analyzed for both open and closed-loop control systems using the electrostatic mechanisms, as different methodologies and technologies can be used to leverage new applications.

1.4.1 MEMS devices test and characterization

The development and improvement of testing techniques for MEMS has received an increasing attention in the MEMS community over the last years [7]. This includes three distinct testing technologies: Optical measurements, electrical measurements and mechanical tests.
Traditionally, there are a number of methods to carry out measurements based on optical techniques, such as scanning electron microscopy (SEM), atomic force microscopy (AFM), stylus profiler, and optical profiler among others [13], where the feedback provided by these tests are typically the device real dimensions.

Electrical tests performed over the structures have also been developed and used mainly to provide functionality tests, but traditionally are not meant to provide information about physical properties. However, due to the possibility of electrostatic actuation, is became possible to perform control loops on the device simulating the external forces and measure the resulting electrical signal from which some mechanical properties can be derived. The low-latency possibilities offered by this technique [14][15], the possibility to test a large range of sensitivities of devices [15], and the lack of need for using costly mechanical stimulation offer a different and complementary solution.

There are however some characteristics that are usually hard to address using both the electrical and optical tests, such as the device stiffness, fracture strength or actuation range. The mechanical application and control of the physical mechanical property on the device (for instance, a micro needle in the case of inertial devices) offers a complementary alternative to the mentioned techniques. It offers the advantage of lacking the dedicated actuation mechanisms built on the device, but such as the optical technique, requires dedicated, expensive machinery and is built to be used on a laboratory environment since the die is often exposed.

The use of both optical, electrical and electromechanical processes has an objective of providing one or more characterization values. The characterization of each kind of MEMS devices is different due to its very specific nature and objective. In fact a single characterization technique may not be enough to characterize one kind of device under every condition it must operate. The new characterization techniques are a result of the industry requirements and drives [16]. Electrical tests have better speed performance and are better suited for automation than the application of a mechanical stimulation, since mechanical stimulation rely on engines and changes in physical properties that have a significant latency associated.

In this subchapter, an overview of the optical, electrical and electromechanical tests is presented as well as the typical full-wafer characterization techniques described in the literature.
Optical measurement

Although electrical and mechanical tests provide functionality feedback and allow the deduction of some design issues, they do not provide the complete measurement of the device geometry and physical properties. Some techniques allow for a real-time dynamic response measurement such as Laser Doppler Vibrometry (LDV) with reported resolutions down to the picometer level and bandwidth up to 24 MHz [4]. Table 1.1 shows a resume of the typical optical measurement techniques and capabilities. The resolution achieved can be very high and some techniques allow a dynamic response measurement over the structure area and even volume.

Other approaches include complex solutions such as the one developed by [13], where a computer microvision system was developed for in-plane motion and a phase shifting interferometry technique is used for the remaining out-of-plane motion measurement.

Although the reliability and precision of optical approaches is quite significant, this kind of characterization techniques require dedicated, expensive instruments and expertise. Besides, there is no possibility to perform real-time diagnosis or in-loco testing since it must be performed with dedicated and laboratory instrumentation.

According to [4], the main advantages of optical measurements include the following characteristics:

- Noninvasive technique;
- Does not disturb the sensitive MEMS device;
- Very high resolutions possible;
- Higher measurement range possible;
- Possible use of a several different optical phenomenons.

Mechanical measurement

Back in 1999, [17] measured a cantilever fracture strength using both a microprobe mechanical stimulus and compared the results with traditional optical techniques. Some other works use a similar approach to determine very specific features: In 2009, [18] used a microprobe to actuate on a magnetic photosensitive polymer
Table 1.1: Optical measurement techniques [4]

<table>
<thead>
<tr>
<th>Technique</th>
<th>Lateral Resolution</th>
<th>Vertical Resolution</th>
<th>Static Shape</th>
<th>Dynamic Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATM (Atomic Force Microscopy)</td>
<td>0.0001 µm</td>
<td>0.0001 µm</td>
<td>3D</td>
<td>No</td>
</tr>
<tr>
<td>SEM (Scanning Electron Microscopy)</td>
<td>0.001 µm</td>
<td>n.a.</td>
<td>2D</td>
<td>No</td>
</tr>
<tr>
<td>OM (Optical Microscopy)</td>
<td>&lt;1 µm</td>
<td>&lt;1 µm</td>
<td>2D</td>
<td>No</td>
</tr>
<tr>
<td>WLI (White Light Interferometry)</td>
<td>&lt;1 µm</td>
<td>&lt;0.001 µm</td>
<td>3D</td>
<td>No</td>
</tr>
<tr>
<td>CM (Confocal Microscopy)</td>
<td>&lt;1 µm</td>
<td>&lt;0.01 µm</td>
<td>3D</td>
<td>No</td>
</tr>
<tr>
<td>DHM (Digital Holographic Microscopy)</td>
<td>&lt;1 µm</td>
<td>&lt;0.001 µm</td>
<td>3D</td>
<td>Yes</td>
</tr>
<tr>
<td>SVM (Strobe Video Microscopy)</td>
<td>&lt;0.01 µm</td>
<td>&lt;1 µm</td>
<td>2D</td>
<td>Yes</td>
</tr>
<tr>
<td>LDV (Laser Doppler Vibrometry)</td>
<td>&lt;1 µm</td>
<td>&lt;10^6 µm</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

cantilever and determine the device characteristics to validate the design models.

The FT-MPS02 MEMS Probestation [1] offered by the Swiss company FEMTOTOOLS enables the mechanical in-plane and out-of-plane testing of devices through the use of a microprobe as shown in Figure 1.2. The mechanical probe holds a force resolution down to 5nN with a silicon tip area of 50µm by 50µm.

![Figure 1.2: FEMTOTOOLS probe station showing a mechanical probe test on a MEMS device [1].](image)

On the other hand, the device specificity can be addressed by forcing the physical property instead of acting directly on the transduction mechanism, such as using a shaker for the stimulation of an accelerometer, or heating/cooling chamber in
the case of temperature sensors.

**Electrical measurement**

The electrical measurement techniques are tightly related to the type of structure and the target physical properties to measure. The idea of having dedicated mechanical electrodes for electrostatic actuation is not recent. [19], [20] and [21] considered self-test techniques for inertial MEMS by using electrostatic actuation to mimic external acceleration.

In 2002, [22] settled an experiment to measure the mass \((m)\), electrodes distance \((d_0)\), and the spring constant \((k)\) using electrostatic actuation on a suited capacitive accelerometer. The experiment is based on the application of a DC voltage that matches the 1G acceleration applied on the structure and the parameters are then deduced mathematically over the collected data.

In 2006, the same principle was used by [23]. The measurement of a cantilever beam physical properties was performed by applying an optimized set of AC signal in the structure capacitors. Mass, damping and spring constant are reportedly determined with 5% accuracy.

[24] and [14] system allows for electrical stimulation on MEMS structures backed by an FPGA set of algorithms to attain a significant performance on the structure parameters evaluation. These techniques are also used to develop self-calibration and self-testing capacity on modern electrostatic inertial sensors and resonators [25].

[14] presented a fully electrical test procedure for MEMS characterization based on electrostatic actuation using a FPGA for data acquisition and a computer to process and control the device position.

Several works use the electrostatic forces to apply new signal processing techniques on a pursuit for better performances or processes automation. [26] demonstrated that an accelerometer can be tested and calibrated without applying a physical stimulus, by application of electrostatic forces using built-in test plates. The innovation of his work stands on the use of extended Kalman filters on a sigma-delta closed-loop scheme to estimate the model unknown process parameters and provide automatic calibration capability.
In the last years some commercial solutions became available to back up this necessity by providing complete or partial solutions to enable the development of customized analysis and control solutions for MEMS:

- The Italian company ITMEMS [27], a spin-off from Polytechnic of Milan offers a ready to use diagnosis tool for MEMS characterization of values such as rest capacitance, stationary CV curves with pull-in and pull-out, resonant frequency and Q factor. It is a closed system with the possibility to perform complex computer analysis over the acquired data for an in-depth analysis of the structure characteristics. This company also provides other hardware modules to perform characterization for specific devices such as gyroscopes, resonators or Peltier-based micro-chambers;

- The French company Asygn offers a signal generation, acquisition and processing system dedicated for MEMS devices based on a Zynq FPGA and a proprietary analog chip for signal generation, acquisition and conditioning. This platform allows for some flexibility by handling the signal conditioning and enabling the customization of the Digital Signal Processor (DSP).

**Wafer-level testing**

The traditional method to wafer-level test MEMS devices is borrowed from the integrated circuits (IC) industry, where electrical tests are performed individually over each die on the wafer, through needle probes. As opposed to the IC devices, MEMS require characterization both in their static and dynamic states. Although the static test can be enough for some MEMS devices, for the majority of sensors, it is essential to test for the behavior and reliability when subjected to the forces or properties that the device is built to measure. Many MEMS sensors need also to be tested while stimulated in order to evaluate the change in its electrical characteristics, when the stimuli vary in its nominal range. While in some sensors, it may be relatively easy to do so, such as in the commercial-range temperature sensors, it can be a very expensive procedure to do with others, such as with high-pressure sensors. In this case, it is usually necessary to create robust and expensive chambers to apply such dangerous pressures as well as all the other constraint that it must withstand, such as humidity and temperature [13]. The use of instrumentation and automation mechanisms may not always be possible under harsh conditions.
The full-wafer analysis can be performed using optical techniques to obtain the map of faulty structures. [4] reports the resonant frequency analysis of a full-wafer using LDP technology with 2 seconds per device measurement rate.

Some authors propose electrical approaches to perform a full-wafer analysis on an automated way: In 2011, [24] proposed a parallel tester architecture to test and calibrate full-wafer MEMS accelerometers using a computer connected to an FPGA capable of application of electrical stimuli’s on the structures and subsequent analysis of simple test routines by pattern matching evaluation and to compute calibration data.

As an evolution of the [24] work, [14] performed a fully electrical test procedure for inertial MEMS characterization at wafer-level. In this work, a computer controlled FPGA setup is developed to measure Capacitance, Fr, Q and QUAD bias. Targeted at wafer-level testing, it takes about 4-10 seconds per device.

1.4.2 Digital solutions for MEMS control

The digital control of MEMS devices poses several advantages by delegating to the digital domain the signal processing and thus, taking advantage of the high performance computation available. [28] classifies MEMS control into three classes:

- Open-loop: The simplest approach where a signal is applied and the result is measured;
- Open-loop with input pre-shaping: The knowledge of the device model allows the creation of pre-fitted inputs to compensate for the device limitations/non-linearities;
- Closed-loop: The most computationally demanding, but allows the correction of many of the devices mechanical limitations;

The creation of dedicated digital systems to control MEMS devices is not recent. Over the years the designs were improved along with the embedded systems technology evolution. In the academic world, the development has geared toward the resolution of specific, isolated problems with the most advanced solutions based on an FPGA or an ASIC to perform the signal processing necessary for signal conditioning and control.
The dominant approach for obtaining a high performance system is the introduction of a feedback loop. The closed-loop approach delegates on the electronics the responsibility for much of the precision improvement and quite often still allows a relaxation on the manufactured device specifications [29]. Unlike traditional macro mechanical systems, MEMS devices control is more challenging than its macro mechanical counterparts due to its small nature, fast actuator dynamics and increasingly demanding noise performances. The development of a closed-loop control, in contrast to the open-loop approach depends on the sensor nature, size and speed [30]. The hardware necessary for the gains brought by the closed-loop approach is being rapidly overcome by the advances in the embedded systems technology, and more specifically, by the digital signal processing performance brought by the FPGA technology.

Vagia et al propose a closed-loop approach for electrostatic actuation control of MEMS devices based on a PID controller [31], [32], [11]. A comprehensive analysis and simulation are performed for a robust PID-control switching scheme for an electrostatic micro-actuator. [33] used this approach to control a micro-actuator position up to 88.9% of the full-gap. [34] designed a fourth-order sigma-delta gyroscope and accelerometer ASIC controller with an electronic filter in series with the mechanical element to reject the in-band quantization noise present in second-order solutions.

The use of sigma-delta modulators stands as the leading technique for maximizing the device performance in closed-loop applications. Several works have explored this technique to achieve state of the art performances such as [35], [36], [37], [29], [38], [39], [40] and [41]. The most recent developments include an exploration of novel setups by the increase of higher order stages [36], [34] and modification of the modulation gains schemes for improvement of specific performances such as noise [39] or nonlinearity compensation [42].

Other solutions include a mix of ASIC and FPGA, while others have the all control integrated on an ASIC. Back in 2004, [35] proposed a new digital architecture for closed-loop control of MEMS gyroscopes. The system consisted on the development of an ASIC containing the circuitry for excitation and readout of the capacitive/electrostatic gyroscopes. An FPGA connected through a digital 1-bit sigma-delta modulated signal has been responsible for the application of the feedback loops and signal extraction. The programmable features of the FPGA allow the system customization for other devices of the same types while the implemen-
tation of the ASIC enabled a greater immunity to analog low-frequency noise. In fact, the use of an FPGA for the development of novel closed-loop control techniques for MEMS has been widely used:

- [36] developed an accelerometer with a fifth-order sigma-delta modulator as a feedback loop. The use of the fifth-order achieved a significant improvement of the Signal Quantization Noise Ratio (SQNR) when compared to a second-order loop;

- [43] developed an FPGA-based hardware platform for tuning MEMS gyroscopes using the closed-loop response analysis using a computer through a classic parallel interface;

- [44] controlled a MEMS disc resonant gyroscope (DRG) using a digital circuit developed on an FPGA in a configurable closed-loop configuration. The digital filters, feedback loop and UART communications are developed to prove the flexibility, precision and reliability of the programmable digital solution as a replacement to the cumbersome and less flexible traditional analog systems;

- [45] developed a FPGA-Labview application for design and noise analysis of a closed-loop tunneling accelerometer. In this case, the author developed a third-order Kalman filter controller on the CompactRIO real-time embedded industrial controller to improve the tunneling accelerometer power consumption and noise performance;

- [46] presents an FPGA based closed-loop control system for a MEMS vibratory gyroscope. The authors implement a least mean square adaptative algorithm to serve as a demodulator to separate the amplitude from phase of the gyroscope’s vibration for subsequent control. The fast separation process proposed allows a compensation input for the automatic gain controller.

- [47] used an FPGA to control a custom micro-g accelerometer in both open and closed-loop configurations. This allowed the exploration of several configurations with significant improvements on the sensitivity, linearity and dynamic range;

- [33] developed an FPGA application that enabled the control of a MEMS actuator out of the linear zone. This closed-loop On-Off controller enabled the controlled displacement up to 88.9% of the full-gap and was obtained
due to the feedback loop high frequency operation offered by the FPGA technology.

- [48] controlled an electrostatically actuated parallel-plate inclinometer using an FPGA to perform pull-in measurements, hence obtaining a very high resolution by using pull-in as the transducing mechanism. The FPGA is responsible for the actuation ramp generation and for the event detection. The data is obtained using a UART peripheral controlled by the FPGA.

- [39] developed a multi-stage sigma-delta controller based on analog amplifiers and a second application implemented on an FPGA for digital control. The system was developed to test and measure new configurations based on cascading sigma-delta blocks, attempting to optimize the stability and obtain a higher overload input level.

- [40] presented ASIC-FPGA platform to evaluate MEMS gyroscopes, in a closed-loop sigma-delta operation. The solution proposed in this work introduces a complete platform for developing MEMS-based closed-loop inertial sensors. The platform comprises a custom programmable digital capacitive ASIC with the sense, drive interfaces and digital filters. An FPGA is used along to perform the application-specific control algorithms.

- [41] presents a nanopositioner MEMS control system based on customized high-voltage actuators and a sigma-delta modulation for analog to digital conversion. The closed-loop control circuit was developed in FPGA;

Some different approaches propose the design of specific processors to improve the system, some of which are patent-protected:

- A. Mokhtar, A. Elsayed and A. Elmallah et al applied for patents to protect an interface for MEMS inertial sensors based on an ASIC (U.S. Patent 8476970, U.S. Patent 8508290, U.S. Patent 9013233). In their applications, an ASIC for capacitive accelerometers and gyroscopes sigma-delta control is described with details on the signal conditioning, interface actuation, and a digital processing core.

- Dahlon Chu (U.S. Patent 6301965) patented a digital feedback control circuit Application-Specific Instruction-set Processor (ASIP) for accelerometer sigma-delta closed-loop control which is an improved version of the work of [49].
[50] simulated the results for an application specific DSP for closed-loop control of MEMS gyroscopes with hardware optimized operations based on a RISC architecture. The main goal is the optimization for the digital filters and the reduction of code complexity and power consumption by adding some application specific instructions in the processor. This project proposes and simulates a change in the use of typical digital solutions by customizing the processor instruction set architecture (ISA) such as FIR filters specific instructions at the processor core level.

1.4.3 Conclusions

The pursuit to push the state of the art performances is now quite often accomplished due to corrections and improvements performed at the system control level. The uniqueness of each device and the lack of a common architecture presents as an opportunity to study and offer a faster prototype solution that can be easily adapted to fit the particular needs of the myriad of devices developed nowadays. From the amount of solutions found in the literature, it is evident that the use of digital solutions to control MEMS devices is widespread but the solutions do not follow a common architecture.

The determinism and fast dynamics nature of the MEMS technology demands a fast yet deterministic solution for the hard real-time problem presented. From the multiple solutions analyzed, the use of an FPGA to perform the signal processing using true hardware parallelism seems to be a common option that offers significant flexibility on a reasonable cost and power consumption, with some companies currently offering solutions for the electric analysis of electrostatically actuated devices.

Also, it is reasonable to conclude from the current set of research works that the sigma-delta modulation has been widely used as a feedback alternative to push the devices performances. The use or development of an ASIC, although interesting, both from the high-volume cost perspective and black-box transfer characteristics translates in the loss of some flexibility, adaptability and/or the necessity for higher investments. It’s advantages, although necessary for some current state of the art solutions, were not considered as an option to build a more generic and fully-adaptable platform.

The design and evaluation of a complete stack solution, from sense and actuation
hardware mechanisms, processor, operating system and high-level scripting inter-
face can contribute with a guideline with practical real-time measurements to the
MEMS technology development.

1.5 Thesis Structure

This thesis is structured on the following chapters:

- Chapter 2 describes the research elements used to build the base system for developing the demonstrator applications. It contains the evaluation of different alternatives on the processing architecture, operating system and development tools, considering the posed real-time constraints;

- Chapter 3 presents the working base system, with the necessary common elements to enable basic MEMS controls, from the input circuitry to output control. The scalability, reusability and real-time constraints are key features to assist the demonstrator applications development.

- Chapter 4 describes the MEMS test and characterization solution using the built-in electrostatic actuation mechanisms. The resonant frequencies (Fr), quality factors (Q) and pull-in voltages (Vpi) measurements techniques are described and the results analyzed. Finally, a full-wafer analysis is carried to test the performance and draw conclusions on the results.

- Chapter 5 presents the solution to create a configurable multi-order sigma-delta accelerometer. Several orders were tested and the noise and sensitivity levels are compared using multiple setups in two different devices.

- Chapter 6 draws the general conclusions. The benefits and limitations from the research work developed are presented and suggestions for future work are addressed.
This chapter describes the elements selected for the platform development that stand as the base instrument for developing the demonstrator applications. The reasons that support the selected platform components and architecture decisions are described. An overview of the hardware and software requirements to realize the proposed system is also presented, including the interface circuits and the MEMS basic features that allow integration with the digital system.

### 2.1 Platform Requirements

Several elements must be considered when developing an embedded solution such as the processor architecture, comprehensive and reliable toolchain and the flexibility to adapt to new configurations. The following requirements have been initially established:

- A commercial available SoC with a stable and comprehensive software stack should be selected to minimize the software development effort;

- The system must be powerful enough to fulfill the computational necessities, but must be easily configurable and extended without significant performance degradation;

- An affordable system cost should be attained by optimizing the available computational resources by extensive use of reprogrammable hardware;

- Intensive signal processing capability and deterministic features are essential
characteristic to attain a hard real-time system.

Based on the above mentioned requirements, a processor centric solution based on the stable and customizable Leon3 soft-core processor was considered, with some inherent advantages related to the soft-core approach [51]. The processor is the central part of a SoC architecture based on the AMBA protocol, where custom peripheral can be easily attached to the processor memory map. Figure 2.1 shows the processor architecture, it’s high-performance bus (AHB) and the peripheral bus (APB), the bridge, memory controller and multiple peripherals that build the processor system. The system is configurable so that the unnecessary peripherals can be removed, saving routing space and power.

![Figure 2.1: Leon3FT block diagram of the available peripherals [2].](image)

The following sections present the solutions and consideration for each part of the platform selection, from the processor and its core functions to the selection of the operation system.

### 2.1.1 Processor Toolchain

Embedded processors, as opposite to general purpose processors, are devices that are tailored for specific applications, and as such, they are especially suited for hardware-software co-design, where both the hardware and software are designed to work tightly coupled, in order to achieve the needed performance while maintaining a low budget solution.
It is then possible to divide the computational load between software and hardware, decreasing performance bottlenecks by deploying some intensive processing to pure hardware blocks, and maintaining a good flexibility and productivity by keeping a processor as the system controller. A soft-core processor is a microprocessor implementation using logic synthesis to be used in programmable logic technologies, such as FPGA or complex programmable logic device (CPLD). By being implemented using only logic, soft-core processors allow a higher degree of flexibility and configurability when compared to their counterparts. In the early ages of programmable logic development, a soft-core processor was used mainly for academic purposes, due to the fact that they occupied the majority of the programmable logic device, leaving almost no space for extra logic, making them a high cost solution with low performance.

With the increasing improvement of FPGA and CPLD technology, the industry started to adopt soft-cores, since the number of logic elements that they occupied became less significant when compared to the increasingly available number of elements, and because their performance got much better. Besides, a soft-core allows a more affordable investment on development, since the processor can be adapted to fit the application needs and more validation tests can be performed before turning the design to ASIC, if it ever gets necessary [52]. A safeguard must be made here to mention that although ASIC processors are regularly prototyped in FGPAs, a effort must be made to accommodate the performance difference of FPGA resources (logic elements, RAMs, multipliers, and routing) to the relative performance of ASIC resources (gates, RAMs, and wires). Because of these relative performance differences, some techniques used by ASIC processors to increase performance may actually decrease FPGA processor performance [53].

Nowadays, there are many soft-core implementations, with distinct features, performances and available toolchains. With the increasing evolution of both programmable logic and computer architecture technologies, it is now common to have Multiprocessor System-on-Chip (MPSoC) devices inside an FPGA, increasing the computational power, while maintaining a low-cost and low power solution. However, for the MEMS dedicated real-time processor necessary for this dissertation, there are some basic characteristics for a soft-core to be considered. Some of them are:

- Coprocessor interface
- Data and instruction cache
A Zedboard development kit, shown in Figure 2.2 was used to develop the system. It offers a good price-quality balance for the Zynq-7020 FPGA, which combines a Cortex-A9 dual-core with an FPGA, 512 MB DDR3 and 256 Mb of Flash memory with many standard and general purpose peripherals. Despite the presence of the hard-core, it was decided to develop the system around a soft-core processor for both the flexibility, portability and above all, the learning opportunities it provides. The Vivado Design Suite 2013.4 was used for simulation and development. The top modules and higher-level control blocks have been developed in VHDL, while some lower-level blocks have been developed in verilog. The majority of the individual modules have been tested and simulated using test benches in order to verify the correctness of the designs.
2.1.2 Leon3 Processor

The Leon3 is a 32-bit RISC SPARC V8 compliant processor targeted at System on Chip (SoC) designs owned by Gaisler Research [54] and developed for the space industry, with special emphasis on fault-tolerance aspects. It is easily customizable, so the processor can be tailored to have only the necessary peripherals and control blocks, improving the silicon space resources, power and performance. It is also manufacturer independent, which makes it a very flexible solution. The LEON3 has a fault-tolerant version, the LEON3FT [54], fully compatible with the basic version and with built-in functionality to detect and correct Single-Event Upset (SEU) errors in all on-chip memories, making it more robust to radiation that threatens the system integrity in harsh environments, such as in space applications.

It can be adjusted for various configurations like size of cache, memory, single or multiprocessor design, number of registers, interfaces for coprocessors, different technologies etc. which makes it a good candidate to develop an Application-Specific Instruction-set Processor (ASIP). The source code is open and free to use for educational purposes and the processor is a platform independent implementation. Other 32-bit RISC soft-core processors have been evaluated; however some alternatives, such as COFFEE RISC and OPEN RISC have been discarded due to unproven maturity and limited toolchain availability. Microblaze has a great set of tools integrated with the Xilinx toolchain, but was discarded due to the unavailability of the source code. LatticeMico32 [55] would also be a good candidate for the development, however the toolchain maturity, community support and documentation is somehow limited mainly because it is a relatively young design.

Table 2.1 presents a brief comparison between the presented soft-cores.

![Table 2.1: Soft-cores comparison](image)

<table>
<thead>
<tr>
<th></th>
<th>Coffee Risc</th>
<th>Open Risc</th>
<th>Leon3</th>
<th>MicroBlaze</th>
<th>LatticeMico32</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open-source</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes, except FPU</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Coprocessor Interface</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>FPU</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Fault-tolerance</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Vendor independent</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>JTAG Debug</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Although many of the proposed devices share many characteristics, the Leon pro-
cessor was considered the most mature, flexible and productive solution to develop a tailored SoC for MEMS applications, with the advantage of keeping the possibility to later create an ASIC and even explore the built-in fault-tolerance mechanisms. Some of the most decisive parameters for selecting the platform were the built-in debugging technologies, the proven maturity, open-source code and toolchain reliability. Also, the Leon has an implementation for most commercial RTOS, such as RTLinux, PikeOS, VxWorks and LynxOS [54]. The Table 2.2 shows the implementation resource usage for the base SoC system main components. The relatively small space occupied by a working processor keeps a lot of free space to design the remaining necessary application-specific peripherals, which in this case will include intensive digital filters that occupy a significant space.

<table>
<thead>
<tr>
<th></th>
<th>LUTs (%)</th>
<th>FFs (%)</th>
<th>BRAM (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core</td>
<td>12</td>
<td>7,7</td>
<td>15,7</td>
</tr>
<tr>
<td>Memory Ctrl</td>
<td>2,3</td>
<td>1,5</td>
<td>2,9</td>
</tr>
<tr>
<td>APB</td>
<td>1,2</td>
<td>0,2</td>
<td>0</td>
</tr>
<tr>
<td>AHB</td>
<td>0,7</td>
<td>0,1</td>
<td>0</td>
</tr>
<tr>
<td>Timer</td>
<td>1,6</td>
<td>0,3</td>
<td>0</td>
</tr>
</tbody>
</table>

From the performance standpoint, the Leon processor holds better results in comparison with other synthesizable CPU cores. An extensive comparison from both the resource usage and benchmark evaluations between Leon2 (which has a similar dhrystone benchmark performance), Microblaze and OpenRisc has been presented and analyzed in [56].

2.1.3 RTEMS RTOS

The events management latency and real-time performance of a Real-Time Operating System (RTOS) is critical for the control of MEMS devices. The hard real-time nature of some events, such as the pull-in makes it necessary to guarantee the prompt processing of such events. An RTOS is used to simplify tasks scheduling, intercommunication, priority and synchronization [57] and usually provides low-level access mechanisms to simplify the device programming, increase code portability, productivity and quality, by promoting the reuse of previously tested code.
With the recent improvements in embedded systems technology, the drawbacks of RTOS related to its memory and performance footprint are now much less significant than a few years ago. However, the use of an RTOS by itself doesn’t ensure the real-time response of a system. The developer is responsible for the understanding of the real-time concepts and apply them correctly using the mechanisms made available by the RTOS. There are several RTOS commercially available that vary significantly in their code size, determinism, responsiveness, tasks criticality management, memory management, peripheral and communication support, performance, etc. The most significant commercially available RTOS with porting for the LEON processor are:

- RTEMS
- eCos
- uCLinux
- Nucleos
- VxWorks
- ThreadX

In [58], a comparison study over the majority of these RTOS was presented. In this study the author compares several characteristics of RTOS, by the criteria and their importance perception for his application. Table 2.3 shows the evaluated parameters as well as the perceived importance to apply to MEMS control. Some items are more important than others, such as the processor performance, task scheduling preemptiveness, low interrupt latency and proper debug tools compatibility.

Some RTOS are more indicated for hard real-time systems, while others privilege flexibility over determinism, thus being more indicated for soft real-time systems. This is determined by the scheduling and interrupt policies allowed by the RTOS. The memory footprint and device driver architecture and support are also two important factors to account when selecting the RTOS. Although many of them share similar features, the RTEMS (Real-Time Executive for Multiprocessor Systems) was considered the more adequate solution, due to both its small footprint and its proven maturity. Besides, it is less complex than uCLinux and more flexible and standard oriented than smaller RTOS such as FreeRTOS.
Table 2.3: Selection Criteria Variables, Prescribes Value and Importance

<table>
<thead>
<tr>
<th>Criteria</th>
<th>Prescribed Value</th>
<th>Importance</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Processor</td>
<td>Leon3</td>
<td>high</td>
</tr>
<tr>
<td>2 Debug</td>
<td>kernel object aware</td>
<td>high</td>
</tr>
<tr>
<td>3 Scheduling algorithms</td>
<td>Priority based preemptive scheduling</td>
<td>high</td>
</tr>
<tr>
<td>4 Inter-task Communication</td>
<td>semaphore, mutex</td>
<td>high</td>
</tr>
<tr>
<td>5 Documentation</td>
<td>Porting guide</td>
<td>low</td>
</tr>
<tr>
<td>6 Portability</td>
<td>Lines of code</td>
<td>medium</td>
</tr>
<tr>
<td>7 Source Code</td>
<td>Available</td>
<td>high</td>
</tr>
<tr>
<td>8 Application Interface</td>
<td>POSIX and TRON</td>
<td>medium</td>
</tr>
<tr>
<td>9 Interrupt Latency</td>
<td>$&lt;50 \mu s$</td>
<td>high</td>
</tr>
<tr>
<td>10 Context Switch Latency</td>
<td>$&lt;50 \mu s$</td>
<td>high</td>
</tr>
<tr>
<td>11 Memory Footprint</td>
<td>$&lt;1$MB</td>
<td>medium</td>
</tr>
<tr>
<td>12 Licensing</td>
<td>Free</td>
<td>high</td>
</tr>
<tr>
<td>13 Community</td>
<td>Active</td>
<td>high</td>
</tr>
</tbody>
</table>

The RTEMS RTOS together with the Leon processor is used on an extensive list of mission-critical projects [59] such as [60]:

- ExoMars Rover Vehicle;
- Flight data recorders;
- Gaia space astrometry mission.

Some of its key features include [61]:

- Standards Compliant
- POSIX 1003.1b API including threads
- RTEID/ORKID based Classic API
- TCP/IP Stack
- High performance port of FreeBSD TCP/IP stack
- UDP, TCP
- ICMP, DHCP, RARP
- TFTP
- RPC
• FTPD
• HTTPD
• CORBA
• Debugging
• GNU debugger (gdb)
• DDD GUI interface to GDB
• Thread aware
• Debug over Ethernet
• Debug over Serial Port
• Filesystem Support
• In-Memory Filesystem (IMFS)
• TFTP Client Filesystem

Although we are only interested in some basic features, including debugging, serial port, task scheduling and event handling, it is relatively easy to integrate with other standard technologies and grow according to the necessities. As an example, the availability of the standard UART device driver allowed a simple processor instantiation on the Leon core, and a fast and robust integration. The use of peripherals requires the instantiation and mapping of the necessary hardware in the processor, creating a customized design to save space and power.

2.2 Zedboard Development Board

Even though the Leon soft-core is vendor independent, a port for the inexpensive Zedboard development board is available. The Zedboard holds a Zynq FPGA with a dual-core ARM processor. To keep the solution platform independent, a decision to keep the soft-core processor instead of the ARM processor was made. Since the PLL is controlled by the ARM processor, a script must be executed to initiate the ARM processor with the following configured clock rates:

• FPGA0_FREQ 70000000 - processor clock
• FPGA1_FREQ 200000000 - AMBA bus clock
• FPGA2_FREQ 250000000 - DAC clock
• FPGA3_FREQ 100000000 - ADC clock

2.3 Hardware Interface for MEMS Devices

The capacitive nature of the targeted MEMS devices requires a more complex acquisition circuit than its resistive counterpart. Besides, the circuit is quite often integrated in the same package to reduce the parasitic capacitance. The sensitivity, noise and temperature performance are key features that are enhanced with this kind of devices [62]. In broad terms, a structure will be controlled by using a complex digital controller with the possibility to add or remove hardware programmable modules, a displacement sensing circuit and an electrostatic actuation interface, as shown in 2.3.

In this case, the interface circuit for displacement measurement and for feedback electrostatic actuation is part of the work developed by [63]. The structure displacement measurement is based on a charge amplifier followed by a 40 MSPS ADC working at a sampling rate of 5 MSPS.

The electrostatic actuation must rely on a fast and precise voltage control. In this case, a board with 4 channels (only 2 are actually used) based on the AD5791 digital to analog converter (DAC) was used. This device is a 20 bits resolution converter capable of an update rate of $1.458\text{MHz}$ (maximum SPI clock of 35MHz) and voltage amplitude from -10V to +10V.

An image of the digital platform, where the main hardware blocks are identified
is presented in the Figure 2.4. The acquisition board is shown on the left side, the logic controller on center and the actuation board circuit on the right.

![Figure 2.4: Developed hardware solution](image)

The sensing circuit, shown in Figure 2.5, performs the signal demodulation digitally through a lock-in amplifier to gain an improvement in the system input noise and sensitivity performances over the traditional analog amplification approach. In this case, 1MHz square wave, generated in the FPGA is applied on the sensing electrodes to enable the capacity measurement using a charge amplifier and subsequent lock-in amplifier.

![Figure 2.5: Readout circuit for digital lock-in amplifier operation](image)

In this approach, the noise performance is approached right at the front-end through the implementation of a digital lock-in amplifier that extracts the signal from the 1MHz carrier frequency [64].

The actuation circuit used to perform electrostatic actuation on the devices parallel plate capacitors is shown in Figure 2.6. It is based on the AD5791 high-precision analog to digital converter controlled by the Serial Peripheral Interface (SPI). Before the actuation capacitor, a ultra-fast AD5791 analog switch is used to apply or remove the DAC output within 140ns. This feature is used for ultra-fast control situations, such as the force removal by the pull-in event or the sigma-delta commutation. In fact, the use of control techniques, requires a very stable and precise actuation voltage.
2.4 MEMS devices characteristics

The MEMS devices used for tests were manufactured using the commercial SOI-MUMPs process except for the L50 structure which was manufactured using a SOI-process over a 50µm wafer described in detail in [48].

They are based on a typical parallel-plate capacitive accelerometer with sensing and actuation electrodes. One of the structures used is shown in Figure 2.7. The actuation electrodes contain both comb-finger and parallel electrode types, although for the purpose of this work, only parallel types have been used. For the system characterization application, several different structures have been used to analyze the results over different structure types. In the sigma-delta application, an accelerometer named L50, with extra mass was used to accomplish higher sensitivities.

From a physical perspective, the structure can be considered a mass, spring and damping system, such as shown in the Figure 2.8:

The theoretical dimensions and characteristics such as the device resonant frequency ($F_r$), quality factor (Q) and rest capacitance can be computed by measuring the design dimensions. Table 2.4 contains the AS structure design parameters.
that are used as an example to compute the devices characteristics based on their physical dimensions.

Table 2.4: AS structure design physical properties

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>169x10^9 kg/m^2</td>
<td>young modulus</td>
</tr>
<tr>
<td>ρ</td>
<td>2350</td>
<td>silicon density</td>
</tr>
<tr>
<td>μ</td>
<td>1.82x10^-5 Pa.s</td>
<td>air viscosity at ambient temperature</td>
</tr>
<tr>
<td>ε₀</td>
<td>8.854x10^-12 F/m</td>
<td>air permittivity</td>
</tr>
<tr>
<td>wafer_thickness</td>
<td>25 μm</td>
<td></td>
</tr>
<tr>
<td>spring_l</td>
<td>[485, 462, 485]μm</td>
<td></td>
</tr>
<tr>
<td>spring_w</td>
<td>[4.5, 4.25, 4.5]μm</td>
<td></td>
</tr>
<tr>
<td>n_a×rms</td>
<td>19*4</td>
<td></td>
</tr>
<tr>
<td>n_sensing_arms</td>
<td>15*4</td>
<td></td>
</tr>
<tr>
<td>arms_width</td>
<td>500μm</td>
<td></td>
</tr>
<tr>
<td>d₀</td>
<td>2.25μm</td>
<td></td>
</tr>
<tr>
<td>mass_area</td>
<td>2.25μm</td>
<td></td>
</tr>
<tr>
<td>weight</td>
<td>mass * 9.8</td>
<td></td>
</tr>
</tbody>
</table>

For this type of springs, we can compute each spring constant as follows [65]:

\[
k = \frac{1}{\frac{spring\_l(1)^3}{12\times E\times I_1} + \frac{spring\_l(2)^3}{12\times E\times I_2} + \frac{spring\_l(3)^3}{12\times E\times I_3}} \tag{2.1}
\]

Where the second inertia moment (I) can be calculated as such:

\[
I = \frac{1}{12} \times spring\_w^3 \times wafer\_thickness \tag{2.2}
\]

The damping coefficient (b) is computed as follows:

\[
b = \frac{768 \times n\_arms \times air\_viscosity \times (wafer\_thickness \times arms\_width)^3}{\pi^6 \times d_0^3 \times (wafer\_thickness^2 + arms\_width^2)} \tag{2.3}
\]
The sensing capacity at rest can be calculated as:

\[
\text{rest\_sensing\_capacitance} = \frac{n\_sensing\_arms}{2 \epsilon_0 * \text{arms\_width} * \text{wafer\_thickness}}
\]

The same goes for the actuation capacity:

\[
\text{rest\_actuation\_capacitance} = \frac{n\_arms - n\_sensing\_arms}{2 \epsilon_0 * \text{arms\_width} * \text{wafer\_thickness}}
\]

Finally, the quality factor (Q) can be computed by the following expression:

\[
Q = \frac{\sqrt{k * m}}{b}
\]

The Table 2.5 holds a resume of the theoretical dimensions for each device.

<table>
<thead>
<tr>
<th>Device specifications</th>
<th>AS</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>NC</th>
<th>L50</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mass (m) [mg]</td>
<td>0.146</td>
<td>0.248</td>
<td>0.153</td>
<td>0.156</td>
<td>0.161</td>
<td>0.161</td>
<td>3.52</td>
</tr>
<tr>
<td>Mechanical spring (k) [N/m]</td>
<td>4.461</td>
<td>3.771</td>
<td>5.015</td>
<td>4.461</td>
<td>5.015</td>
<td>4.461</td>
<td>20.8</td>
</tr>
<tr>
<td>Zero-displacement gap (d0) [µm]</td>
<td>2.25</td>
<td>2.25</td>
<td>2.25</td>
<td>2.25</td>
<td>2.25</td>
<td>2.25</td>
<td>2.25</td>
</tr>
<tr>
<td>Natural resonant frequency (f0) [Hz]</td>
<td>870</td>
<td>620</td>
<td>910</td>
<td>850</td>
<td>888</td>
<td>837</td>
<td>385</td>
</tr>
<tr>
<td>Damping coefficient (b) [mN.s/m]</td>
<td>0.756</td>
<td>1.176</td>
<td>0.956</td>
<td>0.956</td>
<td>0.956</td>
<td>0.478</td>
<td>10.6</td>
</tr>
<tr>
<td>Sensing capacitance (Scap) [pF]</td>
<td>1.48</td>
<td>2.22</td>
<td>1.97</td>
<td>1.97</td>
<td>1.97</td>
<td>0.99</td>
<td>4.53</td>
</tr>
<tr>
<td>Actuation capacitance (Acap) [pF]</td>
<td>0.39</td>
<td>0.58</td>
<td>0.39</td>
<td>0.39</td>
<td>0.39</td>
<td>0.20</td>
<td>1.32</td>
</tr>
<tr>
<td>Quality factor (Q)</td>
<td>1.06</td>
<td>0.85</td>
<td>0.92</td>
<td>0.88</td>
<td>0.94</td>
<td>1.77</td>
<td>0.814</td>
</tr>
</tbody>
</table>
Chapter 3

SoC for Fast Prototyping of MEMS Control Systems

This chapter describes the developed system architecture that stands as a base for the solutions studied and presented in this work. The main features, the architecture, and the implementation details are described with emphasis on the base resources necessary to implement the proposed control applications.

3.1 Introduction

The architecture of a digital system is a crucial factor for the success of any real-time embedded application. Digital signal processor (DSP) applications typically have strict real-time constraints and the computation is quite often data intensive, with the demanding use of digital filters. Our interconnection and functional models ensure that configuration (managed by the programmability) is minimally intrusive, from a real-time performance perspective, on dedicated hardware. The architecture works as a fast prototype base for development of task specific modules to test new control routines and device behavior theories. The co-processors are mapped in the processor data space as a memory location so the data can be accessed using simple data pointers. Fig 3.1 shows the complete system processor, with the LEON3 processor basic components, and the multiple custom developed co-processor elements. Some elements are included or excluded on some setups to optimize the resource fingerprint.
3.1.1 Base System

The selection of functionalities that must be delegated to hardware is of the utmost importance in order to fulfill the timing constraints and allow a good flexibility. Some features have been developed as hardware modules, allowing the processor to perform the setup on the modules and the signal flow, and having interrupts to signal the processor on the detection of specific common events. The Fig 3.2 shows the complete system, with the FPGA elements as well as the physical elements, including the readout and actuation physical elements (ADC, charge amplifier and DAC). The base system is composed by the microprocessor, the hardware necessary for position sensing and for the electrostatic actuation.

The processor bus is divided into two buses technologies that are interconnected through a bridge: the advanced high-performance bus (AHB) and the advanced peripheral bus (APB). The main difference between the two protocols is that the AHB uses full-duplex parallel communications for fast and bulky memory access, while the APB privileges the I/O accesses. The APB is simpler, since there is no pipelining implemented, being ideal for peripherals with low bandwidth control.
access. Each developed hardware peripheral is connected through the AMBA APB bus and are memory mapped according to the Table 3.1.

3.1.2 ADC Controller

The ADC controller module allows the control and communication with the ADC at a 5 MHz signal acquisition rate. The ADC output is parallel with a data-ready output pin to drive the input register. Since the processor and the ADC data ready pin work at different clock rates, a digital synchronization circuit is necessary to avoid metastability events that commonly arise from developing circuits using different clock domains. The clock synchronization is based on a four-flip-flop synchronization scheme [66], shown in Figure 3.3, to transpose the signal into the processor clock domain and reduce considerably the probability of such an event to occur.
Table 3.1: Base system hardware modules memory and IRQ map

<table>
<thead>
<tr>
<th>Id</th>
<th>Unit</th>
<th>Address / IRQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>cpu0</td>
<td>Processor</td>
<td>AHB Master 0</td>
</tr>
<tr>
<td>ahbjtag0</td>
<td>JTAG Debug Link</td>
<td>AHB Master 1</td>
</tr>
<tr>
<td>rom0</td>
<td>AHB ROM</td>
<td>AHB: 000000000 - 00100000</td>
</tr>
<tr>
<td>apbmst0</td>
<td>AHB/APB Bridge</td>
<td>AHB: 800000000 - 80100000</td>
</tr>
<tr>
<td>dsu0</td>
<td>LEON3 Debug Support Unit</td>
<td>AHB: 900000000 - A0000000</td>
</tr>
<tr>
<td>mig0</td>
<td>DDR2 Controller</td>
<td>AHB: 400000000 - 50000000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>APB: 800000000 - 80000100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 2</td>
</tr>
<tr>
<td>irqmp0</td>
<td>Interrupt Controller</td>
<td>APB: 800002000 - 80000300</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 8</td>
</tr>
<tr>
<td>gptimer0</td>
<td>Timer Unit</td>
<td>APB: 800003000 - 80000400</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 8</td>
</tr>
<tr>
<td>uart1</td>
<td>Generic UART</td>
<td>APB: 800007000 - 80000800</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 3</td>
</tr>
<tr>
<td>gpio0</td>
<td>GPIO port</td>
<td>APB: 800006000 - 80000700</td>
</tr>
<tr>
<td>adev11</td>
<td>ADC Module</td>
<td>APB: 800008000 - 80001000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 11</td>
</tr>
<tr>
<td>adev12</td>
<td>DAC Module</td>
<td>APB: 800010000 - 80001800</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 13</td>
</tr>
<tr>
<td>adev13</td>
<td>Lock-in amplifier</td>
<td>APB: 80001A000 - 80001B00</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 15</td>
</tr>
<tr>
<td>ahbstat0</td>
<td>AHB Status Register</td>
<td>APB: 800004000 - 80000500</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 7</td>
</tr>
</tbody>
</table>

Figure 3.3: Flip-flop synchronization circuit to transpose the ADC data to the processor clock domain.
3.1.3 Lock-in Amplifier

The capacitive transduction in MEMS allows a higher sensitivity than a piezoresistive equivalent with the cost of a more complex electronic circuit [67]. The capacity measurement is then an important block in order to obtain the best displacement signal from the MEMS device. The MEMS platform was designed with a single analogue block, a charge amplifier, followed by a digital lock-in amplifier in order to maximize the signal to noise ratio (SNR) and allow a digital tuning of the amplifier gain and noise performance (through the implementation of digital filters). Since it consists on a digital multiplication and filtering, it eliminates the need for a noisier analog amplifier, and also enables digital tuning, as opposed to the fixed analog components of traditional amplifiers. The signal frequency is isolated and all the other frequencies are frequency-shifted and filtered out, making it suited for noisy environments.

The demonstrator application was built to measure a resonant frequency evaluation up to a few kHz. The signal acquisition is based on the MEMS capacitive changes, through a charge amplifier and as such, it is necessary to excite the charge amplifier with a 1 MHz signal (for a capacity of a few pF), allowing subsequent signal isolation through filtering. The acquisition frequency was set to 5 MHz, fulfilling the Nyquist requirements. Due to its tight synchronization and digital filtering requirements, the lock-in amplifier must be implemented in hardware. The ADC signal is multiplied with a synchronized 1 MHz modulation signal and follows a 70 kHz IIR low-pass filter (LPF) to extract the displacement signal from the modulated signal. The fact that the 1 MHz signal is generated inside the FPGA circuit allows a simple signal synchronization that would be harder to obtain if the signal was external (a phase locked loop would be required to synchronize the signal multiplication). Figure 3.4 shows the lock-in circuit scheme developed.

![Figure 3.4: Lock-in amplifier basic scheme.](image)

Since the capacitive excitation signal consists of a square-wave generated by the FPGA, a simple lock-in amplifier can be developed by multiplying the modulated
signal \( (V_{S\text{sin}}(w_{st} + \theta_{sig})) \) with the reference signal \( (V_{R\text{sin}}(w_{rt} + \theta_{ref})) \), obeying to the following equation:

\[
V_{\text{sig}}V_{\text{ref}} = V_S(t) \sin (w_{st} + \theta_{sig}) \ast V_R \sin (w_{rt} + \theta_{ref})
\] (3.1)

Which can be rewritten for an easier spectral lines identification:

\[
V_{\text{sig}}V_{\text{ref}} = \frac{1}{2} \ast V_S(t) \ast V_R \cos ([w_S - w_R]t + \theta_{sig} - \theta_{ref}) \\
- \frac{1}{2} \ast V_S(t) \ast V_R \cos ([w_S + w_R]t + \theta_{sig} - \theta_{ref})
\] (3.2)

In this case, the signals are synchronized \( (w_{S} = w_{R} = W) \), thus resulting in the following expression:

\[
V_{\text{sig}}V_{\text{ref}} = \frac{1}{2} \ast V_S(t) \ast V_R \cos (\theta_{sig} - \theta_{ref}) \\
- \frac{1}{2} \ast V_S(t) \ast V_R \cos (2Wt + \theta_{sig} - \theta_{ref})
\] (3.3)

Equation 3.3 shows the result of the multiplication of the modulated signal with the reference signal consists of a sum of two signals. Under normal conditions, the first part results in a DC signal \( (\theta_{sig} = \theta_{ref}; \cos(0) = 1) \) and the second part appears at a high frequency and is thus easily removed by the use of a Low-pass Filter (LPF). The use of a selective frequency improves significantly the Signal-to-noise Ratio (SNR) since the noise present in the entire spectrum is rejected by the signal multiplication.

Figure 3.5 shows the capacity variation for the lock-in version along the device linear range, at about 1/3 of the device displacement range [9]. The capacity variation was computed using Equation 3.4 that relates the capacity with structure displacement, where \( n \) is the number of capacitor arms, \( l \) is the arms length, \( t \) is the arms thickness, \( d_0 \) is the rest position gap between capacitor plates, \( \epsilon_0 \) is the air permittivity \( (8.854 \times 10^{-12}) \) and \( x \) is the measured displacement:

\[
C = \frac{n \ast \epsilon_0 \ast l \ast t}{d_0 - x}
\] (3.4)

The noise was measured with no actuation applied on the structure and keeping
the structure as still as possible over a period of 5 seconds. The noise value can be computed by the following equation:

$$Noise = \frac{\text{std}(\text{signal})}{\sqrt{f_{\text{cut}}}}$$ (3.5)

A total noise of $2.06 \mu V_{\text{rms}}/\sqrt{Hz}$ has been measured at the lock-in amplifier output setting the capacity detection limit of the system at $6.1 \mu F/\sqrt{Hz}$ and a linear output voltage slope of $338mV/pF$.

Due to performance and area constraints, the input signal and the sequence multiplication are performed using integer registers. The signal is multiplied at the 5 MHz sampling rate and after multiple experiments the following sequence was determined to produce the best outcome (the left one is synchronized with the output excitation signal):

$$1 \ 1 \ 0 \ -1 \ -1$$

In order to obtain a digitally amplified signal, the input signal and coefficients are pre-conditioned (the input signal is left-shifted 15 times, the filter b coefficients are left shifted 52 times and the a coefficients are left-shifted 32 times) in order to compute decimal values and obtain an amplified filter result with appropriate resolution. The structure displacement signal is then divided (right-shifted) according to the application configurable gain. The digital filter is a 6th-order IIR butterworth implementation based on a transposed direct form II filter with a
cascade of second order Biquad sections [68]. Figure 3.6 shows the implemented filter.

Figure 3.6: 6th order IIR filter based on a transposed direct form II cascade of Biquad sections

Figure 3.7 shows the filter frequency bode plots over the decimal coefficients, where the attenuation at 1MHz is 105dB and at 2MHz is 180dB. The DC gain is not zero because the coefficients are integer and thus, there is a constant gain applied. The signal is attenuated after the filter is applied using a configurable rotation.

Figure 3.7: Lock-in amplifier IIR filter frequency response
Finally, the low pass filter implements a signal prescaler to allow the subsampling of the original signal for subsequent signal processing on lower rates. A prescaler counter register is available through the ADC address space for that purpose.

### 3.1.4 Direct Digital Synthesizer

The digital synthesizer is an important FPGA hardware module responsible for the real-time generation of pre-established periodic signals in the output channels. It can be used to generate complex periodic signals without processor run-level intervention and allows the mechanical response analysis by the use of developed or customized detection mechanisms (such as the threshold/peak detection). It is based on an array of values that are set in the processor space, and can, after the configuration, be set to run automatically by the hardware controller, ensuring a real-time and precise behavior. This module is based on an array of 256 values of 20 bits each (each DAC channel word is 20-bits long) that represent the first of the four periodic signal quadrants that are correctly replicated in the remaining three quadrants. It also holds a register to apply a DC offset and allows the possibility to invert in each channel and a clock prescaler to adjust the frequency. The maximum frequency that can be applied at the output is then:

\[
F_{max} = \frac{70 \text{MHz}}{256 \times 4} \approx 68.3 \text{KHz} \quad (3.6)
\]

### 3.1.5 Actuation Controller

The Actuation Controller is responsible for the communication with the DAC channels implemented through a SPI protocol. It also allows a direct route between the digital synthesizer and the DAC, releasing the processor from performing that high frequency task. The actuation controller must allow the application of a constant DC value as well as a configurable sine wave output, that may be necessary to keep in synchronization with the second channel. It must also signal the DDS zero-cross event to the processor, and control the high-frequency switches position. Figure 3.8 shows the simplified actuation controller circuit in detail for one of the output channels where the three output signals paths are depicted (DDS, DC value or sigma-delta).
3.1.6 Threshold/Peak Detector

The threshold/peak detector is a module responsible for detecting events that allow the measurement of the structure properties and position. It has two operation modes. The first is a detector capable of measuring the delay between two subsequent threshold-cross events (useful for frequency measurement) and a peak detector that can be used to measure the signal amplitude of a movement. The Figure 3.9 shows the simplified developed circuit where several configuration registers can be used to define threshold detection points and the slope detection direction.

An internal timer counter (not represented in the figure) was added to measure the difference between subsequent threshold-cross events to improve the measurement precision that can be affected by the microprocessor interrupt latency and be read by the processor when an ISR is dispatched. The threshold-cross detector is particularly useful to detect pull-in events and signal the processor to promptly disable
the actuation switches, thus avoiding a counter-electrode collision and possible damages to the structure. The signal can be used to drive the actuation switches by using an AND logic operation inside the FPGA switches control circuit.

3.2 Closed-loop Control System

A closed loop control consists of using the measured sensor position to steer an actuation mechanism and continuously drive the proof mass to the rest position. The strength of the electrical output signal necessary to perform the operation provides the desired measurement. An increase on the device sensitivity is expected due to a significant reduction of the device deflection and nonlinear effects. On the other hand, the control system complexity is increased, thus making this a good candidate for testing the platform flexibility. Other methods can be used for closed-loop control such the basic on-off controller [9] classic proportional/integral/derivative controller (PID) [69], but the sigma-delta approach has been selected as a demonstrator since it requires challenging processing capabilities to
generate a high-order accelerometer structure. On the other hand, it can produce a straight digital output and achieve sub micro-g resolutions \cite{70}.

3.2.1 Lead-lag compensator

Every feedback system is in broad terms composed by a controller, a device and a feedback loop, as shown in Figure 3.10.

![Figure 3.10: Closed loop system control](image)

The lead-lag compensator is also necessary for other types of open-loop control systems \cite{71} or even other closed-loop control systems \cite{72}. In the case of MEMS devices, an effective loop delay is always existent due to the delay between an effective mass displacement and the measured feedback pulse. The nature of the closed-loop system is based on limit cycles that can exhibit low-frequency oscillations when the loop is improperly compensated \cite{73}. The compensator is therefore essential to achieve high in-band signal to quantization noise ratio (SQNR). Besides, the transfer function must contain a zero to compensate for the system phase delay. On the other hand, the zero produces a high gain at high frequencies and therefore, a pole must be also added to minimize this effect and obtain a unity gain output. The following transfer function describes the generic lead-lag compensator:

$$H_{\text{comp}}(S) = \frac{Ks + z_0}{s + p_0} \quad (3.7)$$

Using Tustin’s approximation, $s = \frac{2}{T} \frac{z-1}{z+1}$ becomes

$$\frac{U(z)}{E(z)} = \frac{(\frac{2k}{T} + kz_0)z + (kz_0 - \frac{2k}{T})}{(\frac{2}{T} + p_0)z + (p_0 - \frac{2}{T})} \quad (3.8)$$

Multiplying by $z^{-1}$ we have the following difference equation:
\[ U(z)(\frac{2}{T} + p_0) + U(z)z^{-1}(p_0 - \frac{2}{T}) = E(z)(\frac{2k}{T} + kz_0) + E(z)z^{-1}(kz_0 - \frac{2k}{T}) \] (3.9)

Solving for the discrete-time domain, results in the following difference equation to be implemented:

\[ u(k) = \frac{(\frac{2}{T} - p_0)u(k - 1)}{\frac{2}{T} + p_0} + \frac{(\frac{2k}{T} + kz_0)e(k)}{\frac{2}{T} + p_0} + \frac{(kz_0 - \frac{2k}{T})e(k - 1)}{\frac{2}{T} + p_0} \] (3.10)

The following generic equation is digitally implemented:

\[ u(k) = A \ast u(k - 1) + B \ast e(k) + C \ast e(k - 1) \] (3.11)

The A, B and C parameters can be software configurable to perform an algorithmic lookup for the best coefficients that minimize the loop oscillations for each individual structure properties and loop processing rate.

### 3.2.2 Multi-order Sigma-Delta

The control loop is based on the configurable multi-order sigma-delta architecture shown in Figure 3.11. The optimum sigma-delta gains for each device can be determined by a successive approach algorithm using the Matlab API to continuously change the gains and analyze the device sensitivity results by sampling the output signal through a hardware decimation filter.

![Figure 3.11: Closed loop system control](image-url)
3.3 Sampler

The use of a lock-in amplifier does not allow the direct evaluation of the structure displacement by means of an oscilloscope probe since the externally available signal is a frequency modulated signal. Also, since the DSP operations are performed inside the FPGA, it became necessary to access the displacement signal in several checkpoints along the signal flow. To accomplish these features and simplify the development, a sampler module was developed. The module contains a front multiplexer to select from different signals, a configurable prescaler and configurable-length buffer that can be increased or reduced to adapt to the available FPGA free space. In order to evaluate synchronized signals, the sampler can be used to store two signals, each in half of the buffer, ensuring the hardware synchronization for subsequent evaluation. In the case of the characterization, since a lengthy FIR filter is present, a 2048 samples array has been instantiated, while in the case of the sigma-delta application a 8191 bytes length buffer could fit in the available space. The signal reading is performed by setting the index and request the buffer index value, in a two-step read process, thus avoiding the re-mapping of the memory space.

3.4 Resources utilization

Table 3.2 shows a synthesis resources utilization resume of both the base system, the characterization system and the closed-loop control system applications. The base system with the processor uses only 18% of the available LUTs, while the closed-loop application, due to it’s higher order filters implementations got to a 82% LUT utilization. The memory LUTs usage is also increased due to the sampler buffer length instantiated.

This high utilization percent begins to saturate the FPGA routing efficiency, creating lengthier routes and sacrificing timing constraints as well as synthesization time.
### Table 3.2: Synthesis results for the sigma-delta control application

<table>
<thead>
<tr>
<th>Synthesis results</th>
<th>Base System (%)</th>
<th>Characterization System (%)</th>
<th>Closed-loop control system (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF</td>
<td>5</td>
<td>16</td>
<td>15</td>
</tr>
<tr>
<td>LUT</td>
<td>18</td>
<td>52</td>
<td>82</td>
</tr>
<tr>
<td>Memory LUT</td>
<td>1</td>
<td>33</td>
<td>65</td>
</tr>
<tr>
<td>BRAM</td>
<td>13</td>
<td>13</td>
<td>13</td>
</tr>
<tr>
<td>DSP48</td>
<td>2</td>
<td>22</td>
<td>54</td>
</tr>
<tr>
<td>BUFG</td>
<td>16</td>
<td>13</td>
<td>13</td>
</tr>
</tbody>
</table>

Clock Frequency: 70Mz
Chapter 4

Devices Characterization

Test and characterization of MicroElectroMechanical Systems (MEMS) is an important step during the development and production phases, and should be as fast and reliable as possible [74].

The current optical and mechanical tests for MEMS characterization, although precise, are not well suited for a fast, full-wafer diagnosis. The use of electrical stimulus, using fully electrical test can provide a fast, cost-wise and easy to adjust system as a step forward on MEMS testing and characterization automation and cost reduction.

The current approaches for early detecting manufacturing issues are largely based on testing and sampling random wafer structures. Since the process is slow, a full-wafer test is expensive and time consuming [75].

The electrical test is a technique initially borrowed from the traditional IC industry, in which a microprobe is used to inject electrical signals to the structure and another probe is used to measure the resulting electrical signal from which some mechanical properties can be derived. The low-latency possibilities offered by this technique [14][24], the possibility to test a large sensitivity range of devices [15] and the non-need to use costly mechanical stimulation are good arguments to develop this approach.

In this chapter, the digital solution to test and characterize MEMS structures, using the built-in electrostatic actuation mechanisms, is presented. The dedicated digital system is responsible for the excitation, measurements, filtering and real-time control loops necessary for the analysis of the MEMS devices greatly
increasing speed and flexibility of the test.

The system enables measurement of resonant frequency (Fr), quality factor (Q) and pull-in voltages (Vpi) and was tested on individual MEMS, as well as with a semi-automated probe station for testing and characterization of MEMS at the wafer-level. The detection and evaluation of process dependent variables, like over-etching in the production cycle are analyzed.

The chapter is divided in 4 sections. After an Introduction, the design and implementation of the digital platform is presented in the second section. In the third section, MEMS characterization results are presented for both individual MEMS and wafer-level testing. Finally, some conclusions are presented regarding the suitability of the presented approach for MEMS testing, characterization and process monitoring.

4.1 Introduction

The digital platform for MEMS evaluation presented here is a fully electrical characterization solution for electrostatically actuated MEMS accelerometers with capacitive readout (it can nevertheless be easily adapted to other transduction mechanism, by changing the readout block).

The core principle is the ability to use electrostatic actuation on the structure actuation electrodes and then evaluate the structure displacement by measuring the capacity variations through a charge amplifier. Figure 4.1 presents a picture of one of the used MEMS inertial sensors, clearly showing the electrodes used to electrostatically actuate on the structure (enabling bi-directional actuation) and the sensing electrodes in the middle region.

It has already been demonstrated that inertial MEMS sensors can be fully described by their resonant frequencies (Fr), quality factors (Q) and pull-in voltages (Vpi) [76], [3]. In addition, these characteristics can also be used to access process related variations like over-etching and material properties (Young’s Modulus and density for instance). These are key device characteristics and their fast and accurate measurement can be very important for both MEMS designers (to evaluate device performance during the design phase) and for process monitoring and/or process development and therefore, the MEMS testing and characterization prober presented here aims the acquisition of this parameters using a fast and reliable ar-
chitecture.

Although the system was developed to test one-axis electrostatically actuated capacitive accelerometers, the digital system can be adapted to other types of devices that can be electrically stimulated by programming the specific digital circuits.

![Capacitive MEMS sensor with sensing and actuation electrodes highlighted areas](image)

Figure 4.1: Capacitive MEMS sensor with sensing and actuation electrodes highlighted areas

The digital solution, schematically presented in Figure 4.2, uses the ADC converter and the charge amplifier to convert the device capacitive changes to voltage (the only analogue circuit), a central processing unit and a 2-channel DAC board to inject signals. The digital processing system is developed and implemented in an FPGA (Field Programmable Gate Array), using the Leon 3 soft-core microprocessor [77], along with custom-designed peripherals enabling true parallel and deterministic behavior, necessary to meet the application requirements for fast and accurate testing. The interrupt driven nature of the digital peripherals allow for true parallel real-time processing capabilities and scalability because it lays on the hardware for the heavy processing that a software system cannot attend.

Due to the system flexibility, based on a soft-core microprocessor, other measurements (besides the resonant frequency, quality factor and pull-in voltages) can easily be implemented and added to the system by programming the microprocessor. The digital blocks, implemented in hardware, are presented next. While the blocks that are responsible for the MEMS characteristics acquisition (pull-in measurement, resonant frequency measurement and quality factor measurement) are novel and advance the state-of-the-art in the field, the remaining blocks, although important (like the lock-in and filters) are just implementations of existing technologies/methodologies.
4.2 Process and Device Main Uncertainties

The step that defines the mechanical structure on typical MEMS processes (surface, bulk and SOI) is critical, since any process tolerances can influence the device dimensions and therefore the sensor characteristics. Figure 4.3 depicts the typical Deep Reactive Ion Etching (DRIE) process deviations namely, over-etching, notch, scalloping and gaps mismatch. The reasons for these non-idealities and consequences are addressed next.

A common occurring phenomenon in DRIE is over-etching (undercut). A hard-mask or photoresist mask is used during the DRIE process and due to the scattering of radicals and chemical reaction with silicon during the etching-phase a slight over-etch occurs under the mask. The two phases process (etching and passivation) also give origin to scalloping (visible on the waviness of the sidewalls). Over-etching is critical for device dimensions and becomes substantial for smaller gaps. Over-etch can be as large as 10% of the gap which for 2µm gaps can be a very large deviation and completely change the devices characteristics (resonant frequencies can be affected in excess of 20% due to over-etching)[3]. Another recurrent phenomenon is notching. It is widely accepted that charging at the oxide interface results in breakdown of the passivation layer at the trench foot resulting in lateral etching (notching). This effect can generate wider gaps and slightly modify the mechanical and electrical characteristics of the device. It’s nevertheless as critical as over-etching. It is also common that due to tolerances, there are gaps mismatches along the device. This is particularly important when differential capacitive transduction
is used, since the initial gaps will have slightly different values, resulting in offset. This offset can be compensated by the readout electronics. In terms of mechanical performance, the mismatch does not influence the mechanical characteristics and therefore, the sensor performance (rather than the offset already mentioned).

### 4.2.1 Pull-in Phenomenon

Pull-in voltages are an important characteristic of parallel-plate electrostatic actuators and can be used for device characterization [76]. The pull-in voltage is usually measured by looking at the device displacement while increasing the actuation voltage from zero until an abrupt change is detected. The electrostatic force is inversely proportional to the square of the displacement, while the counteracting elastic force is proportional to the displacement. Equation 4.1 determines the structure pull-in voltage in terms of the spring elastic constant ($k$), the zero displacement gap ($d_0$), the air permittivity ($\varepsilon_0 = 8.8546 \times 10^{-12}$) and the plates total length ($l$) and width ($w$):

$$V_{pi} = \sqrt{\frac{1}{2} \frac{d_0^3 k}{\varepsilon_0 w l}}$$

(4.1)
The voltage at which this abrupt change is detected corresponds to the pull-in voltage. It is therefore clear that the resolution of the measurement depends on the resolution used for the actuation voltage control, which is typically much more accurate and inexpensive to perform. Figure 4.4 shows a real pull-in event in response to an ramp voltage applied to the structure. It is evident the fast nature of the pull-in event (in less than 100µs the structure can hit the counter electrodes) and the necessity to detect the event directly in the hardware, using high frequency mechanisms that provide the necessary deterministic features.

Figure 4.4: Pull-in phenomenon on a structure with the application of a voltage ramp

4.2.2 Resonant Frequency on 2nd Order Systems

The resonant frequency is a property of second order mechanical systems and can be described as the frequency at which the system naturally vibrates when put into motion, very specific to the system unique physical properties. It offers valuable insight into the MEMS manufacturing process repeatability. Figure 4.5 shows an example of some devices frequency response bode plots. The resonant frequency can be recognized by the maximum amplitude gain but also by the 90° phase shift that occurs.
4.2.3 Quality Factor

The quality factor represents the measurement of energy dissipation in a linear-circuit element and defined as the maximum energy stored during a cycle divided by the energy lost per cycle [78]. In another words, it is a measurement of how under-damped a second order system is. It can be calculated by measuring the response amplitude to a signal at the resonant frequency (where the maximum amplitude occurs) and divide it by the amplitude at a close to steady-state condition, as shown in Equation 4.2.

\[ Q = \frac{w_f}{w_0} \]  

The MEMS devices quality factor can vary from values under 1, such as in common accelerometers up to many thousands, such as in gyroscopes, where the device is placed in a vacuum sealed package to attain those high values essential to the device functioning.
4.3 Digital Signal Processing

4.3.1 Pass-Band Digital Filter

Taking advantage of the FPGA parallel computing capabilities, a 70th order finite impulse response (FIR) filter is built to allow filtering the lock-in output signal according to the detection routine necessities. The processor can then perform a setup for the FIR coefficients. For instance, a band-pass \((F_{c1} = 0.023; F_{c2} = 0.067; Ap=1\text{db}; Ast=-60\text{db})\) was designed and used during the resonant frequency search procedure. Figure 4.6 shows the implemented filter block diagram and Figure 4.7 shows the bode plot for the filter response to the normalized frequency, where the DC voltage is rejected and the band-pass gain is close to 0 dB.

The filter has a built-in sample prescaler that enables an easy filter parameters adjustment by changing the sampling frequency, therefore enabling the change of the band-pass region along the frequency domain, avoiding changing the filter characteristics. This allows for a faster analysis, a predictable filter behavior as well as a constant filter delay.

The filter phase delay was measured by applying a low frequency sine wave (structure delay \(\approx 0\)) on the structure and measuring the delay between the DAC zero-cross event and the measured ADC zero-cross event.

The delay is measured between the zero-cross events instead of peak values because the structure signal is more stable (where the structure velocity is maximum) and accurate in the zero-cross region than in the peaks region.

![70th order FIR filter block diagram](image)

Figure 4.6: 70th order FIR filter block diagram

This FIR filter was used in the characterization application due to its inherent permanent stability. It should be noted however that the use of the IIR filter improves the space and performance, since it requires a smaller order filter to accomplish the same attenuation. The recursive nature of the IIR filter makes it unstable under certain conditions, and therefore, that condition must be analyzed.
4.3.2 Peak/Threshold Detector

The programmable peak or threshold value detector with interrupt capabilities is available to the processing system. This peripheral is used to detect the movement peaks, which is then used to measure the structure delay.

The threshold detector is used to detect the pull-in voltage and promptly notify the processor to take the actions (in this case to remove actuation) in order to avoid collisions.

Figure 4.8 shows a real example, where a device was actuated with a 50 Hz sine wave and the phase delay computed based on the delay between the applied signal and measured signal zero cross instants. Using the real-time approach of the proposed architecture, every actuation cycle results in a phase measurement outcome with minimal processor effort (the processor workload has been measured to be below 4% in this measurement stage).

4.4 Pull-in Measurement

Ramp Approach

In order to have an acceptable resolution (1mV resolution as used in [3]), pull-in voltages are measured by applying three consecutive ramps with increasing resolution (500mV, 40mV and 1mV) as demonstrated in the fluxogram presented in the Figure 4.9. The three steps ramp can be easily identified as the three hori-
Such approach allows the algorithm to jump with a larger resolution to a point closer to the pull-in voltage. This feature strongly speeds up the pull-in voltage measurement (if a 1mV ramp would be used from zero until pull-in is detected, the required time to measure pull-in would be considerable more). This procedure is repeated at least twice for each side to increase robustness, i.e., only after two consecutive similar pull-in voltages are measured, the measured pull-in voltage is considered valid.

Another key feature of this block is the displacement detector that prevents the device from hitting the counter-electrodes. During pull-in measurements, the peak/threshold detector is programmed to trigger an interrupt on the processor when the device displacement is larger than 1/3 of the gap (when pull-in occurs). When the interrupt is triggered, the microcontroller switches off the actuation voltage and the device returns to its rest position, preventing it from hitting the stoppers. This interrupt also informs the microcontroller that pull-in was detected and the voltage applied is stored as the corresponding pull-in voltage.

Figure 4.10 shows a real example of the described ramp generation method with the pull-in detection points highlighted and where the delay between the detection and the voltage removal, which is 1 ms long can be seen.
Figure 4.9: Pull-in ramps generation and measurement fluxogram

Figure 4.10: Pull-in ramp with highlighted detection points. The immediate actuation voltage removal is evident to avoid hitting the counter electrodes

Accessing the Detection Values

The theoretical pull-in voltage is easy to compute by evaluating the designed structure physical characteristics. This value however can vary due to manufacture tolerances and/or deviations. The presence of a lock-in amplifier does not allow the capture through an oscilloscope and determine the threshold value limits to be established in order to perform a correct measurement. The solution found was to use the high-level Matlab scripting features to perform a small routine and increase the threshold value in small steps until no significant variation is detected,
as shown in the Listing 4.1:

Listing 4.1: Pull-in measurement threshold detection

```matlab
prev_left_val = 0;
prev_right_val = 0;
i = 0;
max_voltage = 6.0; \% theoretical limit for this structure
for voltage= 0.5:0.05:5.0 %voltage step
i = i + 1;
left_pi_det = -voltage;
right_pi_det = voltage;
pi = pull_in(uart, left_pi_det, right_pi_det, max_voltage);
if pi.success && prev_left_val < pi.lft_pi &&
    prev_right_val < pi.rgt_pi
    fprintf('values: lft: \%.2f | rgt: \%.2f', pi.lft_pi, pi.rgt_pi);
end
end
```

Statistic Distribution

A set of 1000 measurements was performed with the AS5 structure to analyze the process repeatability and measurement deviations. Figure 4.11 shows the resulting graphic distribution where a measurement with 1mV of precision is performed with a very small standard deviation outcome (std = 0.0004 for the left displacement and 0.0008 for the right displacement pull-in voltage).

![Pull-in measurement statistical distribution over 1000 samples](image)

Figure 4.11: Pull-in measurement statistical distribution over 1000 samples

The measurement time was also evaluated and the result is shown in Figure 4.12.
The majority of samples are retrieved in 0.6s. The variation is due to noise disturbances when the device is near the pull-in point, causing an invalid measurement and the necessity to repeat the actuation ramp.

![Pull-in time measurement distribution](image)

Figure 4.12: Pull-in time measurement distribution.

### 4.5 Resonant Frequency Measurement

This characteristic of 2nd order systems poses that at resonant, the system output is $90^\circ$ phased-sifted with the input. From the point of view of measurement, the phase shift is easier and more accurate to detect than the peak amplitude gain shown in the example bod plot example of Figure 4.5.

In this characterization stage, the resonant frequency is measured by applying a sine wave at a known frequency on one of the structure actuation electrodes while the other side actuation electrode is actuated in phase opposition (both sine waves have a positive DC offset) [79].

For a parallel plate capacitor, the electrostatic force is given by:

$$F = \frac{\epsilon AV^2}{2d^2}$$  \hspace{1cm} (4.3)

The application of a sine wave with a fixed amplitude and offset on one actuation electrode and the same signal with inverted phase in the opposite electrode, results in a displacement with the same frequency than the input. The forces balance equations are described by the following equations:
Applying the electrostatic force equation, where \( o_1 \) and \( o_2 \) are the offset values and \( a_1 \) and \( a_2 \) are the amplitude values, we get:

\[
x = \frac{\epsilon A}{2kd^2} \left[ (o_1 + a_1 \sin(w_1 t))^2 - (o_2 + a_2 \sin(w_2 t + \pi))^2 \right]
\] (4.5)

Unrolling the square terms we have:

\[
x = \frac{\epsilon A}{2kd^2} \left[ \frac{1}{2} (-a_1 \cos(2w_1 t) + a_1^2 + 4a_1 o_1 \sin(w_1 t) + 2o_1^2) \right. \\
- \frac{1}{2} (-a_2 \cos(2w_2 t) + a_2^2 + 4a_2 o_2 \sin(w_2 t) + 2o_2^2) \right]
\] (4.6)

By applying the same offset and amplitude to both signals, some terms cancel themselves and we get:

\[
x = \frac{2\epsilon A}{kd^2} (a \sin(w t))
\] (4.7)

As the expression shows, this configuration enables to move the structure with a frequency equal to the one applied eliminating the squared terms from the electrostatic force.

Since the device frequency displacement is known, the digital band-pass filter is then digitally adjusted to the actuation frequency, strongly eliminating noise, and the phase difference between actuation and displacement is measured. This procedure can be performed for several frequencies to retrieve the device bode plot, but since the goal is to have a fast characterization setup, a proportional controller (Figure 4.13) was implemented that automatically adjusts the applied frequency (and filter parameters) until a 90° phase shift is achieved (at the resonant frequency). The resonance frequency measurement is shown in the Figure 4.14 fluxogram, where the asynchronous ADC zero cross event after the filter, essential to perform the phase measurement for any given frequency is shown.

The use of the controller is critical, for a fast determination of the resonant frequency.
In this procedure, the zero-cross event was used instead of the peak event detection, since the structure velocity is higher at that point and thus, the signal presents less noise.

Figure 4.13: Resonant frequency proportional controller blocks.

![Resonant frequency proportional controller blocks](image)

Figure 4.14: Resonant frequency measurement fluxogram.

![Resonant frequency measurement fluxogram](image)

### 4.5.1 Step Response Analysis

As already stated in Section 1, the manufacturing variations result in an uncertainty of the device exact parameters, hence the resonant frequency can vary significantly from the expected design value. In order to evaluate the real resonant structure frequency, a step voltage was applied and a second order response fit-
ting was performed to manually obtain a real measurement and compare with the outcome. The peak overshoot is given by:

\[
M_p = \frac{y_{\text{peak}} - y_{\text{DC}}}{y_{\text{DC}}} = \frac{0.0354 - 0.025}{0.025} = 0.416
\]  

(4.8)

In an underdamped system, the peak overshoot is expressed in function of the damping ratio by:

\[
M_p = e^{-\frac{\pi\zeta}{\sqrt{1 - \zeta^2}}}
\]  

(4.9)

Which in terms of \( \zeta \) is expressed as:

\[
\zeta = \sqrt{\frac{\ln^2 M_p}{\ln^2 M_p + \pi^2}} = 0.2689
\]  

(4.10)

The undamped natural frequency is given by the following approximation:

\[
w_n = 2\pi \frac{1}{t_{\text{second\_peak}} - t_{\text{first\_peak}}} = 2\pi \frac{1}{0.00221 - 0.00072} = 4217 \text{rad/s}
\]  

(4.11)

The resonant frequency is related to the undamped natural frequency by:

\[
w_n = \frac{w_d}{\sqrt{1 - \zeta^2}}
\]  

(4.12)

Replacing \( w = 2\pi f \) we can compute the resonant frequency:

\[
f_{\text{res}} = \frac{w_n \sqrt{1 - 2\zeta^2}}{2\pi} = \frac{4378 \sqrt{1 - 2 \times 0.2689^2}}{2\pi} \approx 644 \text{Hz}
\]  

(4.13)

Figure 4.15 shows the measured device step response and the second order fitting using the above method. It clearly shows that the resonant frequency is about 644Hz.
4.5.2 Resonant Frequency Amplitude Analysis

The sine wave amplitude applied to the structure will have an impact on the measured resonant frequency value. The AS structure resonant frequency measurement outcome in function of the excitation wave amplitude is shown in Figure 4.16.

This phenomenon has been described in the literature as the negative spring effect of parallel plate actuators \([80] [81] [82] [83]\). At resonance, the spring elastic
constant is defined by [83]:

\[ k_{\text{net}} = k - V^2 \frac{C_0}{x_0^2} \left( \frac{1}{(1 - x_e(V)/x_0)^3} \right) \]  

(4.14)

Where \( x_e \) is a function of the excitation voltage \( V \) (\( x_e \) increases with \( V \)), which in its turn decreases the total spring constant, resulting in a smaller resonant frequency measurement outcome.

### Statistic Distribution

A set of 1000 measurements was performed on the AS5 structure to verify the measurement consistency. The Figure 4.17 shows the measurement results (the initial lookup value was set to 400Hz). Since the AS device pull-in value is about 5.5V, a 3V amplitude and 0.75V offset voltage were used to stay out of the pull-in zone, resulting in a resonant frequency mean value of 620Hz, which is consistent with the Figure 4.16 data. The standard variation is 2.89, which can be improved at the expense of a smaller tolerance between confirmation measurements, and therefore, a larger sampling time.

The time analysis results are shown in Figure 4.18. The time variation is higher than the pull-in due to the set tolerance between subsequent measurements (it takes at least 5 measurements), but the mean time is still quite small (0.31 seconds).

It is also important to notice that the initial lookup frequency is already set at 400Hz and that devices with smaller resonant frequencies will need more measurement time because the oscillation period is obviously higher (a measurement at 200Hz will require the double amount of time than to perform a phase measurement at 400Hz).

### 4.6 Quality Factor

This characteristic of each second order mechanical system is used to measure a device performance and serves as a comparison mark between similar devices [84]. The AS5 structure quality factor was manually assessed using the sampler module to acquire the displacement at the lock-in filter output in order to compare against
Figure 4.17: Resonant frequency measurement statistical distribution over 1000 samples.

Figure 4.18: Resonant frequency measurement time statistical distribution over 1000 samples.
4.6.1 Manual Measurement of Quality Factor

The quality factor was measured by applying a 62Hz and a 620Hz (resonant frequency) sine wave with the actuation method used for the resonant frequency evaluation and measured the peak. In this case, a signal with 3V of amplitude and 0.75V of offset was set (the evaluation is performed in Section 4.6.2). The fluxogram shown in the Figure 4.19 describes the processor implemented algorithm with the hardware specific features, such as the ADC Peak detect ISR.

The quality factor sine wave voltage amplitude must be small in order to comply with the amplitude considerations described in section 4.5.2. The Figure 4.20 shows the structure response to a resonant frequency signal as well as to a low amplitude signal \( f = F_{res}/10 \) Hz, where the phase delay is considered to be minimal. The manually measured quality factor is then:

\[
Q_{\text{manual}} = \frac{0.016}{0.01} = 1.6
\]
4.6.2 Quality factor amplitude analysis

The AS structure quality factor measurement in function of the excitation wave amplitude is shown in Figure 4.21.

It is evident from results shown in Figure 4.21 that the measurement value is more accurate when using a smaller amplitude signal due to the damping effect that attenuates the signal amplitude on higher displacements.

A small excitation value will provide a more accurate result because the electrostatic force amplitude is related to the structure displacement amplitude and a
bigger displacement will increase the damping force impact.

**Statistic Distribution**

The measurement of 1000 samples was also performed to evaluate the quality factor repeatability and the results are shown in Figure 4.23 and in the Figure 4.24. The mean value is 1.67 and the mean measurement time is 0.47 seconds, but in this case, the evaluation time variation is significantly higher because the measurement is performed on the peaks, where the noise disturbances are higher, and since the algorithm performs multiple samples (represented in the Figure 4.19 by the variable $N_{samples}$), more samples are necessary to achieve a result with a good tolerance level (for simplicity, the samples comparison is not shown in the Figure 4.19, but samples that diverge significantly will be discarded and new ones will be acquired, increasing the sampling time).

![Figure 4.23: Quality factor measurement statistical distribution over 1000 samples.](image)
4.7 Solution Memory Map

Table 4.2 presents the processor peripherals, their respective addresses and interrupt addresses. The phase detector and the filter (not mapped in the bus) are the only modules necessary to build from the base platform to perform the measurement specific features, namely the peak and zero cross events. A pull-in detection mechanism feature was also developed inside the ADC module to optionally remove the actuation by hardware when a movement threshold is crossed.

4.8 Wafer-level Testing

Testing and characterization at the wafer-level is very important since relevant information regarding the process variability within the same batch, and critical information about the process (that can later be used to improve the design) can be derived. Therefore, the availability of a fast and reliable characterization system for MEMS at the wafer-level can be of outmost importance during the development phase (device design and process development), but also for production
Table 4.2: Characterization system hardware modules memory and IRQ map

<table>
<thead>
<tr>
<th>Id</th>
<th>Unit</th>
<th>Address / IRQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>cpu0</td>
<td>Processor</td>
<td>AHB Master 0</td>
</tr>
<tr>
<td>ahbjtag0</td>
<td>JTAG Debug Link</td>
<td>AHB Master 1</td>
</tr>
<tr>
<td>rom0</td>
<td>AHB ROM</td>
<td>AHB: 000000000 - 00100000</td>
</tr>
<tr>
<td>apbmst0</td>
<td>AHB/APB Bridge</td>
<td>AHB: 800000000 - 80100000</td>
</tr>
<tr>
<td>dsu0</td>
<td>LEON3 Debug Support Unit</td>
<td>AHB: 900000000 - A0000000</td>
</tr>
<tr>
<td>mig0</td>
<td>DDR2 Controller</td>
<td>AHB: 400000000 - 500000000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>APB: 800000000 - 800001000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 2</td>
</tr>
<tr>
<td>uart0</td>
<td>Generic UART</td>
<td>APB: 800001000 - 80000200</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 2</td>
</tr>
<tr>
<td>irqmp0</td>
<td>Interrupt Controller</td>
<td>APB: 800003000 - 80000400</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 8</td>
</tr>
<tr>
<td>gptimer0</td>
<td>Timer Unit</td>
<td>APB: 800006000 - 800007000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 12</td>
</tr>
<tr>
<td>gpio0</td>
<td>GPIO port</td>
<td>APB: 800005000 - 800006000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 13</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 7</td>
</tr>
</tbody>
</table>

and calibration. The digital platform developed was used to perform tests at the wafer-level. A 200mm processed SOI (25µm active layer) wafer containing 420 MEMS devices (with 5 very similar layouts, M1 to M5 distributed in 21 reticules as shown in Figure 4.25) was tested using a semi-automated probe station (Figure 4.26). Electrical probes were used to connect the MEMS actuation electrodes and the sensing capacitors to the digital platform. The existing control software for the probe station allows loading the testing points along the wafer, but since the software is closed (does not enable external triggering), it was not possible to link the probe station control software with the digital platform RS-232 serial interface. Therefore, every time a new position was available for test, a manual input was required to start the MEMS testing which strongly increased the total testing time. For the wafer-level testing, a new simple routine to check if the device is
good or faulty was added to the digital testing platform, prior to the characterization of the resonant frequency, quality factor and pull-in voltage. This routine applies a known excitation voltage while checking the device displacement. In case the device moves above a pre-defined threshold (meaning the device is moving), it performs the remaining characterization, otherwise passes to the next device and signals the device as faulty.

Figure 4.25: 200 mm processed SOI wafer with 21 reticules (420 DUT). Each reticule contains 20 MEMS devices (5 different configurations, M1 to M5).

Figure 4.26: Semi-automated probe during wafer-level testing.
4.8.1 Wafer-level Testing Results

For all the tested 420 DUTs, data was recorded regarding the device status (good or faulty), and the measured mechanical characteristics (resonant frequency, quality factor and pull-in voltage) for the good devices. The information was then post-processed in order to analyze process variability and process characteristics like over-etching. For the calculation of the process over-etch, the methodology presented in [3] and in [85] was used. The method relies on accurate device models that include process variables (like over-etching). The measured data is then introduced in the models enabling to retrieve the process variables. The first analysis performed with the measured data was an yield analysis and location of the good DUTs within the wafer (see Figure 4.27). For the wafer analyzed, a global yield of 48.3% was obtained.

![Figure 4.27: Results from the wafer-level testing process yield.](image)

Next, the process variability for the measured characteristics was plotted for the 5 different layouts (M1 to M5). The cumulative distribution curves for the several parameters, average values and standard deviation are presented in Figure 4.28. Overall, the measured parameters follow a Gaussian distribution within the wafer and the small differences among the 5 different layouts are captured by the values measured.

For comparison, the expected characteristics for the 5 different layouts are presented in Table 4.3, assuming a $1 \mu m$ over-etch, and are in good agreement (in average) with the measured values. Process uniformities around 30%, 60% and
20% are found for the several layouts regarding the resonant frequencies, quality factor and initial capacitance values respectively.

Table 4.3: Expected parameters of devices M1 to M5 based on layout assuming 1µm over-etch

<table>
<thead>
<tr>
<th>Device</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Fr</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Expected resonant frequency (Fr) [Hz]</td>
<td>4794</td>
<td>4687</td>
<td>4793</td>
<td>4853</td>
<td>4751</td>
</tr>
<tr>
<td>Expected quality factor (Q)</td>
<td>3.17</td>
<td>3.37</td>
<td>3.39</td>
<td>3.36</td>
<td>3.57</td>
</tr>
<tr>
<td>Expected initial capacitance (C0) [pF]</td>
<td>1.10</td>
<td>1.06</td>
<td>1.09</td>
<td>1.14</td>
<td>1.11</td>
</tr>
</tbody>
</table>

Finally, the process over-etching was estimated for each device and based on the device location within the wafer, an over-etching map was created as shown in Figure 4.29. An average over-etch of 840nm was estimated from the measurements.
Figure 4.29: Over-etch wafer map.
Chapter 5

Sigma-Delta Controller

This chapter presents the Sigma-Delta application developed on the base platform to find the optimum gains and evaluate multiple orders and configurations on two different MEMS structures. It starts with an introduction on the sigma-delta working principle and then a description of the solution developed to create a multi-order, configurable solution for fast assessment of structures control gains. Some real examples are presented for all the possible orders and an evaluation on the sensitivity and bandwidth tradeoffs are performed.

5.1 Introduction

The traditional and simplest sensor measurement techniques are based on an open-loop approach where a physical change in the transducer is measured by electrical means for subsequent processing and interpretation. The closed-loop approach on the other hand delegates on the electronics the responsibility for the precision improvement and quite often still allows a relaxation on the manufactured device specifications [29]. This different paradigm brings with it a demand for better and more complex electronic circuits to achieve state-of-the-art performances. The small nature of MEMS add an extra complexity when compared to traditional mechanical systems, because they pose extra computational requirements due to limited availability of sensor data, the fast sensor and actuator dynamics and noise associated with them [30]. The sigma-delta modulator was first developed as an ADC technique by [86], and its principle stands on the conversion of an analog signal to a stream of pulses using a frequency considerably higher than the
Nyquist frequency. The original concept introduced 1-bit converters, with limited performance and applications, but the subsequent advancements such as the first development of a digital decimation filter proposed back in 1969 by [87] initiated a momentum that allowed the creation of very efficient converters that are still used and improved nowadays. In the core concept, the sigma-delta converters use oversampling to reduce the noise spectral density without affecting the signal power or the total quantization noise. The stream of pulses can be digitally filtered by applying a decimation algorithm. The decimation low-pass filter removes the out of band noise, resulting in a noise attenuation out of the signal interest range.

Some advantages include:

- High resolution conversion using low-cost components;
- Less demanding anti-aliasing filters;
- Easier and more efficient noise attenuation.

On the other hand, some limitation may apply:

- Limited bandwidth for high resolutions (typical 1M samples/s for 16-bit and 100K samples/s for 24-bit);
- The oversampling required is a significant challenge for high-frequency application. The use of dedicated hardware is a typical solution;
- Latency associated with digital filtering.

The application of the sigma-delta modulation technique on a MEMS device capacitive accelerometer was first published in 1990 [88]. According to [89], the sigma-delta modulator technology enables various advantages, especially on high-end applications. The in-depth analysis of the developments of EM-ΣΔM (electromechanical sigma-delta modulators) closed-loop MEMS accelerometers over the last decade [89], concludes that this kind of approach is currently the best solution to achieve navigation-grade performances. The development of high-order sigma-delta controllers can be a lengthy process that needs high-performance real-time computing for the necessary digital signal processing. The setup of the sigma-delta control on MEMS accelerometers is traditionally determined based on simulations. These simulations allow for the verification of the system stability and the pursuit for optimum system gains [90] but are relatively slow to perform.

The sigma-delta modulation is a well-studied closed-loop control technique that
uses signal feedback and integration to reject in-band quantization noise by moving it out of band \cite{91}. Several publications show the advantages of the sigma-delta modulation technology on the improvement of the electrostatic forces linearization over the traditional voltage amplitude modulation approach \cite{90} \cite{88} \cite{34}. The closed loop system architecture is shown in Figure 5.1.

![Figure 5.1: Closed loop accelerometer with sigma-delta controller.](image)

In this chapter, a different approach is proposed. The developed application built on top of the base platform aims at the control of an accelerometer with a configurable multi-order sigma-delta controller that allows for fast assessment of multiple conditions on the real device and detects instability of the device real responses when subject to real stimulus.

## 5.2 System Overview

The physical scale of MEMS devices impose time constraints several orders of magnitude smaller than the traditional mechanical counterparts. Also, the necessity for significantly larger sampling rates than the device bandwidth was a computational obstacle until recent technological advances. In this solution, the feedback net is composed by the base system lock-in amplifier, followed by a configurable prescaler to adjust the operation frequency, a lag-compensator for phase adjustment, a multi-order sigma-delta modulator and a simple circuit for electrostatic actuation using fast IC switches. The system is capable of operating without processor intervention after the setup is performed. This minimizes the workload on the processor and allows a feedback loop operation in real-time up to 5MHz, which is limited only by the ADC sampling frequency. The amount of digital signal filters, and mathematical operations required for such sampling rate is not compatible with modern real-time processors. On the other hand, such as with the characterization solution, having a processor to setup and control these elements
allows for a flexibility and configurability that is harder to develop, maintain and scale with pure hardware implementations. The interrupt abilities and low-latency of the embedded processor allow for asynchronous information such as the pull-in event related to instability to be triggered in the processor. Figure 5.2 shows the digital block that composes the processing system.

![Digital system components for sigma-delta closed-loop operation.](image)

5.2.1 Phase Compensator

A MEMS accelerometer is a second order mechanical system described by the following expression relating the displacement and acceleration, where $W_n$ is the natural frequency and $Q$ is the quality factor:

$$\frac{x(s)}{a(s)} = \frac{1}{s^2 + \frac{W_n}{Q}s + W_n^2}$$  \hspace{1cm} (5.1)

The mechanical nature introduces a phase delay that must be compensated in order to reduce the structure closed-loop oscillation. The module was developed to allow a phase lead or lag compensation (although the structure always introduces a phase lag) by implementation of the following discrete transfer function:

$$G_{\text{comp}}(z) = K \frac{(z - a)}{(z - b)}$$  \hspace{1cm} (5.2)
Which is implemented in hardware by the following discrete time equation (as already deducted in Section 3.2.1):

\[ out(i) = A \times out(i - 1) + B \times in(i) + C \times in(i - 1); \]  

(5.3)

The phase lag compensator coefficients can finally be tuned for each individual structure by a lookup algorithm that minimizes the output oscillation when the system is set to 2\textsuperscript{nd} order sigma-delta controller under no acceleration.

### 5.2.2 Sigma-Delta Module

The sigma-delta component, shown in Figure 5.3 allows for four different circuits that result in different orders. It can be bypassed, resulting in a second order system provided by the MEMS device, or it can be configured to select a third, fourth or fifth order path, according to the multiplexer position configured by software. The feedback and forward gains between each stage are also mapped in the processor memory space and are thus easily reconfigurable by software. The multiple topologies were compiled from several works, including [37] and [90].

![Figure 5.3: Multi-order configurable sigma-delta controller.](image)

### 5.2.3 Decimator

The decimation is the process by which the sigma-delta bitstream is requantized to produce the sensor outcome. The decimation is performed in hardware by the application of a low pass second order IIR filter with a 1kHz or 200Hz cutoff.
frequency (both were tested for evaluation). The signal is then sampled at a configurable decimation rate. An interrupt can be enabled to signal the presence of new data for the processor.

### 5.2.4 Actuation Controller

The electrostatic actuation is based on an AS5791 digital to analog converter (DAC), but a small adaptation must be made to change from manual to automatic switch control, allowing hardware control, with its inherent high rates and predictable performance. In order to comply with the necessary fast actuation rates, the ADG1434 analog switch is used to enable or disable the force application. The system is also capable of detecting a pull-in event, with configurable threshold limits, and removes immediately the force upon detection. This is important to preserve the structures integrity when tested with unstable gains.

![Actuation circuit](image)

**Figure 5.4**: Actuation circuit that allows flexibility and speed by enabling real-time hardware delegated closed-loop control.

### 5.3 Results

A comparative study between five different sigma-delta architectures applied to two different MEMS devices was performed using the experimental setup depicted in Figure 5.5. The read-out circuit, and consequently the MEMS sensor are attached to a precision motor, enabling the measurement of the sensitivity and the analysis of the system noise figures. The actuation system and FPGA development board are also shown.

For all the performed measurements, the sigma-delta modulator was operating with a sampling frequency of 454 kHz, and the one-bit DAC uses a voltage of 10 V
to stimulate the microstructure. The system is capable of a measuring cycle lower than 100 milliseconds between set positions.

![Figure 5.5: Sigma-delta evaluation system experimental setup.](image)

To achieve improved performance of the sigma-delta modulator, all the gains must be adjusted for each device. Usually, this is performed by simulation [92], but here, the flexibility of the approach enables the fine tuning of the gains, trough experimental results, in a very short period of time [93]. A gain combination evaluation time is composed by the time it takes to configure the sigma-delta module, the motor rotation time between the three chosen inclinations (-0.1g, 0g, +1g), the stabilization time, the decimation output communication and the sensitivity computation time. Using this solution, each combination takes about 10 seconds, where over 90% of the time is consumed by the motorized angle adjustment.

The noise performance improvement from a second order sigma-delta (the device is in itself a second order system) to a third order system (using only one block) is shown in Figure 5.6.

### 5.3.1 Sigma-delta evaluation and optimization

The structures AS5 and L50 (with extra mass) gains were used to evaluate the sigma-delta module. The structures Scanning Electron Microscopic (SEM) pictures can be seen in Figure 5.7, where the L50 structure extra-mass is evident.
Signal switch spike compensation

The readout circuit is composed of a charge amplifier (shown again in Figure 5.8), which is based on a simple current integrator. The Sigma-Delta control is based on a very fast electrostatic inversion on the actuator plates voltage that triggers a current inversion on the amplifier feedback loop. This inversion creates a short but large output spike inherent to the amplifier circuit that propagates throughout the readout circuit, that is not fully attenuated by the digital filters and effectively affects the measurements.

In order to overcome this limitation, a simple digital mechanism was implemented between the ADC and the lock-in signal flow blocks, to replicate the latest 16
recorded samples when a signal inversion is applied on the structure. The discarded samples do not present a significant signal degradation since the ADC works at 5MHz and as such, only 3.2\(\mu\)s are ignored. Besides, the difference is still attenuated by the lock-in low-pass filter.

**Phase compensator tuning**

As explained in section 5.2.1, the phase lag compensator parameters must be fine tuned to attenuate the closed-loop oscillations caused by the mechanical system inherent delay. In order to achieve high sensitive performances, the phase compensator must be adjusted for each single device. It can be done by setting a second order sigma-delta scheme and search the phase lag phase and frequency that minimizes the device oscillation using a simple look up algorithm. The phase lag compensator phase and frequency found to compensate the AS5 and L50 structures are shown in Table 5.1.

Table 5.1: Adjusted phase compensator parameters for the micro-devices

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Phase</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>AS5</td>
<td>80°</td>
<td>7000 Hz</td>
</tr>
<tr>
<td>L50</td>
<td>66°</td>
<td>3800 Hz</td>
</tr>
</tbody>
</table>

**Optimum Gains Lookup Algorithm**

The optimum sensitivity gains look up algorithm is based on a simple successive approximations routine.

In a initial approach, a wide granularity gains map is generated to apply and get a first approach on what may be the optimum region. When this first gains range is determined, a closer, finer gain map is generated in order to avoid the application of an enormous gains combinations. The algorithm look up results for the target
structures are shown in the Table 5.2.

Table 5.2: Optimum gains for the multiple gains on the AS5 and L50 structures

<table>
<thead>
<tr>
<th>Order</th>
<th>AS5</th>
<th>L50</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>k1=0</td>
<td>k1=0</td>
</tr>
<tr>
<td></td>
<td>k2=0</td>
<td>k2=0</td>
</tr>
<tr>
<td></td>
<td>k3=0</td>
<td>k3=0</td>
</tr>
<tr>
<td></td>
<td>b1=b2=0</td>
<td>b1=b2=0</td>
</tr>
<tr>
<td></td>
<td>g1=g2=0</td>
<td>g1=g2=0</td>
</tr>
<tr>
<td>3</td>
<td>k1=0.01</td>
<td>k1=6*10^-6</td>
</tr>
<tr>
<td></td>
<td>kf1=15</td>
<td>k1=1365.5</td>
</tr>
<tr>
<td></td>
<td>k2=0.05</td>
<td>k2=6*10^-5</td>
</tr>
<tr>
<td></td>
<td>kf2=120</td>
<td>kf2=814</td>
</tr>
<tr>
<td></td>
<td>k3=55</td>
<td>k3=1485</td>
</tr>
<tr>
<td></td>
<td>b1=b2=0</td>
<td>b1=b2=0</td>
</tr>
<tr>
<td></td>
<td>g1=g2=0</td>
<td>g1=g2=0</td>
</tr>
<tr>
<td>4</td>
<td>k1=6*10^-6</td>
<td>k1=6*10^-6</td>
</tr>
<tr>
<td></td>
<td>kf1=15</td>
<td>k1=1365.5</td>
</tr>
<tr>
<td></td>
<td>k2=6*10^-5</td>
<td>k2=6*10^-5</td>
</tr>
<tr>
<td></td>
<td>kf2=814</td>
<td>kf2=814</td>
</tr>
<tr>
<td></td>
<td>k3=1</td>
<td>k3=1</td>
</tr>
<tr>
<td></td>
<td>kf3=1485</td>
<td>kf3=1485</td>
</tr>
<tr>
<td></td>
<td>b1=b2=0</td>
<td>b1=b2=0</td>
</tr>
<tr>
<td></td>
<td>g1=g2=0</td>
<td>g1=g2=0</td>
</tr>
<tr>
<td>5b</td>
<td>k1=6*10^-6</td>
<td>k1=6*10^-6</td>
</tr>
<tr>
<td></td>
<td>kf1=15</td>
<td>k1=1365.5</td>
</tr>
<tr>
<td></td>
<td>k2=6*10^-5</td>
<td>k2=6*10^-5</td>
</tr>
<tr>
<td></td>
<td>kf2=814</td>
<td>kf2=814</td>
</tr>
<tr>
<td></td>
<td>k3=1</td>
<td>k3=1</td>
</tr>
<tr>
<td></td>
<td>kf3=1485</td>
<td>kf3=1485</td>
</tr>
<tr>
<td></td>
<td>b1=b2=0.005</td>
<td>b1=0.0025</td>
</tr>
<tr>
<td></td>
<td>b2=0.004</td>
<td>b2=0.004</td>
</tr>
<tr>
<td></td>
<td>g1=g2=0</td>
<td>g1=g2=0</td>
</tr>
</tbody>
</table>

The gains are applied and the decimation data is evaluated. If the system is unstable for a set of gains, a pull-in event will occur, the processor will be signaled with an interrupt event and the hardware will immediately switch off the actuation.
voltage to avoid the collision.

With the phase compensator and gains optimized, the sensitivity and Allan variance were measured for the two devices, for two different bandwidths, 200Hz and 1000Hz. The Allan variance is a commonly used method to analyze the decimated data to verify the decimation algorithm and measure the sensor noise performance. This was achieved through different designs of the low-pass filter and decimation ratio of the decimation filter.

The Table 5.3 presents a summary of the experimental sensitivities and noise figures, and as expected, due to the much bigger spring loaded mass, the sensitivity is higher on the device L50. Noise figures are also better (lower) in device L50, being in accordance with the theoretical thermomechanical noise.

<table>
<thead>
<tr>
<th>Device: AS5</th>
<th>Order 2</th>
<th>Order 3</th>
<th>Order 4</th>
<th>Order 5</th>
<th>Order 5b</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth: 200 Hz</td>
<td>17.376 bits/g</td>
<td>17.365 bits/g</td>
<td>17.361 bits/g</td>
<td>17.356 bits/g</td>
<td>17.349 bits/g</td>
</tr>
<tr>
<td>Resolution: 20 bits</td>
<td>260.2 $\mu g/\sqrt{Hz}$</td>
<td>64.84 $\mu g/\sqrt{Hz}$</td>
<td>46.19 $\mu g/\sqrt{Hz}$</td>
<td>37.49 $\mu g/\sqrt{Hz}$</td>
<td>35.57 $\mu g/\sqrt{Hz}$</td>
</tr>
<tr>
<td>Device: AS5</td>
<td>Order 3</td>
<td>Order 4</td>
<td>Order 5</td>
<td>Order 5b</td>
<td></td>
</tr>
<tr>
<td>Bandwidth: 1000 Hz</td>
<td>12.887 bits/g</td>
<td>12.575 bits/g</td>
<td>12.557 bits/g</td>
<td>12.559 bits/g</td>
<td>12.550 bits/g</td>
</tr>
<tr>
<td>Resolution: 15 Bits</td>
<td>1589 $\mu g/\sqrt{Hz}$</td>
<td>185.1 $\mu g/\sqrt{Hz}$</td>
<td>97.93 $\mu g/\sqrt{Hz}$</td>
<td>62.89 $\mu g/\sqrt{Hz}$</td>
<td>62.96 $\mu g/\sqrt{Hz}$</td>
</tr>
</tbody>
</table>

The results of the Allan variance measurements for the AS5 and L50 structures are shown in Figure 5.9 and in Figure 5.10 respectively. It is perceptible that the results are generally better for the 200 Hz bandwidth. The best result achieved was $4.4/\sqrt{Hz}$ for device L50 with a 5th order sigma-delta modulation. It is also visible that the device L50 is oscillating for the higher-orders modulations at low frequencies. This phenomenon can have different origins, such as mechanical vibrations of the building that are interfering with the measurements, or low frequency oscillations caused by the sigma-delta architectures and gains.

The power spectrum density of the system’s bitstream for both devices at different bandwidths are shown in Figure 5.11, Figure 5.12, Figure 5.13 and Figure 5.14. As illustrated, the noise shape is being modulated into the higher frequencies as the modulator order increases.

The performed tests yielded results in an accordance with the theoretical founda-
tions of sigma-delta modulators, with higher modulation orders resulting in lower noise levels within the bandwidth, increasing the performance of the accelerometer. The noise is also being shifted into the higher frequencies as the modulator order increases.

As a final note, these results are in concordance with the fundamental theory of sigma-delta modulators, included in the work developed by [90].

Figure 5.9: AS5 structure Allan variance with multiple orders.
Figure 5.10: L50 structure Allan variance with multiple orders.

5.4 Solution Memory Map

The Table 5.4 presents the processor peripherals, their respective addresses and interrupt addresses. The decimator and the complex sigma-delta modules are the only modules necessary to build from the base platform to perform the sigma-delta control. In the case of the sigma-delta, the gains and configurations are mapped in the Lock-in memory space to avoid the overhead necessary by the instantiation
of another APB module. The DAC was also modified to allow an automatic control option, delegating the closed-loop operation to the hardware, as explained in Section 5.2.4. The pull-in detection mechanism feature was reused from the characterization application to preserve the structure integrity when an unstable gains arrangement is applied.

The hardware based feedback loop allows a high frequency operation, which leads to bandwidth and sensitivities performances improvement, while assuring the integrity of the structure.

Figure 5.11: Power spectrum density for AS5 device with 1000Hz bandwidth.
Figure 5.12: Power spectrum density for AS5 device with 200Hz bandwidth.
Figure 5.13: Power spectrum density for L50 device with 1000 Hz bandwidth.
Figure 5.14: Power spectrum density for L50 device with 200 Hz bandwidth.
<table>
<thead>
<tr>
<th>Id</th>
<th>Unit</th>
<th>Address / IRQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>cpu0</td>
<td>Processor</td>
<td>AHB Master 0</td>
</tr>
<tr>
<td>ahbjtag0</td>
<td>JTAG Debug Link</td>
<td>AHB Master 1</td>
</tr>
<tr>
<td>rom0</td>
<td>AHB ROM</td>
<td>AHB: 00000000 - 00100000</td>
</tr>
<tr>
<td>apbmst0</td>
<td>AHB/APB Bridge</td>
<td>AHB: 80000000 - 80100000</td>
</tr>
<tr>
<td>dsu0</td>
<td>LEON3 Debug Support Unit</td>
<td>AHB: 90000000 - A0000000</td>
</tr>
<tr>
<td>mig0</td>
<td>DDR2 Controller</td>
<td>AHB: 40000000 - 50000000 APB: 80000000 - 80000100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 2</td>
</tr>
<tr>
<td>uart0</td>
<td>Generic UART</td>
<td>APB: 80000100 - 80000200</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRQ: 8</td>
</tr>
<tr>
<td>irqmp0</td>
<td>Interrupt Controller</td>
<td>APB: 80000200 - 80000300</td>
</tr>
<tr>
<td>gptimer0</td>
<td>Timer Unit</td>
<td>APB: 80000300 - 80000400 IRQ: 8</td>
</tr>
<tr>
<td>gpio0</td>
<td>GPIO port</td>
<td>APB: 80000600 - 80000700</td>
</tr>
<tr>
<td>adev11</td>
<td>Decimator</td>
<td>APB: 80002A00 - 80002B00 IRQ: 10</td>
</tr>
<tr>
<td>adev12</td>
<td>ADC Module</td>
<td>APB: 80000800 - 80001000 IRQ: 11</td>
</tr>
<tr>
<td>adev13</td>
<td>DAC Module</td>
<td>APB: 80001000 - 80001800 IRQ: 13</td>
</tr>
<tr>
<td>adev14</td>
<td>Sample Module</td>
<td>APB: 80001800 - 80001900 IRQ: 14</td>
</tr>
<tr>
<td>adev15</td>
<td>Lock-in amplifier</td>
<td>APB: 80001A00 - 80001B00 IRQ: 15</td>
</tr>
<tr>
<td>ahhbstat0</td>
<td>AHB Status Register</td>
<td>APB: 80000400 - 80000500 IRQ: 7</td>
</tr>
</tbody>
</table>
Chapter 6

Conclusions

The MEMS devices control is still a popular research subject due to the improvements it can provide to the devices performances and manufacture processes. This thesis presented an hardware assisted microprocessor centered solution capable of addressing the modern challenges, based on a design space exploration of the common elements, their association and individual performance requirements. The processing capability, customization simplicity and re-usability have been demonstrated in both the characterization and sigma-delta control applications with significant improvement at measurement and evaluation time.

The control of MEMS devices is a typical issue that needs to be addressed when designing a MEMS device. It was the purpose of this thesis to explore the possibilities offered by the electrostatic actuation on capacitive accelerometers, by describing the system characteristics and exploring the possibilities offered by modern digital processing systems. It is clear from the analysis of the multitude of devices, each with it’s own unique physical characteristics that there is no ’one-solution fits it all’ approach. However, the present development and exploration of a flexible control stack solution can be classified as a contribute to perform design decisions whose extension to different devices can be explored with promising advantages.

The typical approaches to handle the structures control are quite often underdeveloped, both due to the increasing complexity and investment required to include modern digital technologies into the design, and from the intense focus on performance improvements on the design and manufacturing skills. Is it clear from the results based on the demonstrator applications that the improvements and opportunities gained by the inclusion of electrostatic control to close the feedback loop is
quite significant, suggesting that the adaptation to other types of devices would be beneficial, since the electrostatic control can be (and already is) extended to many devices other than accelerometers. The complete stack solution also presents a real bottom-up approach with several problems solved, from the signal acquisition and actuation circuits and logic, passing through the digital optimization of front-end sensitivity and noise performance, the microprocessor control of all the necessary high-performance hardware blocks specific to each solution, up to the high-level gateway provided to allow the use of the powerful Matlab language and algorithms on real structures under the concept of an abstraction layer.

In the characterization application, the fast assessment of three typical accelerometer characteristics (Pull-in voltage, Quality Factor and Resonant Frequency) can be measured in 1.5 seconds, and further development targeting a time-wise full-wafer analysis was accomplished. Each characteristic was analyzed, both in terms of accuracy, repeatability and measurement interval. The experimental data acquired validates the digital approach followed in this work and shows that the digital platform is a powerful tool for MEMS testing and characterization. When combined with device modeling, it can be used for layout validation, during the design phase, process variability characterization and process parameters estimation, such as in the case of over-etching. Moreover, since the key mechanical characteristics are obtained, such characterization techniques can be used to derive calibration parameters for the MEMS devices. In the future, the algorithms used to measure the device characteristics can be optimized, in order to further reduce the testing time. All the necessary actuation and control peripherals were identified and developed in order to comply with the singular real-time necessities of each, in an attempt to optimize the balance between configurability, performance and flexibility.

In the sigma-delta application, a new approach is proposed, by using a fast assessment on the real structure instead of the traditional and lengthy simulation approach. The proposed approach for sigma-delta control evaluation of MEMS devices allows for a fast assessment of a set of gains in real devices within 100 milliseconds, subject to real conditions, including noise and physical oscillations. Using the real-time features and a high-level Matlab instruction interface, the plethora of advanced mathematical algorithms can be explored to improve the assessment time and results. Also, the test on real structures allows a fine tuning of gains to compensate for each device individual properties and degradation that comes with the structure aging.
As a final note, we are convinced that the use of digital systems will continue to spread and develop in the MEMS field and that much of the devices performance improvement will be accomplished by exploring novel control methods that in it’s turn will put more pressure on fastest and more efficient digital signal handling and delegate much of that responsibility to the modern hardware-software technologies.

6.1 Limitations

During the system development, a few challenges occurred that have been solved in a way to minimize it’s effect on the results. There are however some limitations we would like to address in order to push the performance further:

- Since the characterization application is fundamentally a digital implementation, several parallel channels can be connected enabling the simultaneous measurement of devices (strongly decreasing the testing time). For instance, for a characterization time of 1.5s (time experimentally validated) and a similar overhead time for automatically changing the electrical probes to a new device, the testing of a full-wafer with 420 DUTs would require 21 minutes. If 10 parallel characterization digital channels would be used, the total time would be reduced to 2.1 minutes;

- The exchange of the parallel plates excitation signal from a square signal to a hardware controlled sinusoidal signal (creating a better spectral behavior) may also have an impact on the front-end sensitivity and noise performance. It would require a refactor of the actuation circuit and the generation of a controlled and synchronous signal inside the FPGA;

- The signal spike that occurs when the actuation is exchanged could be solved by changing the front-end charge amplifier to a switched capacitor amplifier circuit. This would be a permanent solution to avoid the inversion spikes and would be expected to increase the frontend SNR whilst reducing the power consumption [94];

- The RTOS task scheduler is currently not being explored to it’s full capabilities, since the majority of operations are simple and sequential. It is therefore important to test RTOS for more demanding operations.
6.2 Future Work

- The use of a soft-core processor was considered for both the learning opportunities, platform independence and for the possibility for future integration of the complete digital circuit on a silicon chip. On the other hand, the current FPGA technology shows a tendency to integrate a hard-core processor such as the ARM processor to free FPGA space and accomplish higher processing performances. The replacement of the soft-core processor on the system can be explored, as it will allow the creation of higher order filters, that in it’s turn will very likely increase the control efficiency without losing flexibility. Besides, the software tools such as the Vivado Suite have a simple memory mapping handling that can simplify and increase the development productivity;

- The sampling mechanism has been used to pinpoint and debug several implementation issues in the signal flow. It is used by filling an internal buffer and subsequently transfer it asynchronously through the serial port. The processor has an ethernet interface that can be explored to create a real-time streaming link that can be used for an extended and simpler analysis of the internal signals;

- The creation of a single development board to hold both the sense and actuation circuits, and the FPGA would ease the hardware replication and incentive the test of new control methods;

- The sigma-delta gains optimization may be improved by using the genetic algorithms available on Matlab since the current lookup algorithm cannot perform much faster and still guarantee to find the best set instead of a local maximum;

- It was observed that the L50 device is oscillating for the higher-orders modulations at low frequencies. This phenomenon can have different origins, such as mechanical vibrations of the building that are interfering with the measurements, or low frequency oscillations caused by the sigma-delta architectures and gains. Further studies will need to be conducted, in order to evaluate and minimize these effects;

- The power consumption was not pondered during this project, since it was not necessary to miniaturize the solution. This power analysis is still needed
to be performed both with the soft-core and the hard-core because they will change in terms of performance but also on the power consumption. The solution developed never presented a significant increase in the FPGA temperature, but the power characterization is still necessary to obtain sustained data;

- The current work was based on inertial devices for testing, however, the changes required to operate other types of devices were not evaluated, and as such, it should be performed in order to increase the platform flexibility and test for the others devices specific requirements;

- The use of three similar structures in three individual setups, each controlled by an individual serial interface and positioned in each of the three accelerations (-1g; 0g and +1g) would improve significantly the gains search algorithm, since the motorization delay takes more than 90% of the time. A final approach and individual device adjustment would finally be performed with the motorized setup to fine tune to each device individual properties.
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