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A CONTROL STRATEGY FOR A THREE-LEVEL UNIFIED POWER QUALITY CONDITIONER

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***Abstract* – In this work a control strategy for a three-level Unified Power Quality Conditioner (UPQC) is introduced. Basically, this control strategy is based on the set of active and non-active (reactive) power definitions in the time domain, which have been proposed by Fryze in the 30´s of the last century. The goal of this work consists in expand this control strategy to deal with three-level converters. The use of three-level converters allows a better performance of the equipment, by reducing harmonics and the ripple of the generated voltages and currents. Simulation results on PSCAD/EMTDC will be illustrated in order to verify the accuracy of the expanded control strategy.**

KEYWORDS

Active Filters, NPC three-level converters, Lagrange Multiplier Method, Power Quality.

I. INTRODUCTION

ONE of the serious problems in electrical systems is the increasing number of electronic components that are used by industry as well as residences. These devices, which need high-quality energy to work properly, at the same time, are the most responsible ones for injections of harmonics in the distribution system.

Therefore, devices that soften this drawback have been developed. One of them is the unified power quality conditioner (UPQC). As shown in Fig. 1, this equipment consists of a shunt active-filter together with a series active-filter. This combination allows a simultaneous compensation of the source currents and the voltages at the sensitive load, in a way they are sinusoidal, balanced and minimized.

A back-to-back configuration is used for the series- and shunt-PWM three-level converters, in which the shunt converter is responsible to maintain the DC-link voltages at an adequate value. It is important to note that the output UPQC current controllers, denominated as (i_{arefJ}, i_{brefJ}, i_{crefJ}) for (J = 1, 2), are equal to six. An explanation about this controller will be given at the next topic.

One of the reasons that prevent the use of such device in electrical systems is the size of their passives components as well as the single-phase transformers. To have a better knowledge of such a drawback, it is important to remind that the controlled voltages and currents, generated by a classical two-level converter, present, depending of the switching frequency, high harmonic levels and ripples.

An alternative to mitigate these problems is to design the passive capacitors and transformers that can be able to operate in such conditions. The proposed solution in this work consists to replace the two-level converter by a converter that presents a three-level topology.

In general, multilevel power converters can be viewed as voltage synthesizers, in which the high output voltage is synthesized from many smaller voltage levels [1]. Thus the harmonics and ripples of the generated voltages and currents are reduced. The major advantage of this characteristic is that the size of the passive components and the series single-phase transformers can be reduced, optimizing the performance of the UPQC.

The UPQC control strategy is based on a set of active and non-active (reactive) power definitions on the time domain, proposed by Fryze in 1932 [2]. The set of these definitions were adopted in a control strategy such that the conditioner is able to compensate, in real time, the harmonics, balances of the system voltages and load currents as well.

The major contribution of this work was to expand the control strategy of the UPQC of two-level to three-level converters. This control strategy also includes a control that regulates the DC-Link voltage capacitors, forcing an exchange of energy between the active power converters and the AC network system. Simulation results on PSCAD/EMTDC are illustrated in order to verify the performance of the conditioner.

II. THREE-LEVEL UPQC CONTROLLER

The expanded control strategy of the UPQC may be seen on Fig. 2. This controller is composed by a digital synchronizing circuit (PLL circuit); together with the control blocks “Reference Voltages Algorithm” and “Reference Currents Algorithm”.

The PLL circuit has the system voltages (v_{as}, v_{bs}, v_{cs}) as inputs and the outputs are the signals *pll_a*, *pll_b* and *pll_c*. The calculated output signals present sinusoidal waveforms with unitary magnitude, at the fundamental frequency and in phase with the positive-sequence components of the system voltages. It is important to state that the PLL circuit is the main part of the controller, since it is the one that must guarantee the load voltages and source currents will be balanced sinusoids at the fundamental frequency and in phase with the positive-sequence system voltages.

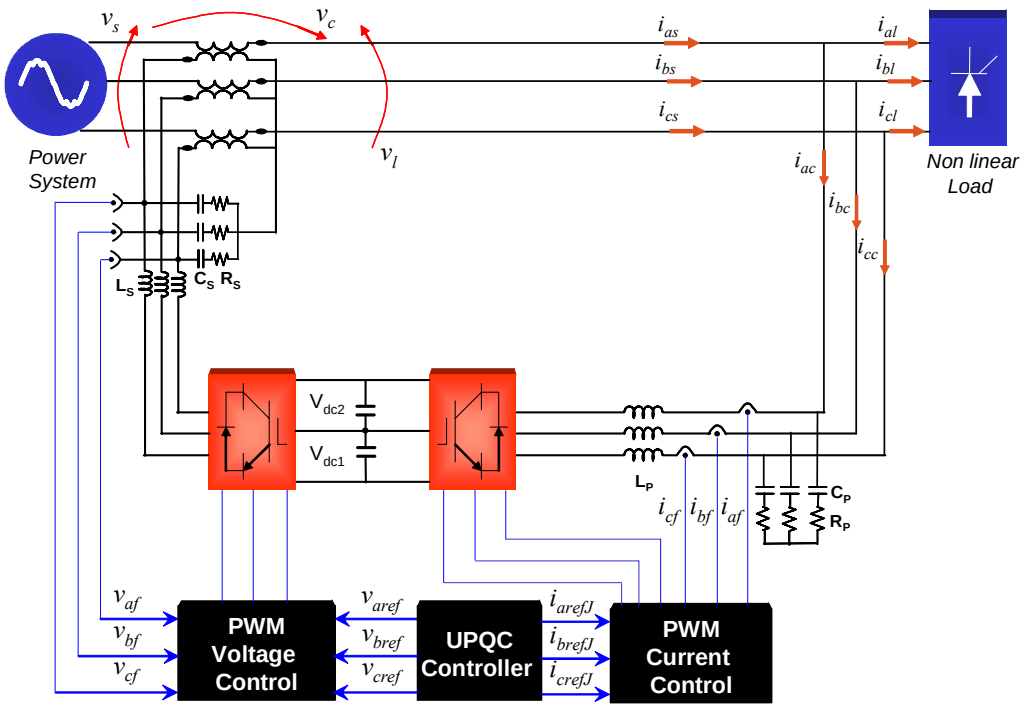

Fig. 1 Electrical Diagram of the Unified Power Quality Conditioner

The control block "Reference Currents Algorithm" determines six reference currents (i_{aref1}, i_{bref1}, i_{cref1}) and (i_{aref2}, i_{bref2}, i_{cref2}), by using the load currents (i_{al}, i_{bl}, i_{cl}), the DC-Link voltages (v_{dc1}, v_{dc2}) and the PLL outputs (*pll_a*, *pll_b*, *pll_c*) as inputs. The reference currents are then synthesized by the shunt-active power converter.

The "Reference Voltages Algorithm" calculates, in real time, the reference voltages (v_{aref}, v_{bref}, v_{cref}) that will be synthesized by the series power converter. The inputs are the PLL outputs (*pll_a*, *pll_b*, *pll_c*), and the system input voltages (v_{as}, v_{bs}, v_{cs}).

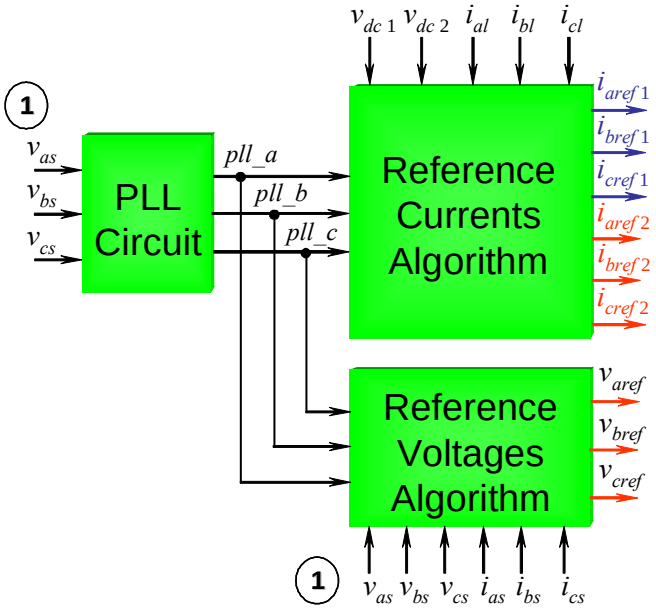

Fig. 2 UPQC Control Strategy

A PLL Circuit

The PLL circuit (Fig. 3) can operate satisfactorily under highly distorted and unbalanced system voltages, as long as the proportional and integral gains are tuned accordingly [3]. The inputs are the line system voltages in p.u. (per unit) quantities $v_{ab} = v_{as} - v_{bs}$ and $v_{cb} = v_{cs} - v_{bs}$. The outputs of the PLL circuit are control signals *pll_a*, *pll_b* and *pll_c*. These control signals present a sinusoidal waveform, at the fundamental frequency with the phase angle of the positive-sequence system voltages component, and an unitary amplitude.

The current feedback signals $ia(\omega t) = sin(\omega t)$ and $ic(\omega t) = sin(\omega t - 2\pi/3)$ are internally generated by the PLL circuit, using the time integral of output ω of the PI-Controller. The PLL circuit can reach a stable point of operation only if the input $p_{3\phi}$ of the PI-Controller has a zero average value ($\bar{p}_{3\phi} = 0$) and the low-frequency oscillating portions in ($p_{3\phi} = \bar{p}_{3\phi} + \tilde{p}_{3\phi}$) have been minimized.

Once the circuit is stabilized, the average value of $p_{3\phi}$ is zero and, consequently, the PLL locks on the phase angle of the fundamental positive-sequence system voltage. Due to this condition, the auxiliary currents $ia(\omega t)$ and $ic(\omega t) = sin(\omega t - 2\pi/3)$, become orthogonal to the fundamental of the positive-sequence component phase-neutral voltages, v_{as} and v_{cs} respectively. Therefore, $pll\_a(\omega t) = sin(\omega t - \pi/2)$ is in phase with the fundamental of the positive-sequence component contained in v_{as}.

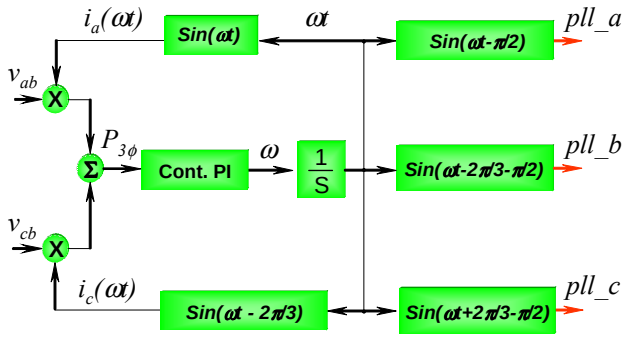

Fig. 3 The PLL Circuit

B Reference Voltages Algorithm

The control strategy employed to calculate the reference voltages v_{aref}, v_{bref}, v_{cref} is illustrated in Fig. 4. Basically, this controller is divided in two control blocks: the V_{+1} voltage detector and the damping algorithm. Both control strategies are based on the Lagrange Multiplier Method, as introduced in [4].

In a UPQC configuration, the passive components may produce undesirable resonances. The use of a damping controller is an interesting alternative in order to provide a power system stability and harmonic isolation. This controller is represented by the "*Damping Algorithm*" control block. More about this controller can be found in [5] and [6].

The V_{+1} voltage detector control block extracts, from the system voltages v_{as}, v_{bs}, v_{cs} its fundamental positive-sequence components, which are denominated as v_{a1}, v_{b1}, v_{c1}. The damping algorithm control block presents as inputs the system currents i_{as}, i_{bs}, i_{cs}, together with the output PLL control signals *pll_a*, *pll_b*, *pll_c*, and determines the control signals v_{ah}, v_{bh}, v_{ch}.

Finally, the reference control voltages v_{aref}, v_{bref}, v_{cref} are calculated by the combination of the system voltages v_{as}, v_{bs}, v_{cs} with the control signals v_{a1}, v_{b1}, v_{c1} and v_{ah}, v_{bh}, v_{ch}, according with Fig. 4.

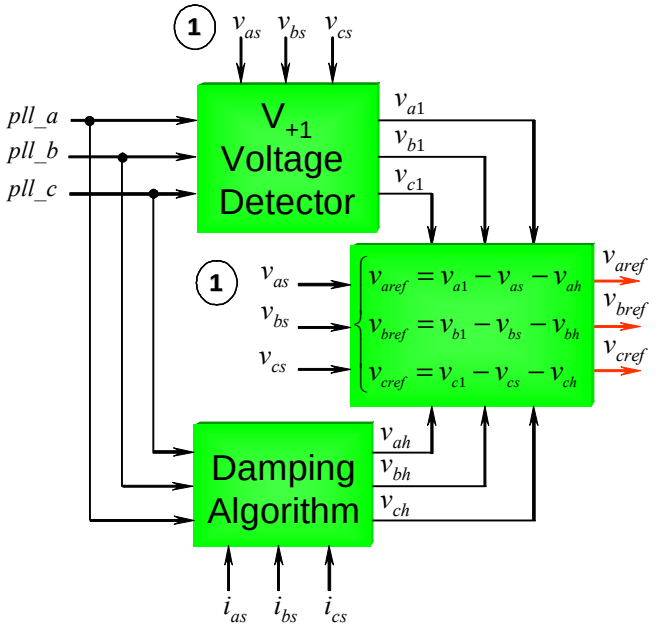

Fig. 4 Reference Voltages Algorithm Control Strategy

C Reference Currents Algorithm

The "*Reference Currents Algorithm*" (Fig. 5) calculates, in real time, the reference currents that must be drained from the power system by means of the shunt active converter. This control strategy is based on the active and non-active (reactive) currents definitions introduced in [2] and applied in active power filters [7].

In a three-level topology, with two capacitors on the DC side, it is desired that the control voltage on each of the capacitors be independent. Therefore the six reference output currents were designed in such a way that three of them enclose the information regarding the control of one of the capacitors, and the remaining outputs of the other capacitor.

According to the Lagrange Multiplier Method, the conductance G is calculated as described in (1):

$$G = \frac{pll\_a \cdot i_{al} + pll\_b \cdot i_{bl} + pll\_c \cdot i_{cl}}{pll\_a^2 + pll\_b^2 + pll\_c^2} \quad . \quad (1)$$

The use of a low pass-filter (sliding average filter) is necessary in order to extract the load currents harmonics and unbalances. The control signals G_{e1} and G_{e2} are calculated according with the equation (2).

$$\begin{cases} G_{e1} = G_{bar} + G_{l1} \\ G_{e2} = G_{bar} + G_{l2} \end{cases} \quad . \quad (2)$$

The control signals G_{l1} and G_{l2} are achieved from the "*DC Voltage Regulator*" control block (Fig. 6). These control signals demand an exchange of energy between the active power converters and the CA network, in order to keep the DC-link voltages regulated.

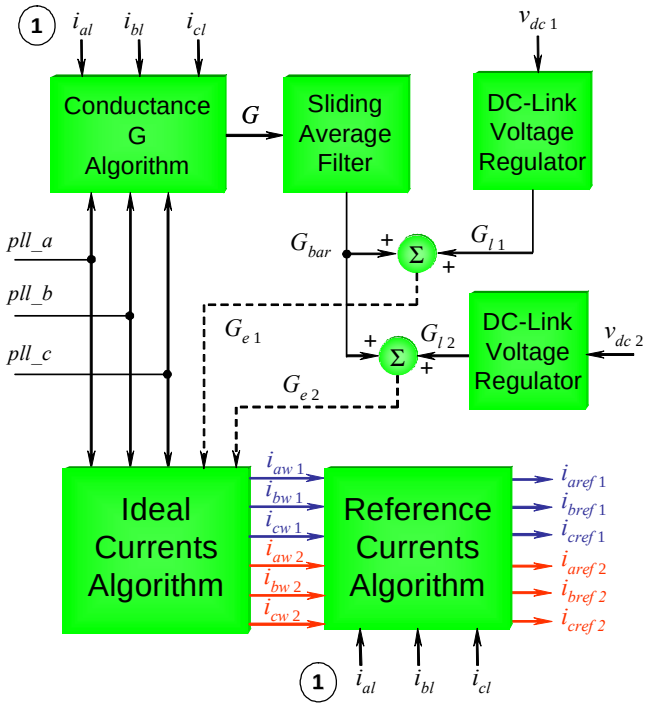

Fig. 5 Reference Currents Algorithm Control Strategy

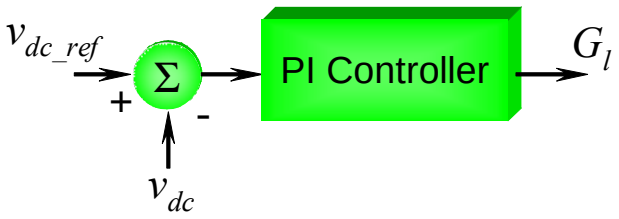

Fig. 6 DC-Link Voltage Regulator

Thus it may be stated that the control signals G_{e1} and G_{e2} represent the magnitude of the fundamental positive-sequence load currents, plus the switching losses of the active power converters.

The six control currents i_{aw1}, i_{bw1}, i_{cw1} and i_{aw2}, i_{bw2}, i_{cw2} are determined from the product between the control signals G_{e1} and G_{e2} and the PLL output signals pll_a, pll_b, pll_c as presented on equation (3).

$$\begin{cases} i_{aw1} = G_{e1} \cdot pll\_a \\ i_{bw1} = G_{e1} \cdot pll\_b \\ i_{cw1} = G_{e1} \cdot pll\_c \end{cases} \quad \begin{cases} i_{aw2} = G_{e2} \cdot pll\_a \\ i_{bw2} = G_{e2} \cdot pll\_b \\ i_{cw2} = G_{e2} \cdot pll\_c \end{cases} \quad . \quad (3)$$

The six output reference currents are calculated from the difference between the six control currents and the load currents according with equation (4).

$$\begin{cases} i_{aref\,1} = i_{aw1} - i_{al} \\ i_{bref\,1} = i_{bw1} - i_{bl} \\ i_{cref\,1} = i_{cw1} - i_{cl} \end{cases} \quad \begin{cases} i_{aref\,2} = i_{aw\,2} - i_{al} \\ i_{bref\,2} = i_{bw\,2} - i_{bl} \\ i_{cref\,2} = i_{cw\,2} - i_{cl} \end{cases} \quad . \quad (4)$$

III. Switching Three-Level Converters

In order to illustrate the switching control technique applied to the series and shunt active power converters, a basic three-level NPC (Neutral Point Clamped) topology, illustrated on Fig. 7, is used as reference.

It is important to state that the conventions applied to the series and shunt converters must be taken into account before establishing the switching control strategies for each one of the active power converters.

The equations (5) and (6) describe the applied conventions for series-and shunt-active power converters, respectively, according with Fig. 1.

$$v_l = v_c + v_s \quad ; \quad (5)$$

$$i_s = i_C + i_l \quad . \quad (6)$$

The switching control technique of the series-active power converter is presented in Fig. 8. It is a very simple controller,

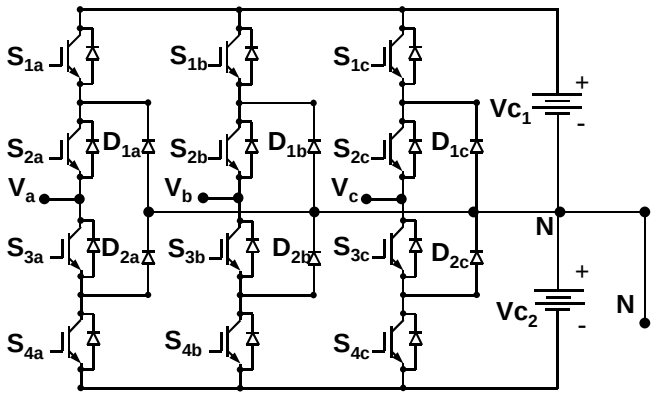

Fig. 7 Three-Level Neutral Point Clamped Converter

presented in [8], and expanded to deal with three-level converter topology. Basically it consists in adding the reference signal, to the amplified error between the reference and the measured signals. The signal v_{a_PWM} is compared with two triangular trigger waves with unitary amplitudes but different limits. The first wave (v_{trig1}) is between 0 and +1 and the second (v_{trig2}) is between +1 and +2. The switching logic for phase "a" may be seen below. The same principle is applied to the remaining phases.

$$\begin{aligned} & v_{a\_PWM} > v_{trig2}: \\ & S_{1a}, S_{2a} - ON\,;\, S_{3a}, S_{4a} - OFF; \\ & v_{trig2} > v_{a\_PWM} > v_{trig1}: \\ & S_{2a}, S_{3a} - ON\,;\, S_{1a}, S_{4a} - OFF; \\ & v_{a\_PWM} < v_{trig1}: \\ & S_{1a}, S_{2a} - OFF\,;\, S_{3a}, S_{4a} - ON; \end{aligned} \quad . \quad (7)$$

The switching control strategy of the shunt active power converter is illustrated in Fig. 9. This control strategy was introduced in [9] and, in this work, it was expanded to deal with the six output references.

Basically it consists in comparing the two error signals (i_{a1_PWM}, i_{a2_PWM}). These error signals are resulted from the amplified difference between the shunt active power converter current i_{af} and the reference currents $i_{a\_ref\,1}$, $i_{a\_ref\,2}$, plus the output PLL signal pll_a. The same principle is applied to remain phases. The phase "a" switching logic

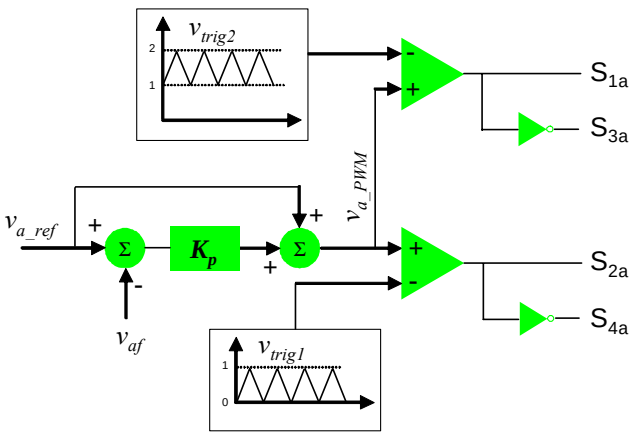

Fig. 8 Series Switching Control Strategy

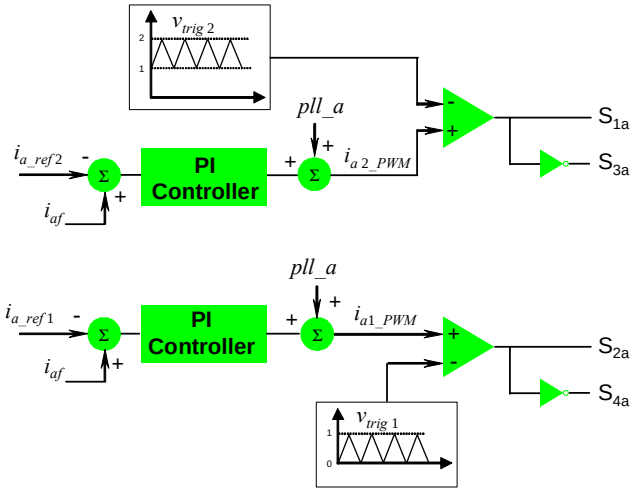

Fig. 9 Shunt Switching Control Strategy

state is illustrated on equation (8).

$$\begin{aligned} &i_{a2\_PWM} > v_{trig2}: \\ &S_{1a} - ON\,;\, S_{3a} - OFF; \\ &i_{a2\_PWM} < v_{trig2}: \\ &S_{1a} - OFF\,;\, S_{3a} - ON; \\ &i_{a1\_PWM} > v_{trig1}: \\ &S_{2a} - ON\,;\, S_{4a} - OFF; \\ &i_{a1\_PWM} < v_{trig1}: \\ &S_{2a} - OFF\,;\, S_{4a} - ON; \end{aligned} \quad . \qquad (8)$$

IV. Simulation Results

A test case was mounted to investigate the performance of the three-level UPQC through digital simulations, in the PSCAD/EMTDC. The power system is equal to 40 KVA, with a 440 V line voltage, including a negative-sequence unbalance plus 7th harmonic. The non-linear load is composed by a three-phase six-pulse thyristor bridge rectifier, together with a three-phase six pulse diode bridge rectifier. The six-pulse thyristor bridge rectifier presents a fire angle equal to 30 degrees.

The shunt-active filter starts its operation at 0.22s and the series-active filter at 0.27s. The six pulse thyristor bridge rectifier is connected with the power system at 0.15s. The six pulse diode bridge rectifier is connected with the power system at 0.5s and disconnected from the power system at 0.8s. The major objective of inserting this second load is to analyze the performance of the DC-Link control voltages, when an additional load is inserted and removed from the electrical power system. The total time simulation is 1.0s.

An inductor and a resistor, whose values correspond to 0.2 % of the system base impedance, compose the source impedance. In this case, the short-circuit power at the load terminal is equal to 20 p.u. The RLC filters to mitigate switching frequency harmonics at the series-active power converter are L = 300µH, R = 1.0Ω and C = 15µF and at the shunt-active power converter are L = 250 µH, R = 2Ω and C = 30µF.

Two capacitors of 2500µF each are used at the common DC-link converters, which mean an equivalent capacitance of 1250µF. The reference voltage is equal to 800V. In order to estimate the dimension of the capacitor, the unit capacitor constant (UCC) is calculated, by the equation (9):

$$UCC = \frac{\frac{1}{2}\cdot C \cdot V^2}{S} = 10ms \quad . \qquad (9)$$

Fig. 10 and Fig. 11 illustrate the distorted load currents i_{al}, i_{bl}, i_{cl}, and the distorted and unbalanced supply voltages v_{as}, v_{bs}, v_{cs}, respectively. The source voltages are composed with 5% of negative-sequence component, plus 5% of a 7th harmonic (negative-sequence).

Fig. 12 and Fig. 13 present the system currents i_{as}, i_{bs}, i_{cs}, and the load voltages v_{al}, v_{bl}, v_{cl}, respectively, during the UPQC connection with the power system. At 0.27 seconds, when the conditioner presents its connection process completed, these currents and voltages become balanced, sinusoidal and minimized.

Fig. 14 shows the source current i_{as}, and the load voltage v_{al}, during the UPQC connection process. Initially the current i_{as} is delayed 30 degrees from the voltage v_{al}. As expected, when the UPQC start its operation, the power factor is regulated.

Finally in Fig. 15 are illustrated the DC-Link voltages, regulated in 400 V each. The robustness of the proposed controller may be verified due the fact that the DC-Link voltages are regulated, even the presence of an additional load, represented by a three-phase diode bridge rectifier.

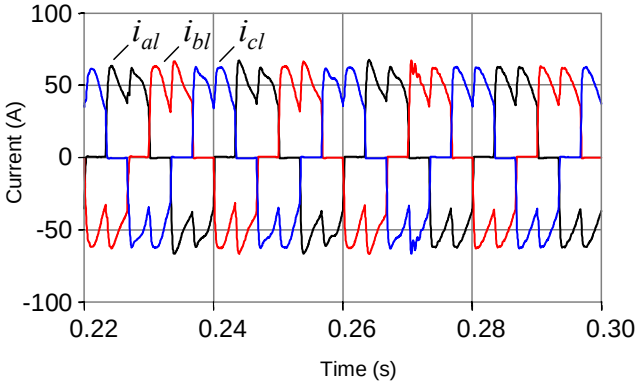

Fig. 10 Distorted Load Currents

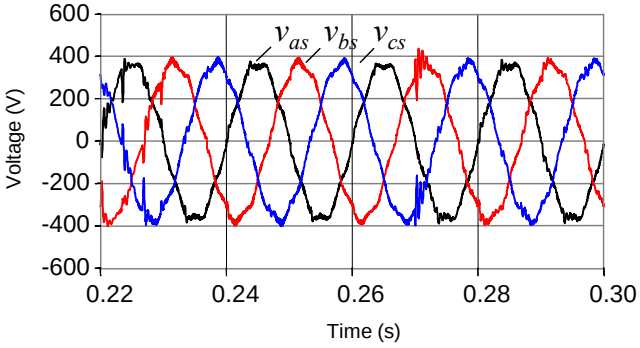

Fig. 11 Distorted and Unbalanced System Voltages

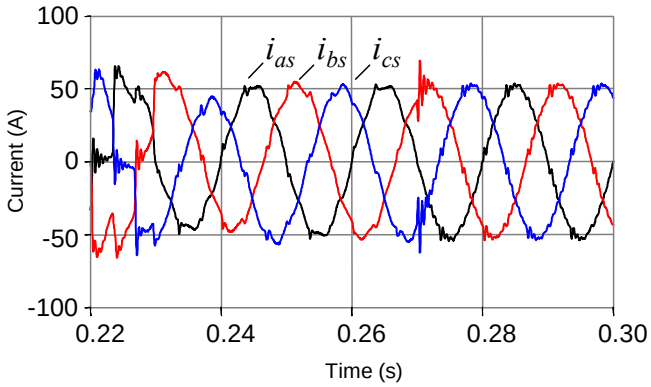

Fig. 12 System Currents during the UPQC connection with the power system

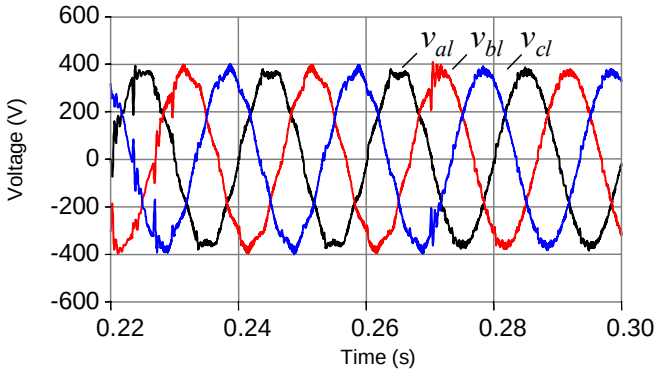

Fig. 13 Load Voltages during the UPQC connection with the power system

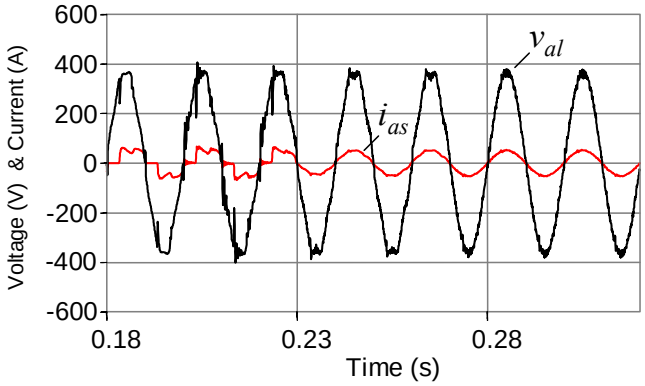

Fig. 14 Load Voltage and System Current during the UPQC connection at the power system

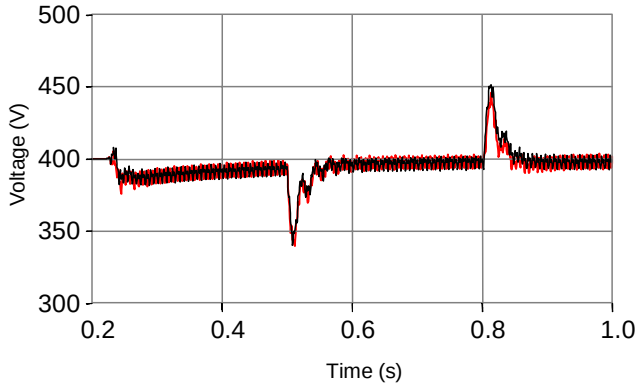

Fig. 15 Regulated DC-Link Voltages

V. Conclusions

In this work an expanded control strategy for three-level UPQC was presented. As confirmed by the simulation results, this control strategy shows a satisfactory performance, such that the compensated system currents and load voltages are sinusoidal, balanced and minimized, with the DC-Link voltages regulated.

Another interesting point is that the introduced switching control technique is done directly from the A-B-C phase system, avoiding Clark or Park transformations to implement it.

At present, the authors are still investigating multilevel converters and control strategies, including switching control techniques, in order to develop power electronics devices to mitigate power quality problems in high power systems.

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