CMOS X-ray Image Sensor with Pixel Level A/D Conversion

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Abstract

This paper describes a pixel array for x-rays imaging consisting in 400 $\mu m \times 400$ μm photodiodes fabricated in CMOS technology, with an A/D converter for each one. Above the photodiodes, an array of scintillating CsI:Tl crystals are placed. So, the x-ray energy is first converted to visible light by the scintillating crystals which is then detected by the photodiodes. The photocurrent produced by each photodiode is finally converted to a digital form by a sigma-delta analog to digital converter. The sigma-delta a/d converter uses 18 minimum-size MOSFETs and one capacitor. 8 to 10 bits of resolution can be achieved.

1 Introduction

One of the first x-ray sensors developed was based on a silicon Charge Coupled Device (CCD) imager [1]. The silicon has a low x-ray absorption coefficient, but for each 1 MeV of x-ray photons absorbed, about 277000 electrons are excited [2]. This enables the construction of x-rays sensors with better sensibility than the traditional radiographic silver films. However, the small number of detected photons in the imager results in a significant quantum noise [2]. In order to reduce the quantum noise, the radiation dose can be increased or the quantum efficiency of the sensor can be improved. The increase in the x-ray dose is obviously not desired for medical applications. The quantum efficiency of the sensor can be increased by adding a scintillating layer above the imager. Since the x-rays are first absorbed by the scintillating layer, which has a high absorption coefficient, and then converted into visible light, the quantum efficiency of the detector is improved. A drawback of this approach is that the spatial resolution of the device is approximately equal to the thickness of the scintillator layer [3] (figure 1). Several techniques were tested in order to increase the scintillating layer thickness without decreasing the spatial resolution [4, 5].

The recent development in CMOS image detectors opens a new way to construct digital x-rays imagers. The replacement of CCDs with CMOS detectors is desirable for several reasons:

- The operating power is 5 to 10 times lower than the CCD (with processing electronics).
- The CMOS is a standard fabrication process, while CCD requires special manufacturing.
- CMOS fabrication costs are 5 to 10 times lower.
- It is possible to integrate analog and digital processing electronics in CMOS.

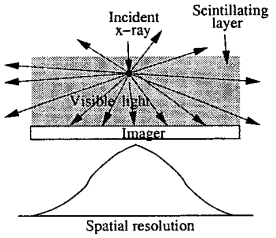

Fig. 1: Imager with scintillating layer and its spatial resolution.

The drawback is the difficult to match the high performance characteristics of CCD in terms of image quality [6].

2 Sensor description

The sensor consists in an array of blocks, containing each one a photodiode and an analog to digital converter. Figure 2 shows a picture of the sensor before the placement of the scintillating crystals. It consists in an 2×2 array of square photodiodes 400 $\mu m \times 400$ μm size. Each photodiode has its own A/D converter whose dimensions are 120 $\mu m \times 270$ μm, fabricated in a standard CMOS nwell 1.6 μm process. The pixel blocks are addressed column by column by means of a m to 2^m decoder

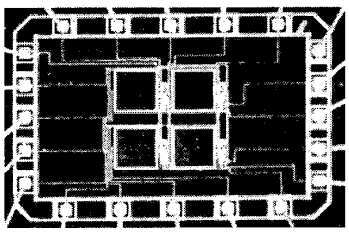

Fig. 2: Picture of the chip before the placement of the scintillating crystal.

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(not in this chip), and each pixel is connected to an output line, being all lines read at the same time by the output circuit. Each pixel block converts the light intensity, coming from the scintillator, in a digital code. This pixel block is shown in detail in figure 3. At the beginning all the integrators are reset

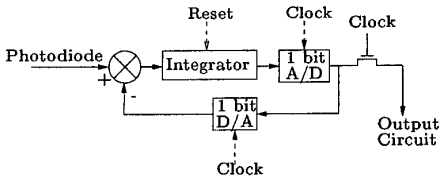

Fig. 3: Block diagram for one pixel.

in order to the analog to digital converters start at a known state. After the radiation fall upon the scintillators, and an image is focused in the photodetectors, the sigma delta converters start the conversion, being their result read in all lines at the same time, column by column. The oversampling rate of sigma delta was established in order to achieve 8 bits resolution.

The sigma delta modulator behaves as an high-pass filter to the quantization noise. As the signal is in a band of interest between DC and half the Nyquist frequency, during decimation, a low pass filter is used in order to remove most of the quantization noise without affect the input signal. This low-pass filter was implemented in software.

3 Circuit description

The circuit is divided in three sections: the integrator, the 1 bit analog to digital converter (comparator) and the 1 bit digital to analog converter. The photodetector is a photodiode implemented by a sn-substrate junction, in order to match the emission wavelengths of the scintillator (near 560 nm).

3.1 Integrator

The integrator is based on a current mirror, as it is illustrated in figure 4. The photodiode current flows

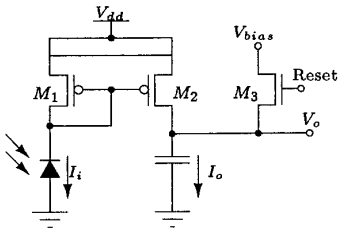

Fig. 4: Integrator based on a current mirror.

through M_1. As $V_{GS1} = V_{GS2}$, ideally a proportional current flows through M_2, since it is working in saturation region.

The maximum output voltage is limited by the fact that M_2 must remain in saturation, therefore

$$Vo_{max} = V_{DD} - V_{DSsat} = V_{DD} - (V_{GS2} - V_T). \quad (1)$$

The output resistance of the current mirror is simply given by the resistance of M_2, so

$$r_o = \frac{1}{\lambda I_o}. \quad (2)$$

where λ is the channel-length modulation parameter of M_2.

The small signal model of the integrator is shown in figure 5.

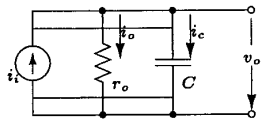

Fig. 5: Small signal model of the integrator.

In this circuit, $i_i = i_c + i_o$, where $i_o = v_o/r_o$ and $i_c = Cdv_o/dt$. After reduction,

$$\frac{dv_o}{dt} = Av_o + Bi_i, \quad (3)$$

where

$$A = -\frac{1}{r_o C} \quad \text{and} \quad B = \frac{1}{C}. \quad (4)$$

If this system is sampled with a sampling period h, it comes

$$v_o(h+1) = \Phi V_o(h) + \Gamma i_i(h), \quad (5)$$

where

$$\Phi = e^{Ah} \quad \text{and} \quad \Gamma = \frac{B}{A}\left(e^{Ah} - 1\right). \quad (6)$$

The transfer function is given by

$$H(z) = \frac{\Gamma z^{-1}}{1 - \Phi z^{-1}}, \quad (7)$$

and the DC gain is

$$H(1) = -\frac{B}{A} = r_o. \quad (8)$$

Equation 8 shows that the DC gain is large, so it is finite and higher than the oversampling ratio. In this conditions, the quantization noise in the signal band only increases 0.3 dB [7].

M_3 is used to reset the integrator, in order to the sigma delta modulator start at a known level. According to Netravali [8], there is about 3 dB improvement in signal to noise ratio by resetting the integrator at the beginning of each slow cycle, when uniform weights are used for the digital filters. Simulations shows that it is true even if the decimation is made with an optimum filter.

The functioning of the integrator was simulated, for an input current of 1 nA. Figure 6 shows the result.

A detailed analysis to the curve of figure 6 indicates that the integrator is linear from 0 V to 4.8 V, and it shows up a Pearson product moment correlation coefficient of 0.999496, quite close to 1. This means that the integrator has a linearity close to ideal.

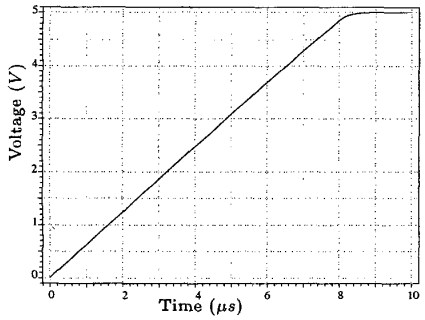

Fig. 6: Time response of the integrator for an input current of 1 nA.

3.2 One bit analog to digital converter (comparator)

Figure 7 shows the schematic diagram of the comparator. MOSFETs M_1 and M_2 constitute a differential pair which amplifies the voltage difference between V_{in} e V_{bias}. The sign of this difference is stored in the latch constituted by M_5 and M_6, when the clock falls down. The latch state is maintained while M_4 is off. This happens when the clock is at down level. Finally, MOSFETs M_7 and M_8 form a common source amplifier which amplifies the latch output voltage, so that the circuit output voltage ranges from 0 V to V_{dd}. Figure 8 shows the output waveform of the cir-

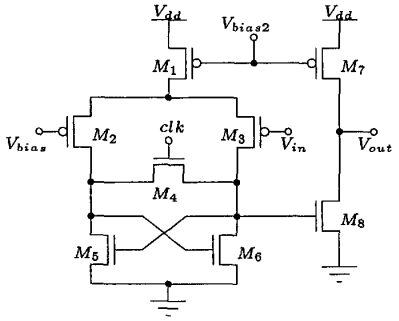

Fig. 7: Comparator.

cuit, when the reference voltage (V_{bias}) is 2.5 V, and a variable V_{in} .

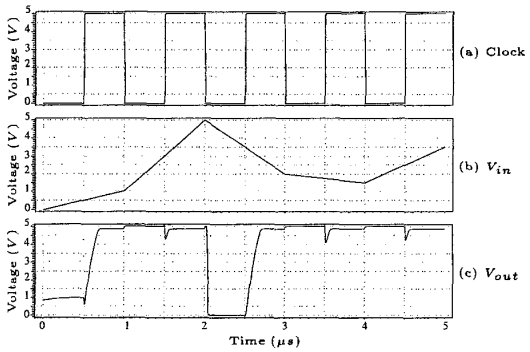

Fig. 8: Waveform of the comparator.

As is shown in figure 8, for each negative clock transition, the output voltage is 5 V if V_{in} is less than V_{bias}, and it is 0 V if V_{in} is greater than V_{bias}.

3.3 One bit digital to analog converter

The schematic diagram of the one bit digital to analog converter is shown in figure 9. This circuit is based

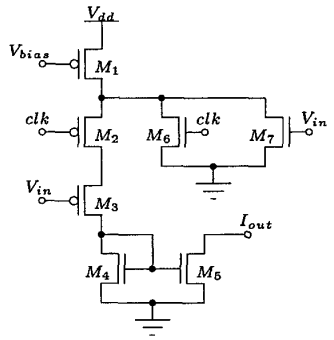

Fig. 9: One bit digital to analog converter

on a current mirror controlled by V_{bias}, the clock signal and the output voltage of the comparator (V_{in}). MOSFET M_1 acts as a constant current source, whose value is determined by V_{bias}. MOSFETs M_2, M_3, M_6 and M_7 form a logic *nor* gate. When the clock and V_{in} signals are at the low level, M_2 and M_3 are switched on, a current appears at the drain of M_5. This current is equal to the one at the drain of M_1 in the case of the dimensions of M_4 and M_5 are identical. If the clock signal or the one at the output of the analog to digital converter (V_{in}) are at the high level, M_6 or M_7 are switched on. This produces a null current at the drain of M_5. The graphic of figure 10 shows the output current waveform of the circuit of figure 9.

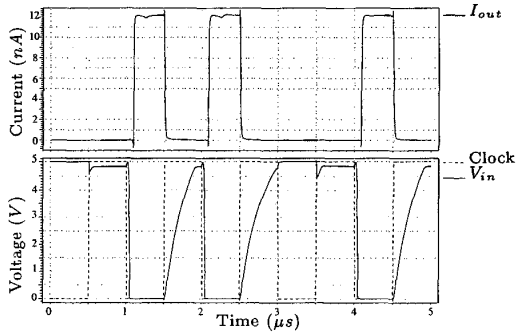

Fig. 10: Input and output waveforms of the one bit digital to analog converter.

3.4 Closed loop analysis of the sigma delta converter

Figure 11 shows the waveforms of integrator and the comparator output voltages (V_{int} and V_{out} respectively).

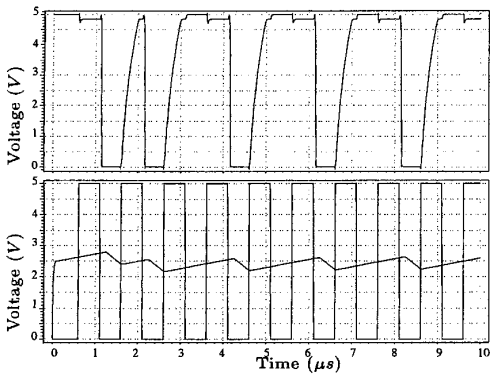

Fig. 11: Input and output waveforms of the sigma delta converter.

4 Experimental results

Figure 12 shows the output value for one pixel with an oversample ratio of 256. The test was performed using a didactic x-ray tube powered with a voltage of 35 kV and currents ranging to 1 mA. In order to obtain this graphic, a simple accumulate-and-dump digital filter was used. Its transfer function is given by

$$H(z) = \frac{1}{N} \sum_{i=0}^{N-1} z^{-i}, \qquad (9)$$

where N is the integer ratio between the input frequency and the output frequency of the filter.

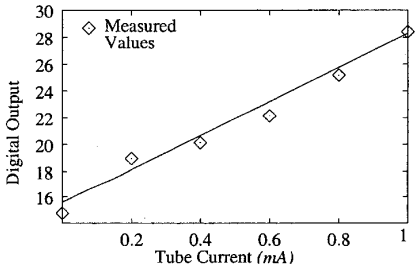

Fig. 12: Binary output of the sigma delta converter

Figure 13 shows the spectral power of quantization noise. In order to obtain this graphic, 14 conversions were made for different x-ray tube input currents. The 14 output bit streams were windowed by an Hanning window in order to calculate its fast Fourier transform. Then the average value was taken in order to draw the graphic. With a noise power of -60 dB near the signal bandwidth, theoretically is possible to achieve an output resolution near 10 bits. In practice, and due to the non idealities of the decimation filter, the noise power in the signal bandwidth will be greater. But with a oversample ratio of 256 is quite easy to obtain 8 bits of output resolution.

5 Conclusion

This paper described the readout electronics for a x-ray imaging sensor based on scintillating crystals.

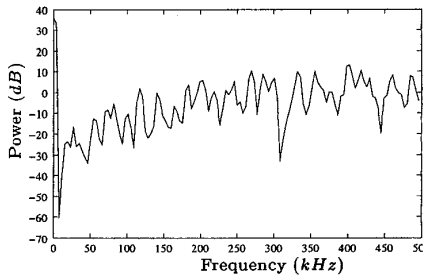

Fig. 13: Spectral power distribution of the quantization noise of the sigma delta converter, with an oversampling rate of 256.

This electronics are based on a sigma-delta analog to digital converter for each pixel. The converter uses only 18 minimum size MOSFETs and one capacitor. Tests carried out using a x-ray source show that a resolution of 8 bits with an oversampling ratio of 256 is possible to achieve with this device. As future work, we are fabricating a new device with 64 pixels of 200 $\mu m \times 200$ μm each one.

6 Acknowledgments

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