Universidade do Minho
Escola de Engenharia

João Elias Valente de Jesus

FPGA based Ultrasound Wireless Communication System

Dezembro de 2014

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UMinho | 2014

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Dissertação de Mestrado
Ciclo de Estudos Integrados Conducentes ao Grau de
Mestre em Engenharia Eletrónica Industrial e de Computadores

Trabalho efetuado sob a orientação do
Professor Doutor José Manuel Tavares Vieira Cabral

e coorientação do
Doutor Marcos Silva Martins

Dezembro de 2014

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Título da dissertação:
FPGA Based Ultrasound Wireless Communication System.

Ano de conclusão: 2014

Orientadores:
Professor Doutor José Manuel Tavares Vieira Cabral
Doutor Marcos Silva Martins

Designação do Mestrado:

Ciclo de Estudos Integrados Conducentes ao Grau de
Mestre em Engenharia Eletrónica Industrial e de Computadores

Área de Especialização: Sistemas Embebidos

Escola: Escola de Engenharia

Departamento: Departamento de Eletrónica Industrial

É AUTORIZADA A REPRODUÇÃO INTEGRAL DESTA DISSERTAÇÃO APENAS PARA EFEITOS DE INVESTIGAÇÃO, MEDIANTE DECLARAÇÃO ESCRITA DO INTERESSADO, QUE A TAL SE COMPROMETE.

Guimarães, 04/12/2014

Assinatura: _____

Under the waves, silence means survival...

Acknowledgements

In first place, I would like to express my gratitude to my advisor, Professor Doctor José Manuel Tavares Vieira Cabral, for the orientation and support throw-out this project. Then I would like to thank co-advisor Doctor Marcos Martins for the guidance and support provided during the entire project.

I also would like to thank the Department of Industrial Electronics of Minho University for all necessary conditions and facilities provided to carry out this dissertation.

I also want to express my gratitude to all my friends and colleagues specially Anderson Batista, Carlos Freitas, Cátia Chamusca, Diogo Sousa, Eduardo Barroso, José Teixeira, Marta Teixeira, Nelson Castro, Ricardo Silva, Rui Luz and Sérgio Gonçalves for theirs companionship, spirit of mutual help and support that they gave me during my academic career.

A very special thanks to my family for the unconditional support and patience showed in good and bad times.

Finally, I would like to thank all those who contributed directly and indirectly to this project.

Thank you all!

I dedicate this work to my family.

Abstract

This work focus on the development of a platform for an underwater wireless communication system. The system to be developed is based on acoustic transducers that are projected to emit sound waves at frequencies between 100 kHz and 4 MHz in an underwater environment. The same sensors are capable of being polarized with voltage signals of different amplitudes and, for instance, being used in different modulations.

The underwater environment is considered an unreliable communication medium due to countless factors acting in the propagation of the acoustic waves such as: high attenuation at long distances, low sound speed, and existence of effects like multipath and Doppler Effect.

Those features make it extremely difficult to predict a satisfactory underwater wireless communication condition and enhance the need for the design of a system flexible enough to work in different conditions counteracting different water channel effects. Therefore, the system could not be projected to work at a certain frequency or with a specific modulation technique. This way, the system must work as a high power signal generator.

To successful accomplish this work's goal an exhaustive survey of all the research in this area were carried out in order to understand how these characteristics may affect the acoustic signals and those effect's influence on the overall system requirements. Then, the project has been divided in parts such as: FPGA based modulator, digital to analog conversion unit, power amplifier, analog signal input instrumentation, analog to digital conversion unit, FPGA based demodulator and host computer user interface.

After the system being developed, several practical use cases were tested to confirm its functionality and accordance with the initial requirements. Several modular tests were also made to test specific functionalities and ate the end, a on the field test was performed with a PZT ultrasound transducer.

After all the testing it was concluded that the initial goals were meet and the project was concluded with success. The final system was able to polarize an ultrasonic emitter with 60 Vpp and output current greater than 3 A at frequencies superiors to 2 MHz. The same system was also able to receive signals as low as 14 μV from a hydrophone at frequencies above 1 MHz.

- **Keywords**

High frequency signals, FPGAs, Microcontroller, Variable gain amplifiers, PCB design, Hand soldering.

Resumo

O presente trabalho tem como objetivo o desenvolvimento de uma plataforma para comunicações subaquáticas sem fios. O sistema a ser desenvolvido baseia-se em transdutores acústicos que são projetados para emitir ondas sonoras em ambiente subaquático, com frequências entre os 100 kHz e os 4 MHz. Os respetivos sensores são também capazes de serem polarizados com sinais de tensão de variadas amplitudes podendo, portanto, serem utilizados para emitir sinais em diferentes modulações.

O ambiente subaquático é considerado um meio de comunicação problemático devido a inúmeros fatores que afetam a propagação das ondas acústicas no mesmo, tais como: alta atenuação a longas distâncias, a baixa velocidade do som, e a existência de efeitos como o *multipath* e o Efeito Doppler.

Essas características fazem com que seja extremamente difícil prever as condições de operação naquele meio. Em consequência, há a necessidade de projetar um sistema suficientemente flexível para que o mesmo possa operar em diferentes condições e não ser afetado pelos efeitos do canal aquático. Como tal, o sistema não pode ser projetado para trabalhar a uma determinada frequência ou com uma determinada técnica de modulação. O que implica que o mesmo deve funcionar como um gerador de sinal de alta potência.

Este projeto foi dividido em partes, tais como: modulador baseado em FPGA, a unidade de conversão analógico para digital, amplificador de potência, a unidade de conversão digital para analógico, a instrumentação do sinal analógico, o desmodulador, também baseado em FPGA e a interface de utilizador.

Depois de o sistema ter sido desenvolvido, vários casos de uso prático foram testados para confirmar a sua funcionalidade e verificar se estavam de acordo com os requisitos iniciais. Vários testes modulares foram também feitos para testar funcionalidades específicas bem como testes em ambiente real com um transdutor de ultra-sons PZT.

Após todos os testes concluiu-se que os objetivos iniciais foram cumpridos e o projeto foi concluído com sucesso. O sistema final foi capaz de polarizar um emissor de ultra-som com 60 Vpp e corrente de saída superior a 3 A e a frequências superiores a 2 MHz. O mesmo sistema também foi capaz de receber sinais de amplitude igual a 14 μV a 1 Hz.

- **Palavras-chave**

FPGAs, microcontroladores, amplificadores de ganho variável, desenho de circuito impresso.

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Acronyms List

ADC	Analog to Digital Converter
AUVs	Autonomous Underwater Vehicles
BJT	Bipolar Junction Transistors
BPF	Band Pass Filter
DAC	Digital to Analog Converter
DFS	Digital Format System
FIFO	First In, First Out
FPGA	Field-Programmable Gate Array
GPIO	General Purpose I/O
HPF	High Pass Filter
I/O	Input/Output
IC	Integrated Circuit
LCD	Liquid Crystal Display
LOFAR	Low Frequency Analysis and Recording
LPF	Low Pass Filter
NAVFACs	Naval Facilities
ONR	Office of Naval Research
OSI	Open Systems Interconnection
OTR	OuT-of-Range
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PSRR	Power Supply Rejection Ration
PT	Lead Titanate
PVDF	PolyViyliDeneFluoride
PZN	Lead Zinc Niobate
PZT	Lead Zirconate Titanate
SIO	Special I/O
SNR	Signal to Noise Ratio
SOFAR	SOund Fixing And Ranging
SONAR	SOund, NAvigation and Ranging
SOSUS	SOund SUrveillance System
UAVs	Underwater Autonomous Vehicles

ULNA	**U**ltra-Low **N**oise **A**mplifier
USB	**U**niversal **S**erial **B**us
UUVs	**U**nmanned **U**nderwater **V**ehicles
VGA	**V**ariable **G**ain **A**mplifier
VGAU	**V**ariable **G**ain **A**mplifier **U**nit
VGAUC	**V**ariable **G**ain **A**mplifier **U**nit **C**ontrol

Chapter 1

1 Introduction

Sound is produced when an object vibrates disturbing nearby air, liquid or solid molecules, and generating compression waves that travel in all directions away from the source. Those waves are perceived as sound when they collide with a human or an animal ear drum and causing a mechanical disturbance that is detected by neurons in the internal ear.

Sound can vary in frequency (high pitch vs. low pitch), amplitude (loudness), and periodicity (the temporal pattern of frequency and amplitude). Together, these three variables can create a complex variety of signals, from an insect's noise to human voice and vocal music. Since sound waves propagate rapidly through air and water, (about 331 m/sec) and (about 1500 m/sec), respectively, acoustic signals can be quickly started, stopped, or modified to send a message.

The human ear is able to detect, at best, sound frequencies within the range of about 20-20,000 hertz (vibrations per second). But some insects (as well as other animals like bats and dolphins) produce and detect sounds that are above this frequency range. Some grasshoppers and moths, for instance, produce ultrasonic sounds around 80 kHz and dolphins can hear frequencies as high as 150 kHz [1].

Dolphins use sound waves to echolocate (Figure 1-1) food in the sea and it involves emitting and interpreting sounds to detect objects' location underwater and is especially useful for two reasons: Bodies of water are often far too murky for sight, and sound actually travels quickly underwater, much faster than in air [2].

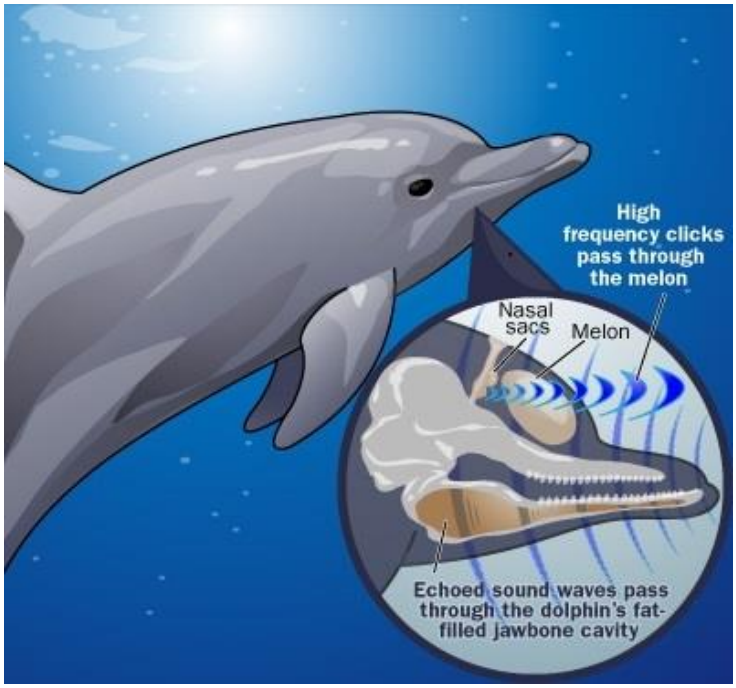

Figure 1-1: *How Dolphins echolocate* [2]

Dolphins use sound waves to communicate between them. Communication via acoustic waves has such advantages as effectiveness in long-range, doesn't need line of sight, but also has its disadvantages such as: reveals the sender's location, it's less effective in noisy environments and suffers high attenuation with distance.

These advantages and disadvantages have paved the way for the exploration of the sound properties for military purposes such as the SOund, NAvigation and Ranging (SONAR). Sonar is a system that uses transmitted and reflected underwater sound waves to detect and locate submerged objects or measure distances underwater. It has been used for submarine and mine detection, depth detection, commercial fishing, diving safety and communication at sea. The Sonar device sends out a subsurface sound wave and then listens for the returning echoes.

As early as 1822, Daniel Colloden used an underwater bell to calculate the speed of sound underwater in Lake Geneva, Switzerland. It was concluded that the velocity of sound in water was 1435 m/s. This value is not too different from currently known values and it led to the invention of dedicated sonar devices by other inventors later on [3].

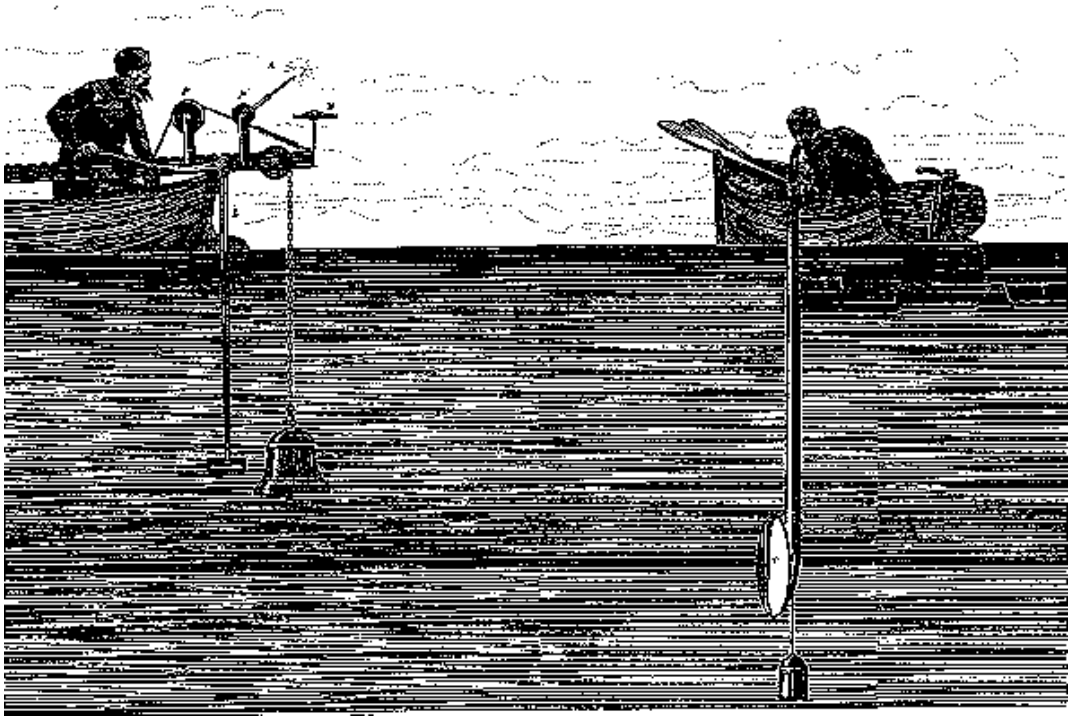

Figure 1-2: *First measurement of sound speed on* [3].

A century later, by early 1950, Frederick Hunt, the head of Harvard University's Underwater Sound Laboratory during WWII, argued that the U.S. Navy could use the SOund Fixing and Ranging (SOFAR) channel to detect submarines at distances of hundreds of miles by listening for the noises that they generate [4].

Under great secrecy, late in 1950, the Office of Naval Research (ONR) developed an undersea surveillance system designed to detect and track Soviet submarines using the SOFAR channel. The system that resulted was given the then highly classified name SOund Surveillance System (SOSUS).

Several arrays of hydrophones were placed at the ocean bottom. The hydrophones were connected by underwater cables to processing centers located on shore called "Naval Facilities" (NAVFACs) and then, Low Frequency Analysis and Recording (LOFAR) instruments installed at the NAVFACs were designed to analyze low-frequency underwater sounds to show which frequencies were present. The distinctive sound signatures generated by submarines could then be seen in what were called LOFAR-grams.

Figure 1-3 depicts a typical SOSUS watch floor. This one, at Centerville Beach, held hundreds of LOFAR "gram-writers," each turning out a frequency-versus-time representation of an array's low-frequency sound output along a given beam direction [5].

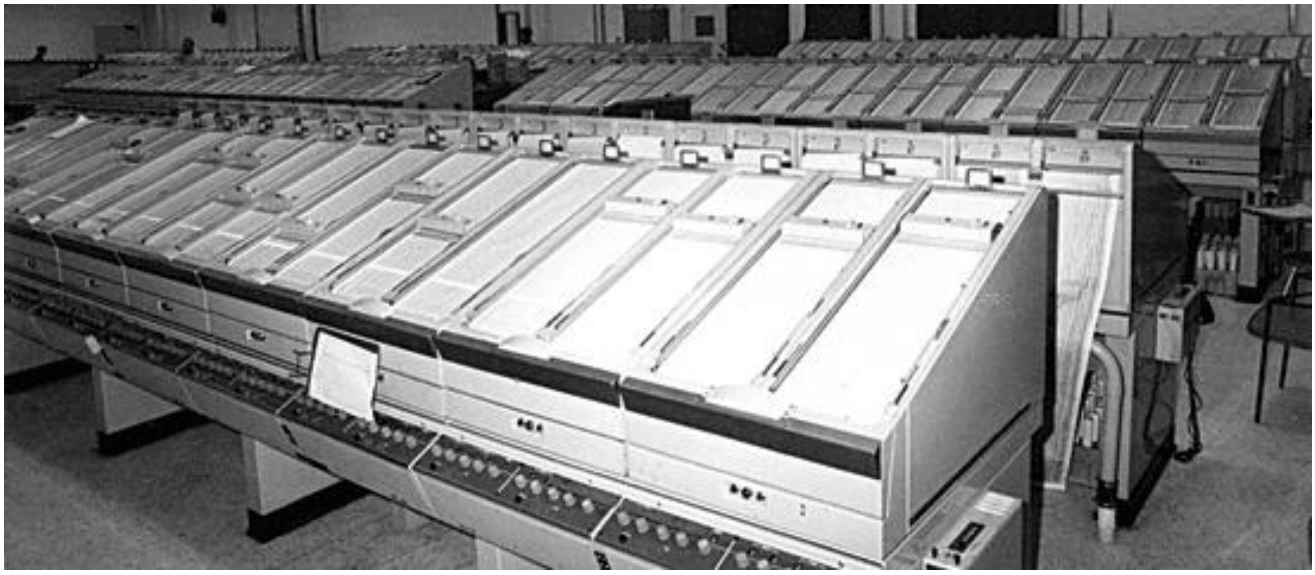

Figure 1-3: *A typical SOSUS watch floor*[5].

The SOSUS system was very successful in detecting and tracking the noisy diesel and then nuclear Soviet submarines of the Cold War. And, in October 26, 1962 after the SOSUS station on Turks Island makes a contact. The submarine, the C-20, was identified as a Soviet "**F**" class and it was forced to surrender [6]. From then on, the water was not a place where a submarine could dive undetected or hide, anymore.

This episode of undersea warfare brought up the importance of the underwater environment as a medium capable to transmit and receive acoustic signals. After that, the water as a communication channel has gain major importance in several fields, especially in the military. However, industrial scientific and medical progresses were made as a result of that.

1.1 Motivation

Along with the ever increasing list of applications for underwater acoustic communications systems, the used transducers were also improved over the times. From the bell, used by Daniel Colloden in 1822, to calculate the speed of sound underwater in Lake Geneva [3], to the 1 Mbps piezoelectric transducer, developed by Marcos Martins, in he's PhD Thesis [7], plenty of water went under the bridge.

The proliferation of piezoelectric transducers posed a challenge for the hardware developers to take full advantage of those transducers, especially in systems where operation covers a wide band of frequencies. This dissertation work aims to take on these challenges and develop a hardware system to match the requirements specified by Marcos Martins [7].

At the academic level, this project represents a fantastic opportunity to develop a multidisciplinary system. It also poses an interesting challenge at the integration level, because it provides an opportunity to work on a Hardware/Software co-design approach, making it a great opportunity to put into practice concepts learned during the course by the author. Therefore, more than an academic task, it represents a personal challenge and provides an excellent opportunity to integrate an active and dynamic team with a good work ethic.

1.2 Objectives

The goal of this dissertation is to develop an electronic system capable of driving the piezoelectric ultrasound emitters developed by Marcos da Silva Martins, at he's PhD Thesis, *Ultrasonic Wireless Broadband Communication System for Underwater Applications*, presented in 2013 at Minho University [7].

Those transceivers must be driven by a power circuit that generates a 30Vpp sinusoidal signal at 4 MHz. The system must also acquire acoustic signals using a Cetacean Research™ C304XR hydrophone, which generates a signal of frequency between 100 kHz and 4 MHz with 11.2 V maximum amplitude.

1.3 Methodologies

To successfully accomplish this dissertation's goal, the project was analyzed in different phases, at different levels in a bottom-up approach. This approach aimed to reduce the complexity of the overall project into smaller and independent systems. To accomplish that, the work was processed in different phases, such as: research, analysis, design, development, testing and documenting. In the documentation phase, the overall system's performance was registered and conclusions were made.

1.3.1 Tasks organization

The first phase of the current work was essentially a research phase that was performed in two main tasks. The first consisted in a research of the underwater acoustic communications systems state of the art, its technologies and transducers types being used. At this phase, the acoustic transducers to be used were characterized. The second task was a research on important theoretical concepts required to develop high frequency electronics, as well as the challenges faced when developing high speed mixed signal electronics, such as: power amplifiers, instrumentation, logic circuits.

The second phase, consists on an in-depth analysis of the system developed and its requirements. At this phase, technical and non-technical constraints were discussed based on the functional requirements. The use-cases were also presented in order to be used as guidelines for the following stages.

At the third phase, the design of a solution for the entire system was presented. From this phase on the system was viewed as a group of simpler systems, from the software layer all the way down to the instrumentation and power electronics. Therefore, solutions for desktop application, microcontroller firmware, FPGA's (Field-Programmable Gate Array) bitstream, Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC)'s instrumentations and the power electronics were designed and simulated.

The fourth phase, implementation, was composed by several tasks which aimed to implement independently the subsystems designed in the previous phase, such as: the desktop application in Java, the microcontroller firmware in C language, the logic programing in Matlab/Simulink, the digital-to-analog conversion, the analog-to-digital conversion, the instrumentation, the signal amplification and the power electronics.

At the integration phase, all subsystems were connected together and then tested for functionality and robustness. These tests were conducted in a convenient environment, using different transducers. At the end, results of each category were presented and both instrumentation and power amplification circuits were tested and characterized.

At the last phase, some conclusions were drawn about the achieved results. This conclusion aimed to describe which goals were achieved, which weren't and why.

1.4 Dissertation structure

For documentation purposes, the document is structured in seven chapters.

- Chapter 1, Introduction;
- Chapter 2, state-of-the-art.
- Chapter 3, System analysis;
- Chapter 4, System design;
- Chapter 5, System implementation.
- Chapter 6, Results;
- Chapter 7, Conclusion and future work;

1.5 Application scenarios

Despite the communication capability of the system under development, the same system could be applied in a variety of different applications, such as:

- Marine life listening;
- Ocean mapping;
- Divers communications (diver to diver or diver to ship);
- Information exchange (underwater Internet through Underwater Sensor Nodes (USNs));
- Underwater surveillance applications;
- Underwater Wireless Video Transmission;
- Assisted or Autonomous navigation (Unmanned Underwater Vehicles (UUVs) or Autonomous Underwater Vehicles (AUVs)).

The oceans research being made today needs Underwater Autonomous Vehicles (UAVs) to reach the most extreme, dangerous and deep places in the sea. Therefore, those vehicles need to be able to be remotely controlled and also retrieve the collected data in real-time.

Sensor networks for the industry are other application for this system. Industrial resources exploration can use sensor networks for monitoring the platforms and their machinery in the sea. Divers often need to communicate between each other to minimize risk and to be able to exchange information underwater. Other applications may include video and audio streaming [8].

Chapter 2

2 State of the art

A communication process takes place throw-out three basic elements that must be present in a communication system. Without these, the communication process won't work. These elements are: the emitter, the transmission channel and the receiver (Figure 2-1). The emitter converts a signal produced by an information source into an appropriate form to its propagation through the channel. The receiver captures the signal from the transmission channel and extracts its information content [9].

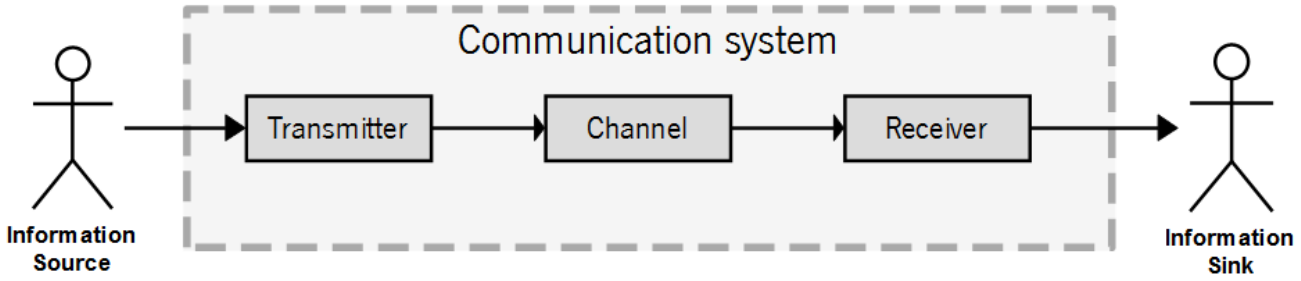

Figure 2-1: *Communication process elements.*

There are several types of transmission channels but, for this project, the focus is in the underwater channel. By underwater channel it should be understood any considerable large enough volume water, such as a fish tank, a swimming pool, a lake or the ocean.

2.1 Underwater acoustic channel

Since acoustic waves are subjected to low attenuation in water [10], they are considered as being preferable for this environment, especially in deep waters with stable thermal conditions. However, despite the advantages of acoustic communication in underwater environments, when compared to optical and radio, the propagation of sound also has significant challenges that influence the development of underwater acoustic communication systems. This is mainly due to the slow of acoustic propagation in water (about 1500 m/s).

When studying sound propagation in the underwater channel, phenomena like attenuation, ambient noise, Doppler Effect, propagation delay and multipath must be taken into account to accurately modulate it. However, for this dissertation work, only attenuation and ambient noise will be taken into consideration.

With the increase of the frequency, it is possible to increase the data-rate, but it also increases the attenuation, leading to a decrease in communication range, because underwater acoustic signals are frequency-

dependent attenuated (Figure 2-2) and an increase in attenuation leads to a signal weakening at the reception point, which leads to a degradation in the Signal-to-Noise Ratio (SNR).

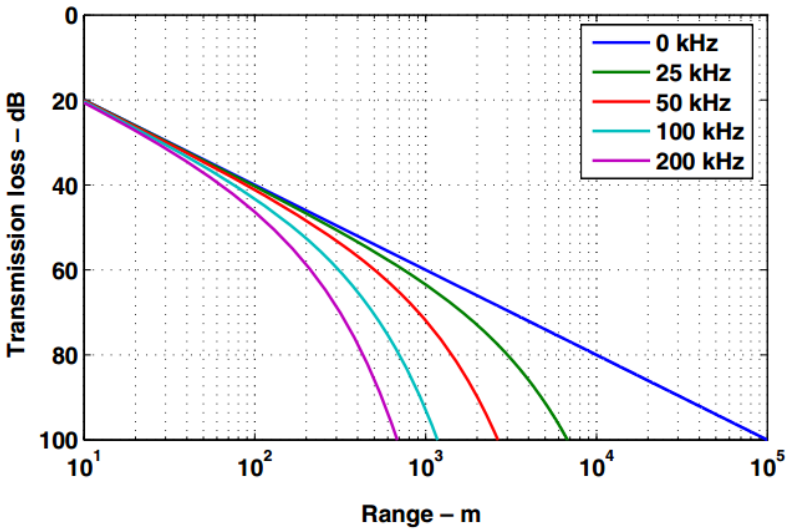

Figure 2-2: *Transmission loss as function of range for the frequencies of 0, 25, 50, 100 and 200 kHz* [10].

These limitations set the maximum range at which a system is capable of operating. Because of that, a compromise between bandwidth and range has to be achieved.

The underwater channel equivalent model used for this dissertation's purposes can be seen in Figure2-3 which depicts a signal being affected by a gain and noise, which represents the attenuation and ambient noise adding to a noise signal when it travels in water.

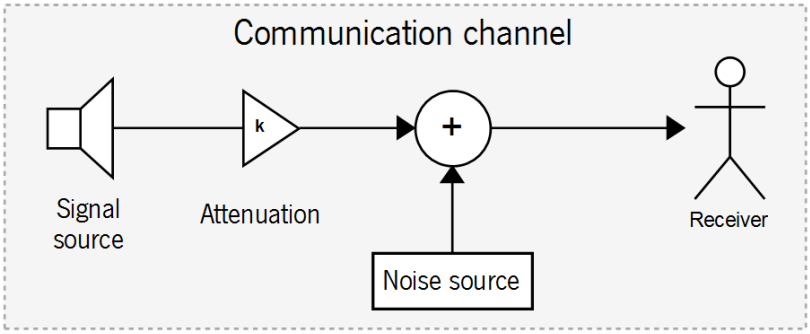

Figure 2-3: *Underwater channel equivalent model.*

Based on this model, shown in, Figure 2-3, the signal S_R received by a certain hydrophone, represents the emitted signal S_E multiplied by the attenuation plus the ambient noise.

$$S_R = S_E * A_{tt} + A_N \quad (1)$$

2.1.1 Sound propagation and attenuation

Attenuation is one of the most important properties regarding underwater acoustic channels because it is present in all types of underwater environments, and its value increases with an increase in distance and frequency [9].

Attenuation is made up of three main components: spreading loss, absorption loss and scattering loss [11] but, for this dissertation's purposes, the attenuation that occurs in an underwater acoustic channel over a distance l, for a signal of frequency f is given by equation 2, where k is the spreading factor, which describes the geometry of propagation (typically 1.5 is used for practical spreading) [12], and $a(f)$ is the absorption coefficient, expressed in dB.

$$A(l,f) = l^k a(f)^k \tag{2}$$

Figure 2-4 shows how distance and frequency affects the attenuation of a signal under water. It can be seen that a 1 MHz signal suffers an attenuation of 350 dB when transmitted at a distance of 1 km. For lower frequencies, for instance 500 kHz, attenuation is only 150 dB.

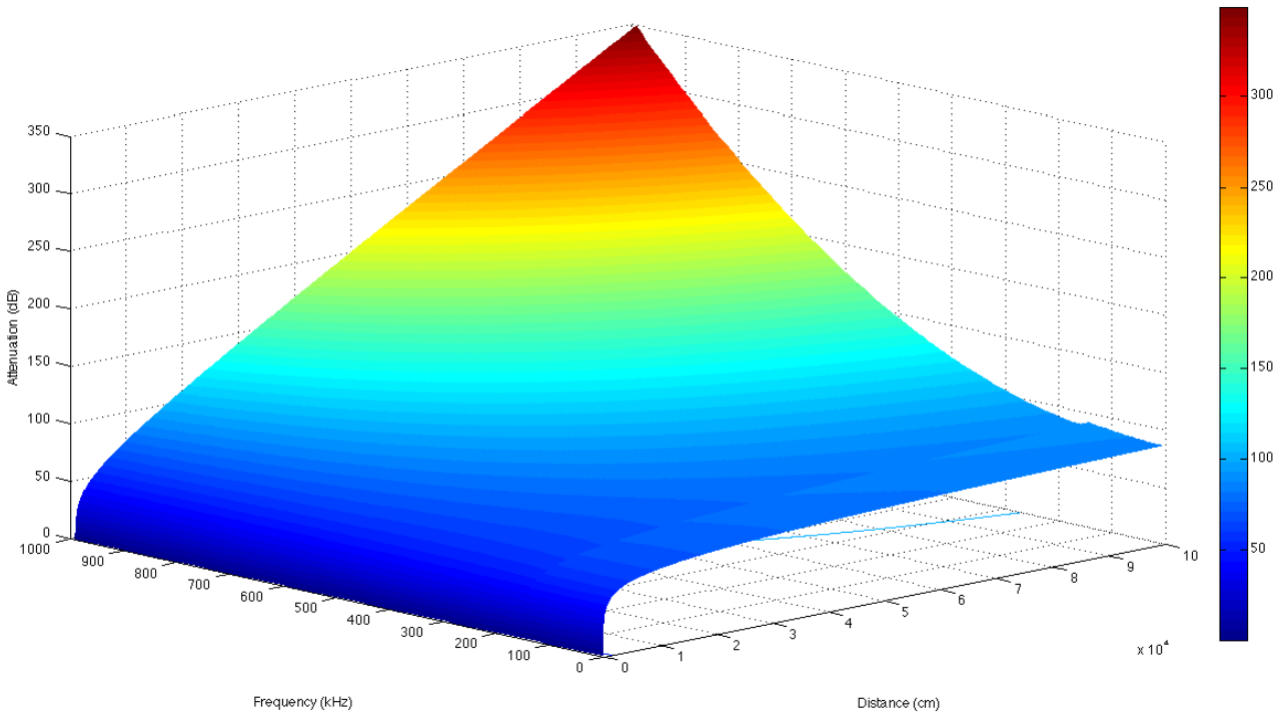

Figure 2-4: *Attenuation as function of frequency and distance* [9].

2.1.2 Noise types and sources

The noise present in an underwater acoustic channel can be classified in three types: man-made noise, site-specific noise and ambient noise. The man-made noise is made by human activities such as noise of machines, submarines and vassals. The site-specific noise exists only in certain places. The ambient noise is due to turbulence, rain, breaking waves, and maritime activity [9], Figure 2-5 shows some sources of noise existing in aquatic environments.

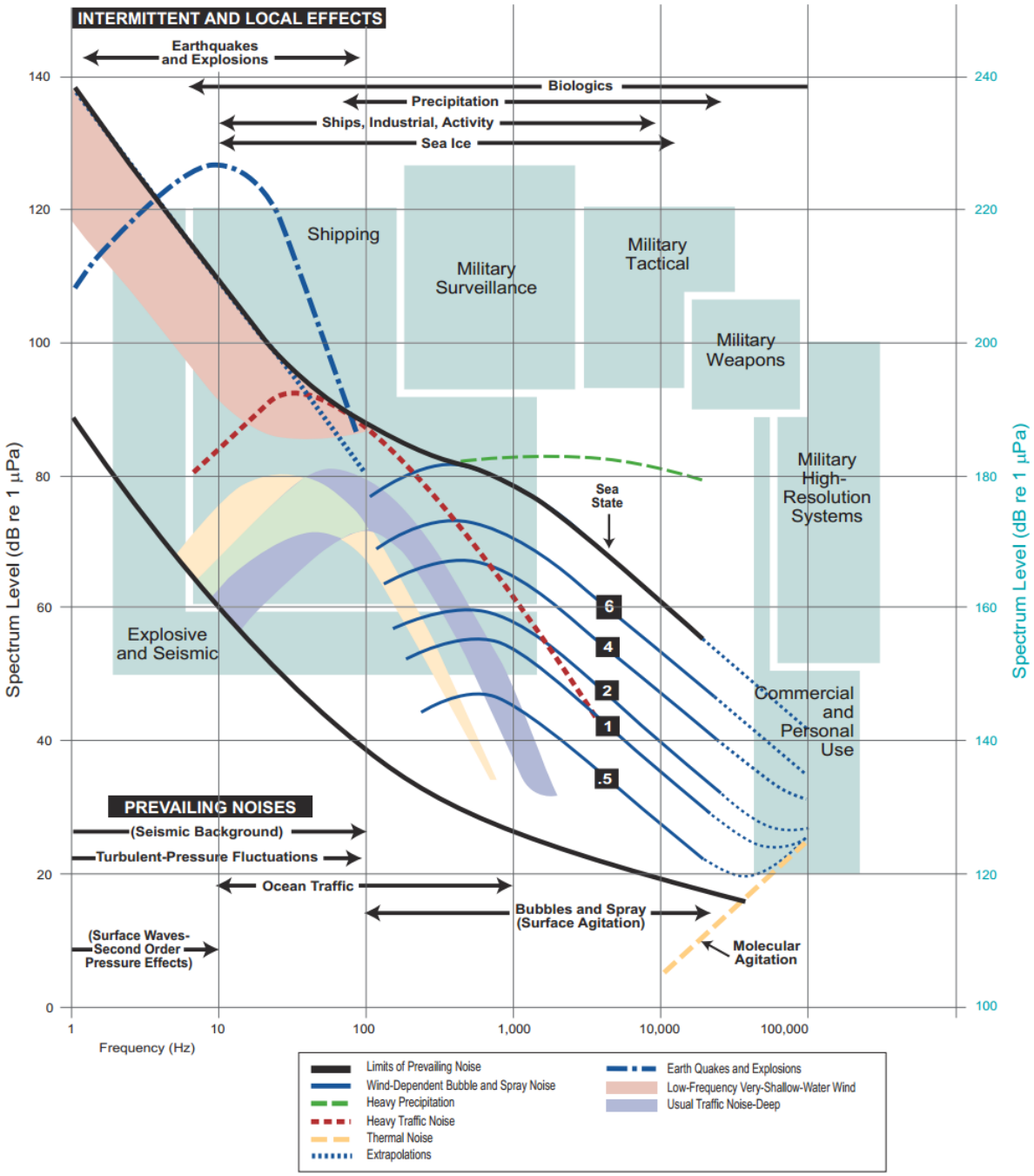

Figure 2-5: *Different sources of noise in the ocean* [13].

2.2 Typical applications for piezoelectric ultrasonic transducers

A transducer is a device that converts a signal in one form of energy to another form of energy. There is two types of piezoelectric ultrasonic transducers; the emitters or projectors and the receivers or hydrophones.

An ultrasonic emitter (or projector) converts electrical energy into mechanical energy and needs an external voltage source to operate, therefore consuming energy, while an ultrasonic receiver (or hydrophone) generates a signal when excited by a mechanical wave, i.e, converts mechanical energy into electrical energy.

Applications for ultrasound transducers range from military devices to medical imaging and industrial applications. Military devices, for example, such as the underwater SONAR system, uses sound waves to navigate, detect objects on or under water, such as other submarines.

In case of a SONAR, a signal is converted into acoustic waves by an underwater transducer, and sent through water. When the acoustic wave strikes something such as a fish or an object, it is reflected back. Then it is acquired and analyzed to decode useful information such as: size, composition, and shape of the object. The exact extent of what can be discerned depends on the frequency, power of the signal transmitted and sensitivity of the hydrophone being used.

Two types of technology share the name sonar: passive sonar is essentially listening for the sound made by vessels, submarines or fish and active sonar (Figure2-6) which emits pulses of sounds and listens for its echoes.

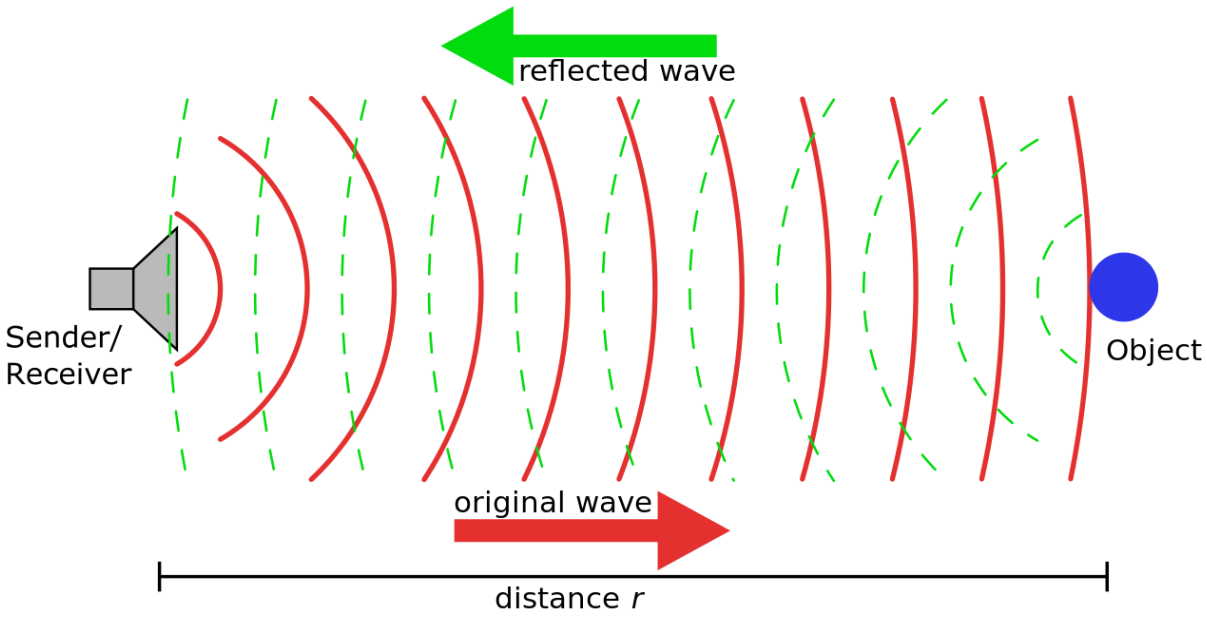

Figure 2-6: *Principle of an active sonar* [14].

In the cleaning industry, ultrasonic transducers are commonly used in small tabletop ultrasonic cleaners and medical applications like dental offices. This cleaning activity is based on the cavitation and implosion effect and as a result of ultrasonic activity displace and remove loosely held contaminants such as dust from surfaces. This method presents the advantage of not using any extra chemical product [15].

In sonars, the acoustic signal has low frequency and can reach several tens of kilometers. On the other hand, medical imaging works with higher frequencies, reaching hundreds of MHz, with signals reaching just few centimeters. Figure 2-7 depicts the operation of fish finder sonar.

For underwater communications, systems operate in frequencies between sonar and medical applications because of range requirements, making a tradeoff between range and frequency.

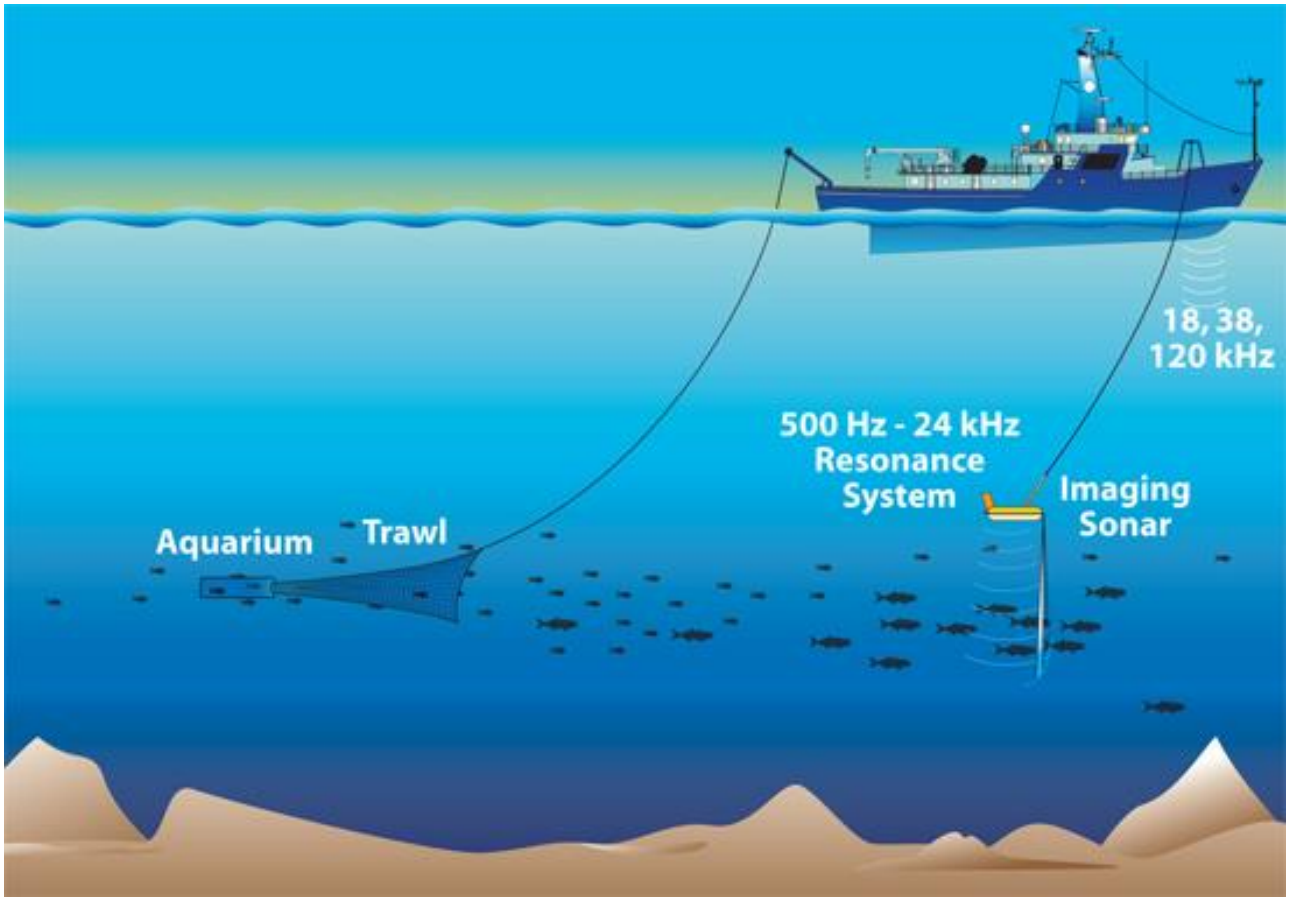

Figure 2-7: *Fish finder sonar* [16].

2.3 Overview of existing underwater acoustic systems

Ultrasonic transducers are used in a variety of applications. This applications range from military SONARs, fish-finder SONARs, seabed mapping SONARs, marine life listening devices and underwater communication systems.

From a structural point of view, these devices include some common parts, namely: a human interface device, usually a Liquid Crystal Display (LCD), a signal generator, a projector and (or) a hydrophone and a signal analyzer.

In the case of SONARs, the systems include a projector and a hydrophone, or use a single transducer acting as an emitter and receiver (Figure 2-8), while marine life listening devices only use a hydrophone and electronics to amplify the collected signal. Figure 2-9 represents a Cetacean Research Technology's SQ26-H1 Portable Underwater Recording System that includes a hydrophone and a digital recorder.

Figure 2-8: *Example of a sonar fish finder.*

Figure 2-9: Underwater Recording Systems

2.4 Piezoelectric ultrasonic emitters

A piezoelectric actuator generates a displacement when subjected to an electric field. This displacement is capable of applying a force and, therefore, the actuator is capable of doing work in the form of an acoustic wave.

There are several materials available for ultrasound transducers, such as: the Lead Zirconate Titanate (PZT), Lead Titanate (PT) and Lead Zinc Niobate (PZN) ceramics and Polyviylidenefluoride (PVDF) [11]. This study will focus on PZT ceramic and PVDF polymer transducers Figure 2-10 since these were the transducers developed by Marcos da Silva Martins[11].

Figure 2-10: *PVDF 4x28µm (Left), PZT 110µm (Top), PVDF 110µm (Right),*

However, there are several other options on the market. Beijing Cheng-cheng Weiye Science and Technology Co., Ltd, for example, provides a wide range of industrial ultrasonic emitters, like the CCH family [17].

Figure 2-11: *CCH Ultrasonic transducer family.*

2.4.1 Ultrasonic projector parameters

The CCH-5938D-25LB Figure 2-12 for example, which is used for ultrasonic cleaning, is a high efficiency, Static Capacity 5400 pF, high power, 60 W and a resonance frequency of 25 kHz [18].

Figure 2-12: *CCH-5938D-25LB ultrasonic emitter.*

This ultrasonic tubular transducer is used in distillation, cleaning, mix and mill for various chemical procedures. However, for this dissertation work it is intended to use different ultrasonic projectors, with different specifications like: area, thickness and number of layers, (Table 2-1).

Table 2-1: *Transducer capacitance.*

Transducer	Radius [cm]	Area [m^2]	thickness [m]	Layers	Capacitance [F]
reference 1cm^2 28µm		0,0001	2,80E-05	1	3,79E-10
piston 3.5cm 2x28µm	1,75	0,0009616	2,80E-05	2	7,30E-09
piston 3.5cm 56µm	1,75	0,0009616	5,60E-05	1	1,82E-09
piston 2cm 2x110µm	1	0,000314	1,10E-04	2	6,07E-10
piston 2cm 8x28µm	1	0,000314	2,80E-05	8	9,53E-09

Although the physical characteristics are important in these projectors, the parameter that matters for this work is the overall transducer's capacitance, which can be calculated using equation 3. This value is important because it is related to the projector current consumption, when driven at a certain frequency.

$$C = E_o E_r \frac{A}{d} N \tag{3}$$

Where C is the capacitance in Farad, E_o is the vacuum permittivity (8,85E-12), E_r is the PVDF relative permittivity to the vacuum (12), A is the area in meters, d is the thickness in meters and N is the number of layers.

2.5 Piezoelectric ultrasonic receiver

Hydrophones convert the underwater sound into an electrically signal, consequently the electrical properties of the transducer are important. There are different hydrophones in the market such as SQ48 Broadband Hydrophone from Shanghai Enou Technology Ltd (Figure 2-13) and C304XR from Cetacean ResearchTM Technology (Figure 2-14).

Figure 2-13*: SQ48 Broadband Hydrophone.*

Figure 2-14: *C304XR Hydrophone*

The hydrophone used was a Cetacean Research™ C304XR which has a sensitivity of -201 [dB re 1V/µPa], a preamplifier gain of 20 dB and an effective sensibility of -181 [dB re 1V/µPa]. In terms of frequency, it presents a linear frequency range (±3 dB) between 0.012 and 1000 kHz and a frequency range (+3/-12 dB) between 0.005 and 2000 kHz. The output impedance is 10 Ω.

2.5.1 Existing ultrasonic preamplifiers

An ultrasonic preamplifier is a voltage amplifier that is placed between the hydrophone and its amplifier in order to provide sufficient gain or broadband signal-to-noise enhancement for optimum acquisition. Preamps can also be used to compensate for amplitude losses caused by very long cables, between the transducer and the test instrument, to improve signal-to-noise ratio. In general, a preamplifier can be used in almost any application where additional gain is required for optimum performance.

The hydrophone preamplifier must be an Ultra-Low Noise Amplifier (ULNA), because it is in the path of very small signals, otherwise inserts noise in the signal of amplitude equivalent to the signal itself, reducing the SNR. If that happens, the signal may not be recoverable even through filtering.

Some hydrophones already include a preamplifier from factory, others don't. Some examples of ultrasonic preamplifiers are the AQ-201 (Figure 2-15), with a gain of 26 dB over a bandwidth of 140 kHz, an input referred noise (IRN) of 100 nV/$\sqrt{}$Hz.

The Shanghai enzhou Instrument Co., LTD (Figure 2-16) offers a differential input and output preamplifier (SA03) which has a 40 dB gain over a Bandwidth of 4 Hz to 80 kHz.

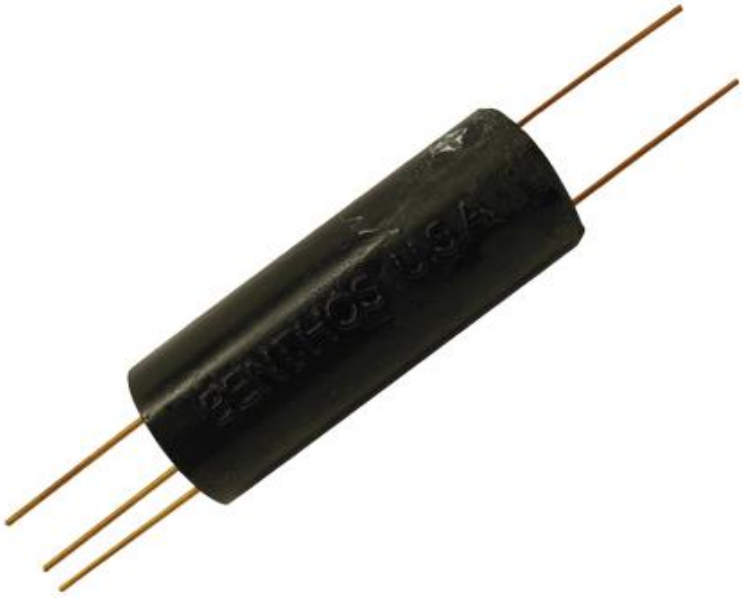

Figure 2-15: *AQ-201 Preamplifier*

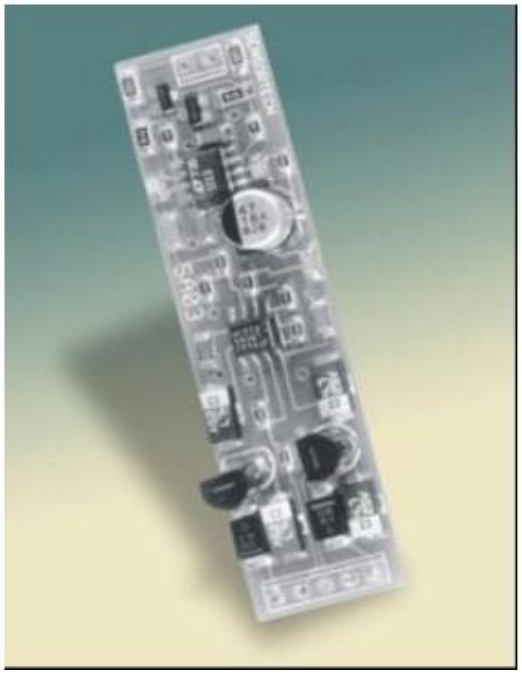

Figure 2-16: *SA03 Differential preamplifier*

Chapter 3

3 System analyses

The system analysis aims clarify the goal of the project, what challenges were expected to be faced and also decompose the system in simpler parts to simplify the development phase.

The objective of this dissertation work is the development of an acoustic modem for underwater communications. It includes the project of an ultrasonic emitter and receiver to drive ultrasonic transducers at frequencies of 4 MHz

3.1 System requirements

Requirements are divided into functional and non-functional requirements. The functional requirements are those that describe specific behaviors of the system. Non-functional requirements are requirements that derive from functional requirements. For instance, if it is a requirement (functional) for the system be usable onboard, it is a (non-functional) requirement the usage of a dedicated battery or the operation with the boat's power supply voltage.

3.1.1 Functional requirements

- The system has to be pluggable in an ordinary computer through a Universal Serial Bus (USB) port.
- The system has to drive a transducer with a sinusoidal signal between 3.3 Vpp and 24 Vpp;
- The sinusoidal signal has to vary in frequency between 100 kHz and 4 MHz;
- The system has to read and amplify signals between 100 kHz and 4 MHz;
- The system has to read and amplify signals between 100 μVpp to 11.22 V;
- The system must be programmable on-the-fly without any key pressing or jumper setting;

3.1.2 Non-functional requirements

- The system has to be powered from 230 V AC and from a 12 V battery;
- The overall system has to be transported easily in a single case;
- The system has to operate long hours without overheating;
- The system has to be enclosed in an inaccessible case;
- Two systems must be able to operate in the same channel, one as emitter and one as a receiver.

3.1.3 Use cases

To meet requirements, the user must be able to: upload the firmware, configure hardware, send a string and receive a string. These are the required use-cases and can be seen in Figure 3-1.

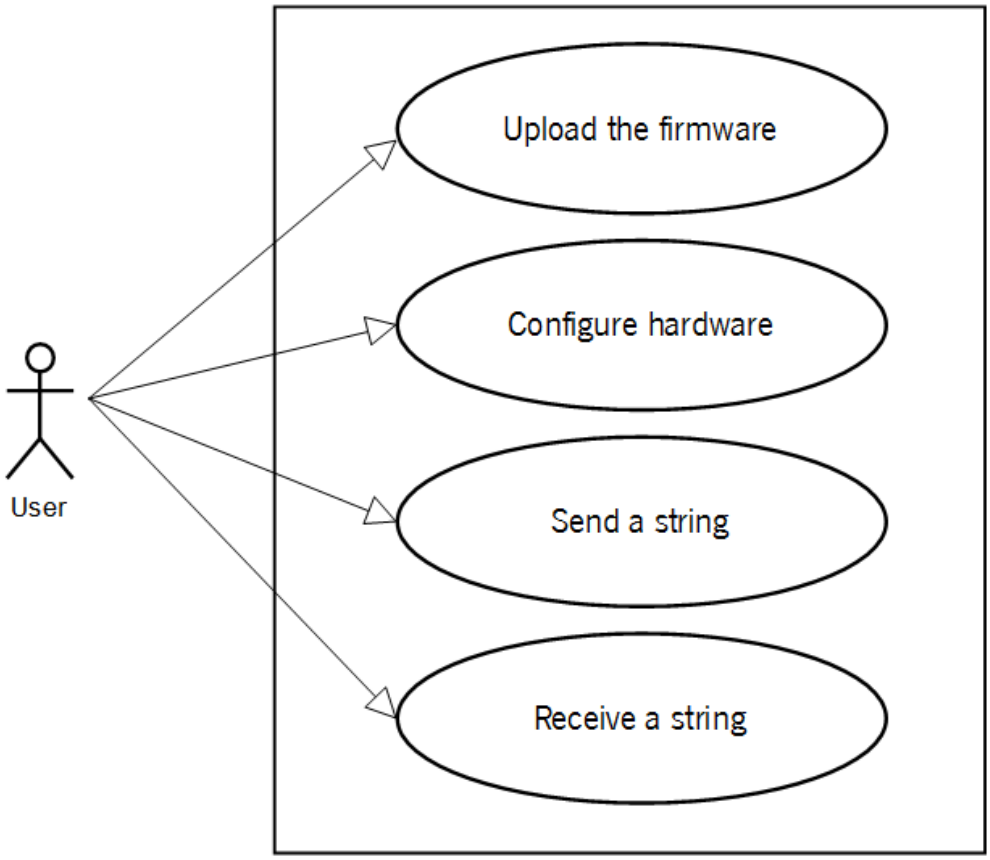

Figure 3-1: *UML use case diagram*

3.2 System Structure

From the developer point of view, the system is divided into three main layers, namely: application layer, hardware layer and physical layer.

At the application layer, the system performs the user interface, the data processing and retrieving process, and handles the communications with the hardware layer.

The hardware layer responds to the application layer, in a slave mode. At this layer, the data coming from the application is decoded and modulated and amplified in voltage and power to be sent to the physical layer. In a similar way, the data coming from the physical layer is acquired, demodulated and sent to the application.

The physical layer is basically composed by both transceivers, the emitter and receiver, and the water channel itself. The ultrasonic emitter is polarized with a voltage signal, generates an acoustic wave, which propagates through the water and reaches the hydrophone, where the effect reverses itself. In the hydrophone, the pressure wave generates a voltage signal, which is passed into the hardware layer.

This structure can be seen in Figure 3-2.

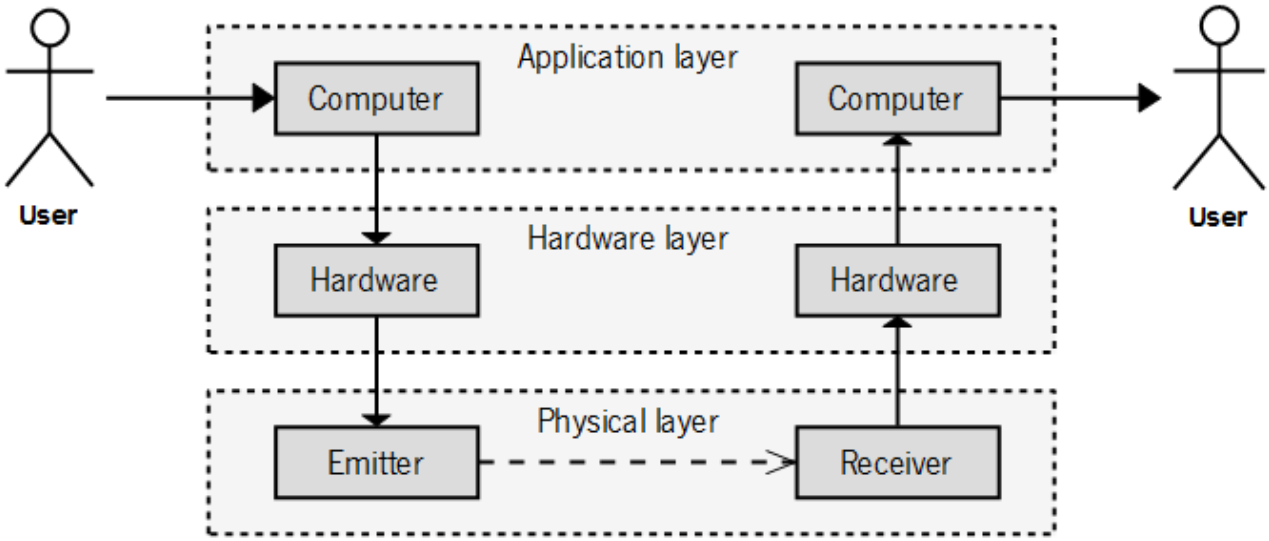

Figure 3-2: *System structure.*

3.2.1 Interconnection diagram

The hardware connection between the three layers, mentioned above, is chosen based on the data types been exchanged and the expected symbol rate. Therefore, as mentioned in chapter 2, the connection between the computer, where the application layer is implemented and the microcontroller, which is part of the hardware layer, should be USB.

The decision to use a USB connection is based on the fact that this connection protocol enables high bandwidth, 480Mb/s in case of USB2.0 [19], which is enough for this project's requirements, and presents also the advantage of being the most used connector in computers and mobile devices, which meets other requirements.

The connection between the hardware layer and the physical layer is divided in two. One connection for power, connecting the power amplifier and the ultrasound emitter, composed by a standard power cable and a coaxial cable connecting the hydrophone and the instrumentation circuitry. These connections are depicted in Figure 3-3.

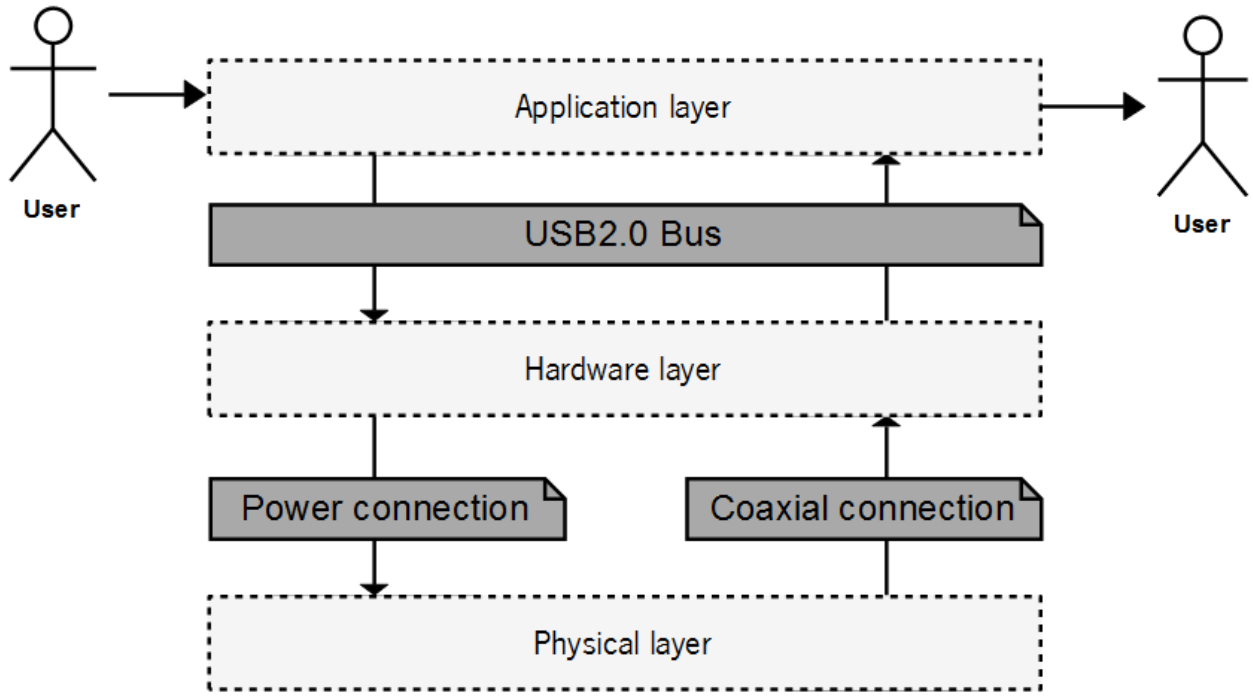

Figure 3-3: *Hardware connection between system layers.*

3.2.2 Software stack layer

At the application layer, the system must perform the user interface and the USB communication handling routines. These two different tasks should be as independent as possible to provide abstraction. Consequently, the USB communication detail shouldn't be visible from the application point of view and in a similar way, the user interface shouldn't be sensitive to the interface medium.

Ideally, any of the previous layers should be changed without affecting the other, because they should be independent has the diagram suggests in Figure 3-4.

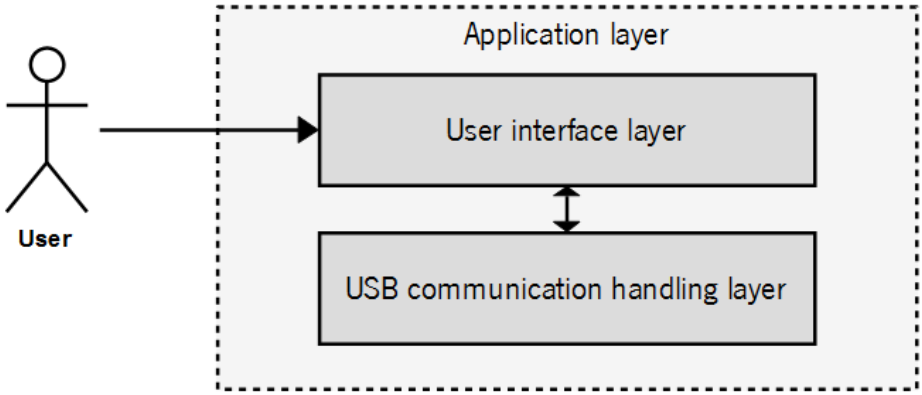

Figure 3-4: *Application layer*

3.2.3 Physical layer

The physical layer is composed by the projector transducer and the hydrophone and the underwater channel itself. The projector, as expressed in the previous chapter, is a capacitive device that is subjected to the hardware layer output signal and generates an acoustic wave. The receiver or hydrophone, is exposed to the acoustic waves, under the water and generates an electrical signal that, is fed to the instrumentation circuitry at the hardware layer.

The overall physical layer can be depicted in Figure 3-5.

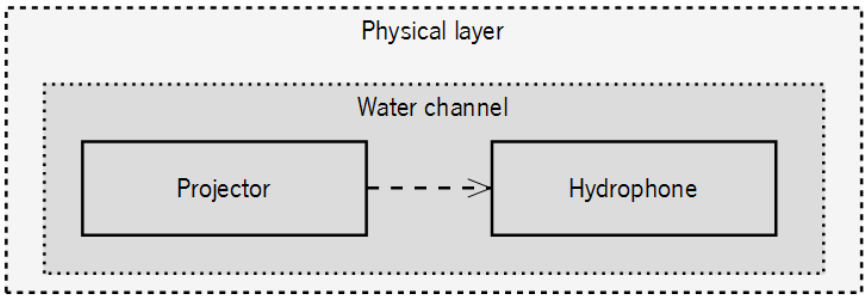

Figure 3-5: *Physical layer*

3.2.4 Hardware stack layer

At the hardware level, the signal path is divided into output signal (going out the modulator) and input signal (coming into the demodulator). Both the input and output signals exist in analog and digital forms.

The output signal, enters the hardware layer at the microcontroller, through the USB2.0 bus. Then, the microcontroller feeds the modulator (implemented in the Field-Programmable Gate Array (FPGA) with one byte at a time. The modulator processes the received bytes and generates a 14 bit word to drive the DAC, which generates an analog signal. From this point on, in the signal path, the signal assumes the analog form. The generated analog signal is then amplified in voltage and power, and applied to the ultrasonic projector, which is part of the physical layer.

The input signal enters the hardware layer through the hydrophone, it is filtered, amplified and then gets sampled by the ADC. From this point on, in the input signal path, the signal is digital. After sampling the signal it is converted in a 14 bit word, which is passed to the demodulator that, at its turn, feeds the microcontroller with a byte.

The input and output signal path are represented in Figure 3-6.

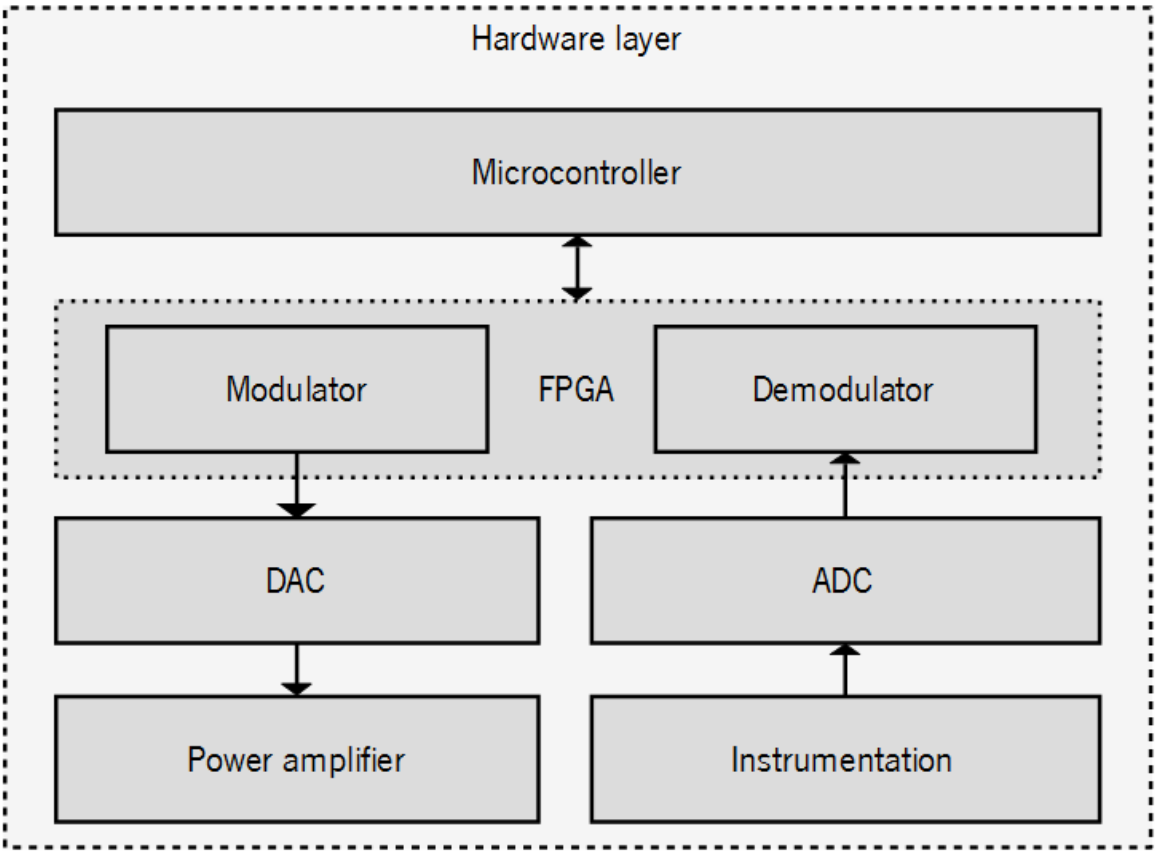

Figure 3-6: *Hardware layer*

3.3 Development considerations

To successfully meet the system requirements, several constraints, in different sections, had to be analyzed. These constraints range from the operating system, all the way down to the physical layer. The understanding of these constraints were very important because those were used as guidelines to optimize the system as much as possible, early in the design phase. This way, the first implementation was expected to be less buggy than otherwise.

In the following subsection of this chapter, those constraints are analyzed and understood one by one. In the next chapter, at the design phase, the appropriate consideration to overcome these issues were presented.

3.3.1 Hydrophone signal acquisition considerations

The receiver sensitivity Rs of a hydrophone, expressed in dB, is the ratio between its response and a standard response. The hydrophone's response is the voltage that it generates when subjected to the sound pressure of the fluid surrounding it. The standard response for hydrophones, in underwater environments is $1\ V/\mu Pa$.

Based on [20], [21], the receiver sensitivity of an hydrophone, Rs, of a receiver can be calculated using equation 4 where V_{out} is hydrophone the response in the fluid and, V_{ref} is the standard response hydrophones in underwater environment.

$$Rs = 20 * log_{10}(\frac{V_{out}\ [V/\mu Pa]}{V_{ref}\ [V/\mu Pa]}) \tag{4}$$

Considering $V_{ref} = 1\ [V/\mu Pa\ ]$, and solving 4 in order to V_{out}, it is obtained 5, which expresses V_{out} in $[V/\mu Pa]$ as function of the receiver sensitivity. This way, equation 5 allows to obtain the response for a particular hydrophone, knowing its sensitivity. Thus, for $Rs = -181\ dB$, applying 5, $V_{out} = 8.91 * 10^{-10}\ [V/\mu Pa]$.

$$V_{out} = 10^{\frac{Rs}{20}} \tag{5}$$

This value can be converted to $[V/Pa]$ by multiplying V_{out} by $1 * 10^{6}$. Therefore, for the Cetacean Research™ C304XR hydrophone, the final response is $891 * 10^{-6}\ [V/Pa]$

The maximum output voltage V_{out_max} expected to be generated by the hydrophone depends on its RMS Overload Accoustic Pressure (RMSOAP) parameter, which assumes a maximum value of $202\ dB\ [re\ 1uPa]$. Thus, $V_{out_max} = 8.91E^{-10}\left[\frac{V}{\mu Pa}\right] * 10^{\frac{202}{20}}\ [\mu Pa] = 11.222\ V$

Therefore, this hydrophone has a sensitivity of $8.91E^{-10}\ V/\mu Pa$ or $891\ \mu V/Pa$ and is capable to generate a signal smaller or equal to $11.222\ V$ between the *SignalOut* and Gnd pins (Figure 3-7).

Figure 3-7: *Cetacean Research™ hydrophone pinout.*

3.3.2 Cable considerations

To transmit the signal from the hydrophone to the instrumentation circuitry, a $10\ m$ cable was used. The cable (Figure 3-8) has four wires and an outer shielding net. The outer shielding net was connected to the hydrophones' Gnd pin. Each wire of the selected cable, has a resistance of $900\ m\Omega$ and a parasitic capacitance of $2.2\ nF$ between it and each of the nearby wires.

Figure 3-8: *C304XR Hydrophone and cable.*

3.3.3 Noise considerations

Since it is a requirement for the system to emit and receive the signal in a band between $f_L = 100\ KHz$ and $f_H = 4\ MHz$ and, given the fact that the used cable acts as a Low Pass Filter (LPF) blocking signals of frequency above f_H, only a input High Pass Filter (HPF) is required to remove signals bellow f_L.

The required HPF blocks signals of frequency bellow $f_L = 100\ KHz$ while the LPF implemented by the cable, rejects signals of frequency above $f_H = 4\ MHz$. Thus, the HPF and the LPF, in series, form a Band Pass Filter (BPF).

3.3.4 Preamplifier considerations

The preamplifier to be implemented has to be projected to have a low input noise in order to be able to amplify very small signals without reducing its Signal o Noise Ratio (SNR), ideally amplify a $8.91\ \mu V$ signal, because $8.91E^{-10}\left[\frac{V}{\mu Pa}\right] * 10E^{3}\ [\mu Pa] = \ 8.91E^{-6}\ [V]$. The highest input impedance possible, to reduce the energy requirements to the hydrophone. The maximum input voltage of $11.222\ V$ to be able to read the hydrophone's full voltage range. The maximum Power Supply Rejection Ration (PSRR) to reduce the power supply noise influence in the amplified signal and a maximum output current to drive the upstream circuitry.

3.3.5 Variable gain amplifier considerations

The gain applied to the received signal must be variable, in order to maintain the signal in the ADC acquisition range. Therefore, a Variable Gain Amplifier (VGA) must be used to enable the system to change its gain dynamically.

Based on the hydrophone parameters, it can generate a signal between $8.91\ \mu V$ and $11.22\ V$, and the ADC's acquisition range is $1\ V$. Therefore a gain G has to be applied to the signal, and so, when the input signal is $11.22\ V$ the gain of $G_{max} = 20 * log_{10}\left(\frac{1}{11.222}\right) = -21\ dB$ has to be applied to the signal and when the signal is $8.91\ \mu V$ again of $G_{min} = 20 * log_{10}\left(\frac{8.9E^{-6}}{1}\right) = 101\ dB$. This way, although the input signal's amplitude may vary, the voltage at the ADC is in the acquisition range.

3.3.6 Variable gain control unit considerations

The gain of the VGA is digitally set. Thus, a logic unit was created in the FPGA to abstract the details of the gain setting procedure from the demodulator. This way, the interface between the demodulator and the Variable Gain Control Unit (VGCU) consists in a generic signal through which the demodulator requests the desired gain to the VGCU and the VGCU decodes the request.

3.3.7 ADC considerations

The signal to acquire has a maximum frequency $f_H = 4\,MHz$ and, based on the Nyquist sampling theorem, must be sampled at the sampling frequency $f_s = Nf_H$ where $N \geq 2$. As the hardware permits, N was taken as $N = 6$, therefore $f_s = 24\,MHz$. The variable N was taken as 6 because is a multiple of the FPGA's main clock source and, based on the Nyquist sampling theorem, is large enough to provide a reasonable approximation between the analog signal and its discrete representation.

Being $f_s = 24\,MHz$ and based on [22], a LPF is required to filter the signal before sampling. This filter has to remove any signal component with $f \geq {f_s}/{2}$.

Because ${f_s}/{2} > f_H$ the LPF can be designed to have a cutoff frequency of f_H. This way, its attenuation is greater at ${f_s}/{2}$. Figure 3-9 show antialiasing filter requirements for a clean sampling.

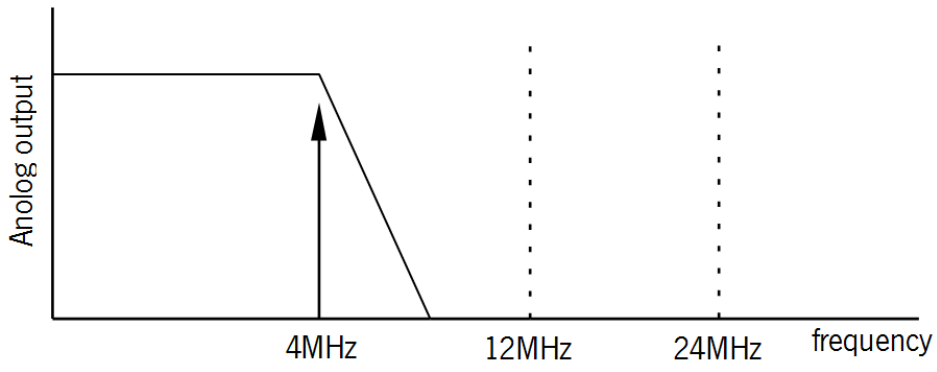

Figure 3-9: *Antialiasing filtering requirements.*

After filtering, the signal is converted from single end to differential, and an offset V_{cm} is added, required to enter the ADC according to its specifications. The ADC samples the signal and converts it to a 14 bit word, which feeds the demodulator, implemented in the FPGAs.

3.3.8 Demodulator considerations

The demodulator is a logic module that receives a 14 bit word from the ADC, stores it to build an array of samples and converts it into a byte which is passed to the microcontroller. The demodulator also sets the VGA value, according to signal strength and demodulation techniques being used.

3.3.9 Modulator considerations

The modulator and demodulator perform inverse tasks. The demodulator logic unit receives a byte from the microcontroller and generates a signal to be converted to analog, based on the modulation being used. Then, a sequence of 14 bit words is generated to be sampled by the DAC.

3.3.10 DAC considerations

Since the system is required to generate an analog signal of frequency $f_a = 4\,MHz$, the DAC's sampling frequency must be $f_s \geq Nf_a$, where $N \geq 2$. Therefore, choosing $N = 6$, the sampling frequency is $f_s = 24\,MHz$. The variable N was also taken as 6 because is a multiple of the FPGA's main clock source and, based on the Nyquist sampling theorem, is large enough to provide a reasonable approximation between the digital signal and its analog version.

3.3.11 High frequency power electronics considerations

Because several transducers are intended to be used, the transducer parameters aren't known, since the project has to be transducer independent. Thus, it as to be assumed the worst case scenario, which is the transducer with highest capacitance and the maximum frequency of the analog signal $f_a = 4\,MHz$. Table 3-1 shows all five transducers current consumption at $30\,V$ and $f_a = 4\,MHz$.

Table 3-1: *Transducers power consumption.*

Transducer	Capacitance [F]	Frequency [Hz]	Impedance Zc [Ω]	Voltage [V]	Current [A]
reference 1cm^2 28µm	3,79E-10	4,00E+06	104,91	30	2,86E-01
piston 3.5cm 2x28µm	7,30E-09	4,00E+06	5,45	30	5,50E+00
piston 3.5cm 56µm	1,82E-09	4,00E+06	21,82	30	1,37E+00
piston 2cm 2x110µm	6,07E-10	4,00E+06	65,63	30	4,57E-01
piston 2cm 8x28µm	9,53E-09	4,00E+06	4,18	30	7,18E+00

The impedance of a emitter can be calculated using equation 6, which expresses $Z_c\ [\Omega]$ as function of frequency f.

$$Z_c = \frac{1}{j\omega C}[\Omega], \quad \omega = 2\pi f \tag{6}$$

Meaning while, its current consumption is given by equation 7.

$$I_c(t) = \frac{V_c(t)}{Z_c} \tag{7}$$

Combining equation 6 and equation 7, it can be seen that the current consumption on an ultrasonic emitter depends on the applied voltage and the transducer impedance, which depends on the frequency f of the signal and the capacitance C of the transducer. While the applied voltage can be fixed throughout the device operation, the impedance

Figure 3-10 plots the current consumption of the piston type 8x28 µm 2 cm hydrophone, (Table 3-1) when subjected to a 30 V sin wave of frequencies between 100 kHz and 4 MHz. in the same plot it can be verified that the current consumption increase exponentially with the frequency. This result poses major challenges when operating in ever increasing frequencies.

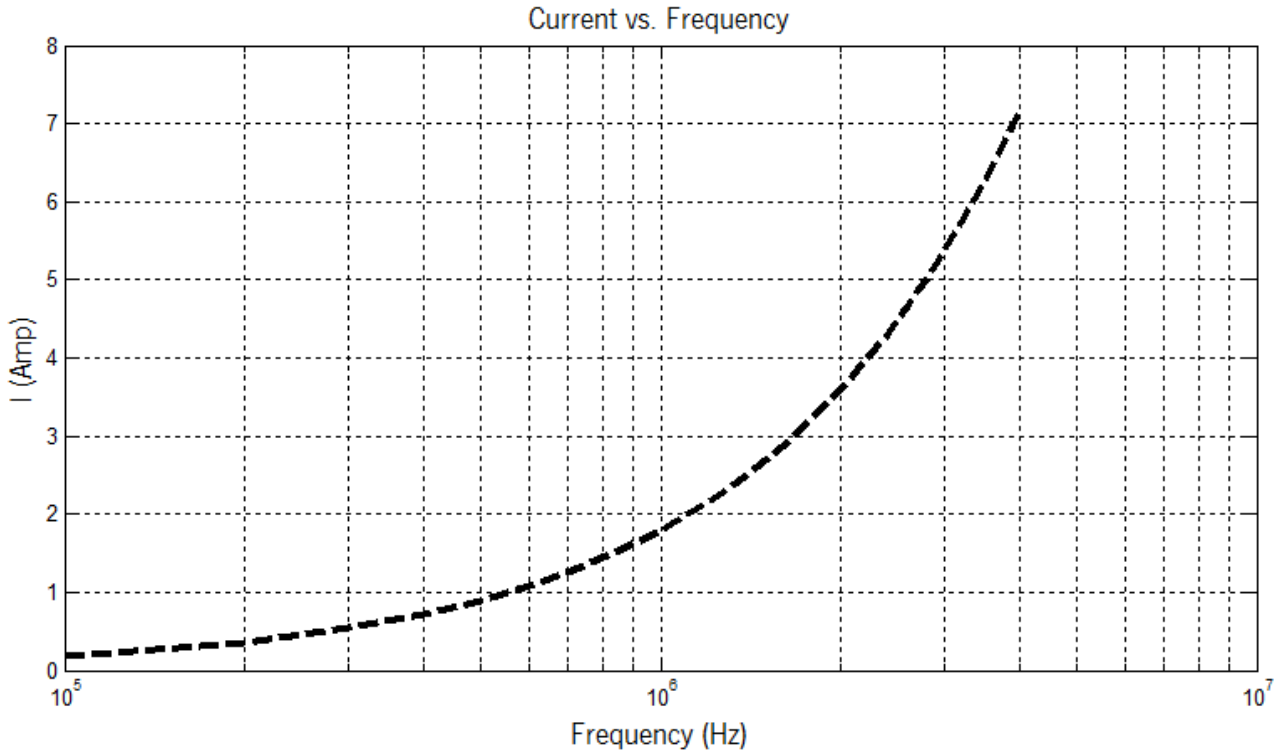

Figure 3-10: Capacitor current consumption over frequency

3.3.12 Logic system considerations

The logic system, running in the FPGA, implements the modulator, demodulator, a variable gain unit and the logic to interface the microcontroller.

The modulator and demodulator logic units are likely to be redesign in future works, out of the scope of this work, for modulations and demodulations improvement, while the logic to interface the microcontroller and the variable gain unit aren't. That way, to simplify future interventions, the logic system is divided in two different layers, an interface layer and a data processing layer.

The interface layer includes the logics to interface the modulator and the demodulator with the external world, which is the microcontroller's interface logic, the variable gain unit, the DAC and the ADC, and its functionality is to route data in and out of those units that are likely to be changed with frequency.

The processing layer is composed by the modulator and demodulator and it's planned to be the easily changeable.

3.3.13 Firmware considerations

The microcontroller interfaces the host computer and the FPGA. It is required to be used to avoid implementing the USB controller in the FPGA. Its function is to deliver the data received from the USB Bus to the modulator and retrieve data from the demodulator to deliver to the host. This data exchange is made through an USB connection.

Because the microcontroller has First In, First Out (FIFO) memories to buffer the USB data, two FIFOs are reserved for this project. One for input and other for output. The input FIFO holds data coming from the demodulator, while the output FIFO stores the data going to the modulator.

3.3.14 USB communication considerations

Despite the target baud rate of 1 Mbps, and the possibility of the system to operate in full duplex, which would be translated in 2 Mbps, the communication link between the hardware and the host computer as chosen to make possible larger baud rates, just in case the physical layer is improved.

The used USB connection, the USB2.0 is capable of transferring 480 Mbit/s. This way, the system bottleneck is transferred to the instrumentation and physical layer.

3.3.15 Application level considerations

The system being developed is not a complete communication system but, instead, an implementation of the first layer of the Open Systems Interconnection (OSI) model. Therefore, the application software to run on the host isn't the main target of this dissertation work. However, an application was developed to send a string and listen to its echo. This way, more complex applications can be developed on the top of it.

3.4 Power considerations

As described in the functional requirements, the system has to be powered from a 230 V AC as well as from a 12 V battery to make it possible to be carried onboard, for example. This requirements implies that both the signal power amplifier and the FPGA, including the receiver instrumentation, have to be able to work when connected to the grid as well as to an ordinary battery.

To supply power to the system from the electric grid, which is 230 V AC, two computer power supply were used, one for the FPGA board and other for the signal power amplifier. The power supply used for the FPGA board, was a 230 V AC to 16 V DC converter, and the one used for the signal power amplifier was a 230 V AC to 24 V DC converter.

To supply power to the FPGA board and instrumentation from a 12 V battery, no special precautions have to be taken into consideration because it works properly with voltages between 10 V and 16 V. Meaning while, to supply power to the signal power amplifier, a Step-Up converter was used to convert the 12 V into 44 V, which is the minimum voltage required for the power amplifier to work properly.

Chapter 4

4 System design

The proper approach to guarantee the quality and correctness of hardware and software design includes validation techniques such as simulation and testing. The application of these techniques ensures the correct relationship between a specification and the corresponding implementation.

The previous chapter, which described the analysis phase, was intended to decompose the system into small subsystems and make it possible to analyze them independently from each other. That goal was accomplished and, from this chapter on, until the integration phase, the system is treated as a group of subsystems. This way, the level of complexity was decreased significantly.

Chapter 4, covering the system design phase, aims to start from issues discussed at the analysis phase and present a solution for those. The solutions for the challenges, described in the analysis phase, are expected to be known at the end of this chapter. For that to be accomplished, the proposed solutions were simulated and validated.

4.1 Instrumentation design

The instrumentation is the hardware involved in the acquisition, filtering, amplification and sampling of the hydrophone signal. These hardware stages were divided into several modulus as described in chapter 3. These modules are the hydrophone selection switch, the VGA unit, the antialiasing filter and the ADC (Figure 4-1).

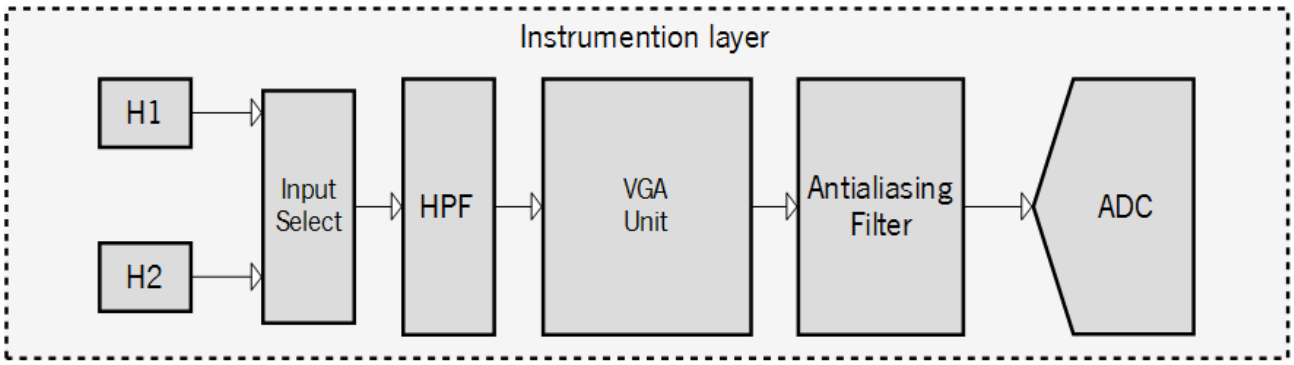

Figure 4-1: *Instrumentation modules diagram.*

These modules are designed separately and are presented in the following sections.

4.1.1 ADC module

The selected ADC was the AD9244 from Analog Devices. This Integrated Circuit (IC) was selected because it is fairly low price and meets all the requirements needed for the project, such as 14-bit at 40 MSPS, low power, 300 mW at 40 MSPS, $2Vpp$ differential full-scale analog input range and single 5 V analog supply. The $3.3\ V/5\ V$ digital interface simplifies the FPGA interface.

The ADC was configured in a $2\ Vpp$ differential input, with a common-mode voltage V_{CM} of $2.5\ V$ as shown in Figure 4-2.

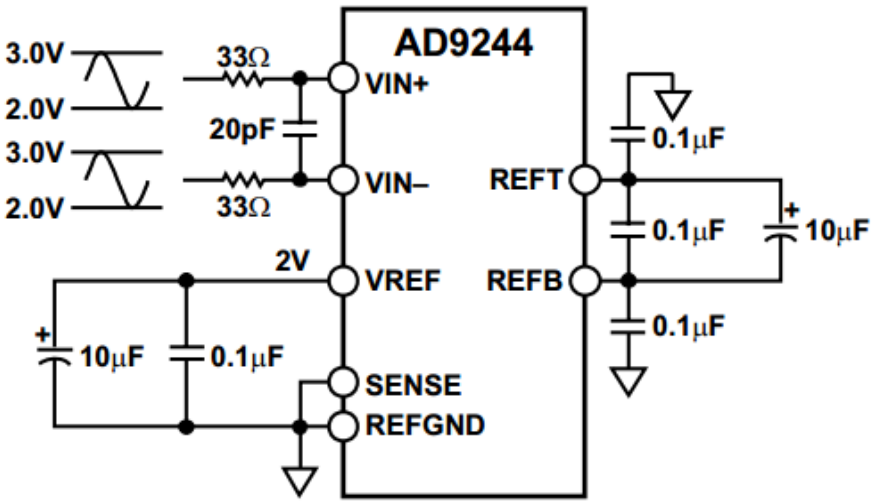

Figure 4-2: *ADC in 2 Vpp differential input.*

Besides that, it has a straight binary or twos complement output data mode selection by a Digital Format System (DFS) and an OuT-of-Range (OTR) indicator (Table 4-1) which indicates when the analog input voltage is beyond the input range of the ADC.

Table 4-1: *ADC's output data format.*

Input (V)	Condition (V)	Binary output mode	Twos complement mode	OTR
VIN+ - VIN-	< -1V	00 0000 0000 0000	10 0000 0000 0000	1
VIN+ - VIN-	= -1V	00 0000 0000 0000	10 0000 0000 0000	0
VIN+ - VIN-	= 0V	10 0000 0000 0000	00 0000 0000 0000	0
VIN+ - VIN-	= 1V	11 1111 1111 1111	01 1111 1111 1111	0
VIN+ - VIN-	> 1V	11 1111 1111 1111	01 1111 1111 1111	1

4.1.2 Antialiasing filter

The antialiasing filter to use before the ADC, has to be a LPF. This filter has to remove, with a significant attenuation signals of frequencies equal or above 12 MHz. This filter could be implemented in a passive or active topology. However, some manufactures provide integrated solutions in the form of a single IC, thus reducing the Printed Circuit Board (PCB) space.

For this antialiasing application, it was chosen the LT6600-5 from Linear Technology, because it is a very low noise differential amplifier (Figure 4-4), with an internal 0.5 dB ripple 4th order 5 MHz LPF (Figure 4-4) and has a dedicated pin for setting the output common mode voltage of the differential amplifier. These features are aligned with the ADC and provide very good anti-aliasing solution, as it can be seen at the gain plot(Figure 4-3) where the gain is 55 dB at the Nyquist frequency.

For the LT6600-5 to insert the minimum noise possible in the signal, i.e, to present the lowest possible noise density at the required frequency, it has to be configured with a gain of 4, or 12 dB (Figure 4-4).

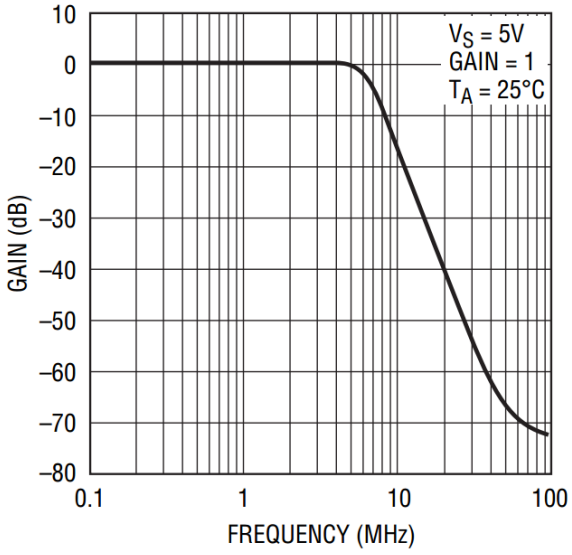

Figure 4-3: LT6600-5 Gain plot.

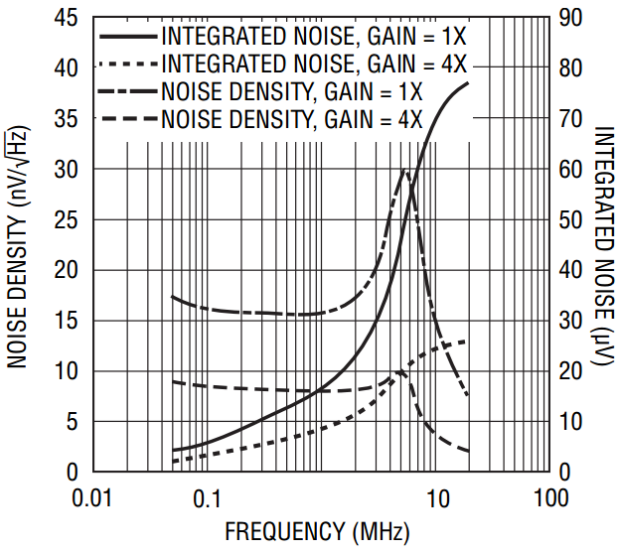

Figure 4-4: *LT6600-5 Noise density plot.*

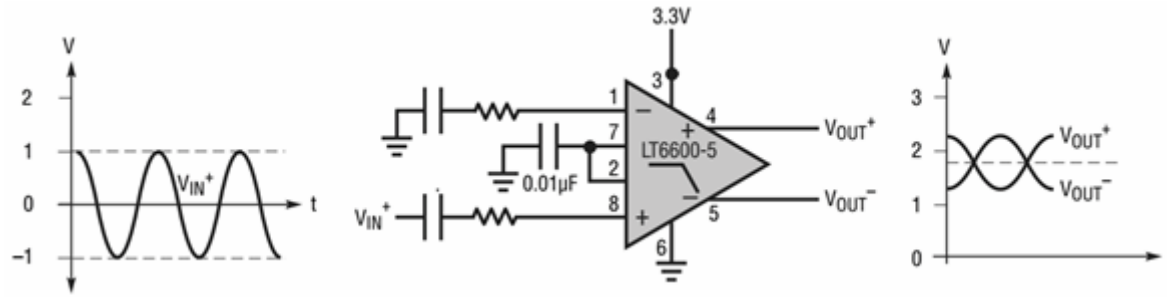

Figure 4-5: *LT6600-5 Configuration circuitry.*

4.1.3 Variable gain amplifier unit

The antialiasing filter inserts a fixed gain of 12 dB in the signal. Therefore, for the signal to reach the ADC with 1 V or $0\ dBV$, the input of the differential amplifier admits a maximum of 250 mV or $-12\ dB$.

The VGA selected was the THS7001 from Texas Instruments (Figure 4-6). Because it includes fixed gain low noise preamplifier and a Programmable Gain Amplifier (PGA) which is digitally programmable in $6\ dB$ steps. The THS7001's PGA has also a range of $-22\ dB$ to $20\ dB$ Gain/Attenuation, output clamp protection, 70 MHz bandwidth, a 175 V/µs slew rate and a wide supply range ±4.5 V to ±16 V.

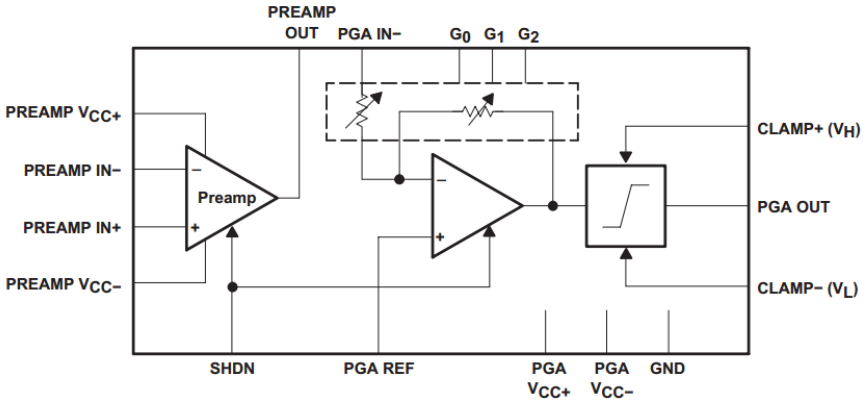

Figure 4-6: *THS7001 Block diagram.*

The THS7001 gain selection is made digitally by setting the value of a three bit field (G0, G1 and G2). The relation between G0, G1, G2 and the THS7001's gain is expressed in Table4-2. The THS7001's preamplifier has a bandwidth of 100 MHz, low noise figure of $1.7\text{nV}/\sqrt{\text{Hz}}$ and it was configured with a fixed gain of $6\ dB$.

Table 4-2: *Nominal Gain/Attenuation*

G_2	G_1	G_0	PGA GAIN (dB)	PGA GAIN (V/V)
0	0	0	−22	0.08
0	0	1	−16	0.16
0	1	0	−10	0.32
0	1	1	−4	0.63
1	0	0	2	1.26
1	0	1	8	2.52
1	1	0	14	5.01
1	1	1	20	10.0

Combining the THS7001's preamplifier and PGA's gains, this IC can apply a gain of $26dB$ ($20dB + 6dB$) to -16 dB ($-22dB + 6\ dB$) also variable in $6\ dB$ steps. Considering the THS7001's maximum output of $-12\ dB$, it's maximum input is $4\ dB$, $(-12\ \text{dB} - (-16\ \text{dB}))$ and it's minimum input is $-38\ dB$,$(-12\ \text{dB} - 26\ \text{dB})$. This means that the input signal has to enter the THS7001's between $12.589\ mV$ and $1.584\ V$.

Based on the VGA unit considerations, the input signal varies between $8.91\ \mu V$ and $11.22\ V$, which in decibels is $-101\ dB$ and $21\ dB$, respectively. Thus, with the THS7001's minimum and maximum input voltage of $-38\ dB$ and $4\ dB$, respectively, attenuation of $-17\ dB$, $(4\ dB - 21\ dB)$ has to be applied when the signal is $21\ dB[V]$ and a gain of $63\ dB$, $(-38\ dB - (-101\ dB))$ when the input is $-101\ dB[V]$.

Although the maximum gain of $101\ dB$ converts the minimum signal $-101\ dB[V]$ to 1 V and the minimum gain of $101\ dB$ converts the maximum signal $21\ dB[V]$ to 1 V, signals in between these values need different gains to be converted to the ADC's acquisition range.

Table 4-3 lists which gain should be applied for each input signal amplitude in intervals $6\ dB$.

Table 4-3: *VGA unit gain configuration.*

Vin (dB)	Fix gain amplifiers (dB)				THS7001 VGA (dB)			LT6600-5 HPF (dB)		Total gain (dB)	Configuration word	
	Attenuator	IA_1	IA_2	Vout	PreAmp	PGA	Vout	Gain (dB)	Vout		Binary	Decimal
-108	0	34	34	-40	6	20	-14	12	-2	106	000111	7
-102	0	34	34	-34	6	14	-14	12	-2	100	000110	6
-96	0	34	34	-28	6	8	-14	12	-2	94	000101	5
-90	0	34	34	-22	6	2	-14	12	-2	88	000100	4
-84	0	34	34	-16	6	-4	-14	12	-2	82	000011	3
-78	0	34	34	-10	6	-10	-14	12	-2	76	000010	2
-72	0	34	0	-38	6	20	-12	12	0	72	001111	15
-66	0	34	0	-32	6	14	-12	12	0	66	001110	14
-60	0	34	0	-26	6	8	-12	12	0	60	001101	13
-54	0	34	0	-20	6	2	-12	12	0	54	001100	12
-48	0	34	0	-14	6	-4	-12	12	0	48	001011	11
-42	0	0	0	-42	6	20	-16	12	-4	38	010111	23
-36	0	0	0	-36	6	14	-16	12	-4	32	010110	22
-30	0	0	0	-30	6	8	-16	12	-4	26	010101	21
-24	0	0	0	-24	6	2	-16	12	-4	20	010100	20
-18	0	0	0	-18	6	-4	-16	12	-4	14	010011	19
-12	0	0	0	-12	6	-10	-16	12	-4	8	010010	18
-6	0	0	0	-6	6	-16	-16	12	-4	2	010001	17
0	0	0	0	0	6	-22	-16	12	-4	-4	010000	16
6	-17	0	0	-11	6	-10	-15	12	-3	-9	011010	26
12	-17	0	0	-5	6	-16	-15	12	-3	-15	011001	25
18	-17	0	0	1	6	-22	-15	12	-3	-21	011000	24

Instead of using a single amplifier with $63\ dB$ of gain, it was convenient to implement it in a cascade of two $34dB$ fixed gain amplifiers, selectable by an analog multiplexer.

The fixed gain amplifiers are implemented using Instrumentation Amplifiers (IA) with different gains and an analog multiplexer to select each one when convenient, as depicted in Figure 4-7.

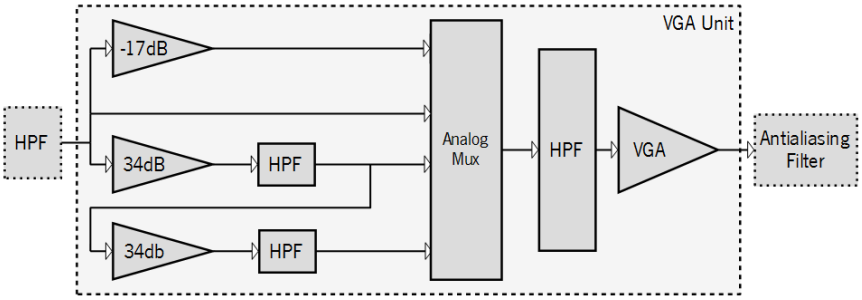

Figure 4-7: *VGA unit diagram.*

Thus when the input signal is smaller than -78 dB[V], the 68 dB (34 dB + 34 dB) amplifier is selected by the analog multiplexer, when the input signal is greater than 78 dB[V] and smaller than -38 dB[V], a 34 dB amplifier is selected by the analog multiplexer. If the input signal is greater than -38 dB[V] and smaller than 4 dB[V], no gain has to be applied before the VGA, because it is in the VGA input range. Thus the input signal is connected directly to the analog multiplexer and, in the case where the input signal is larger than 4 dB[V], a -17 dB attenuator is selected to reduce the signal amplitude to within the VGA's acquisition range. Figure 4-7 shows the inclusion of three HPF inside the VGA unit module. These filters have the function of removing the offset voltage inserted in the signal by the low noise IAs.

4.1.3.1 Low noise amplifier

The IA selected to implement the low noise fixed gain amplifiers is the AD8429 from Analog Devices which is an ultralow noise. This is an instrumentation amplifier projected for measuring very small signals. It has a 1 nV/√Hz input noise (G = 100) (Figure 4-8), 50 µV maximum input offset voltage, 80 dB CMRR, 15 MHz bandwidth (G = 1), 1.2 MHz bandwidth (G = 100) (Figure 4-9).

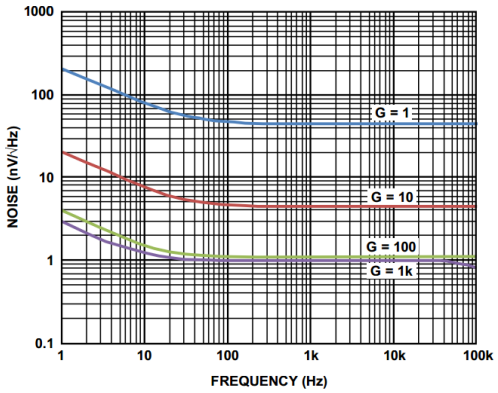

Figure 4-8: *Noise Spectral Density vs. Frequency.*

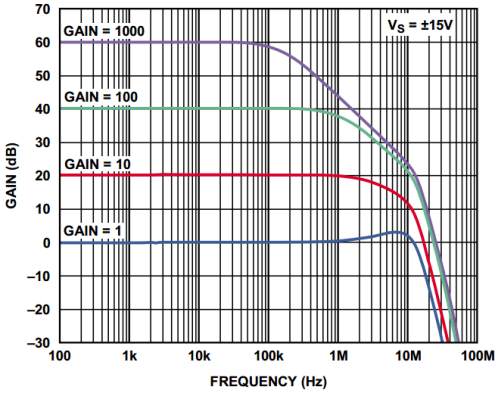

Figure 4-9: *Gain vs. frequency.*

4.1.3.2 Decoupling filters

Even though the AD8429 has a PSRR of 80dB for the positive supply and 60 dB for the negative (green line in Figure 4-10 and Figure 4-11, a decoupling filter has to be used to reduce the noise at the power supply which can adversely affect performance.

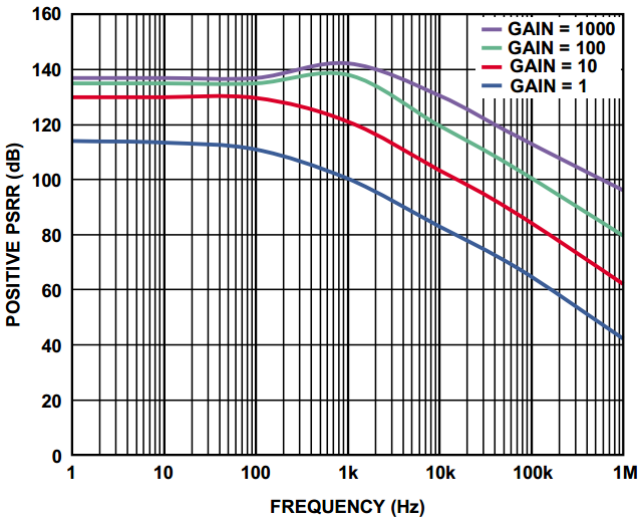

Figure 4-10: *Positive PSRR vs. Frequency.*

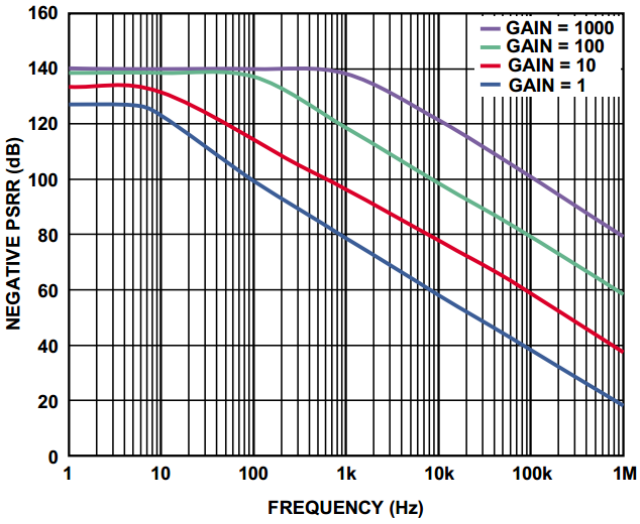

Figure 4-11: *Negative PSRR vs. Frequency.*

Thus a 0.1 µF capacitor was placed as close as possible to each supply pin (Figure 4-12).

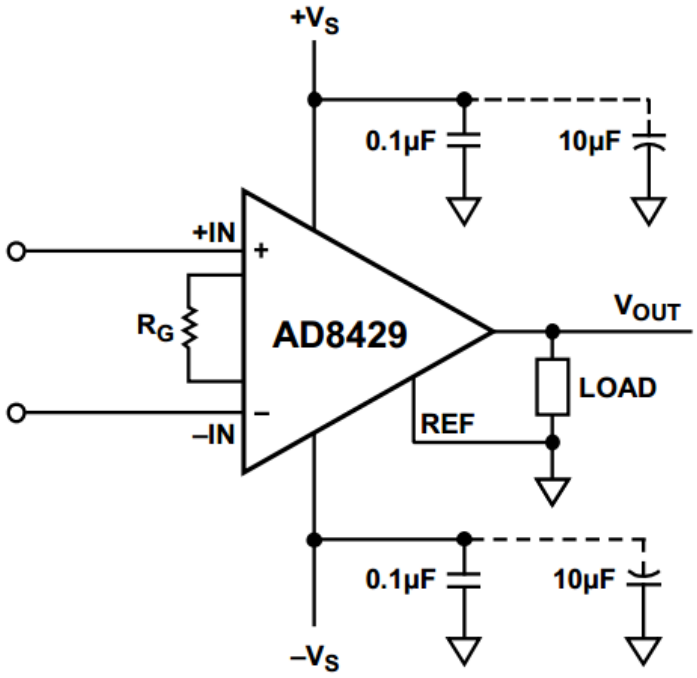

Figure 4-12: *Decoupling capacitors configuration.*

4.1.3.3 Ferrite bead

In the case of the first 34 dB gain instrumentation amplifier, which amplifies signals from -101 dB to -78 dB, a ferrite bead should be placed in series with the power supply line [23], [24] to remove high frequency noise, in the power supply line

Therefore, a B-20F-57 which is a MnZn KEMET B-20 series bead core was used [25]. The B-20F-57 has an impedance of 40 Ω at 1 MHz and above 90 Ω for frequencies 3 MHz and 30 MHz (Figure 4-13), which is suitable to reject the 24 MHz influence from digital signals nearby.

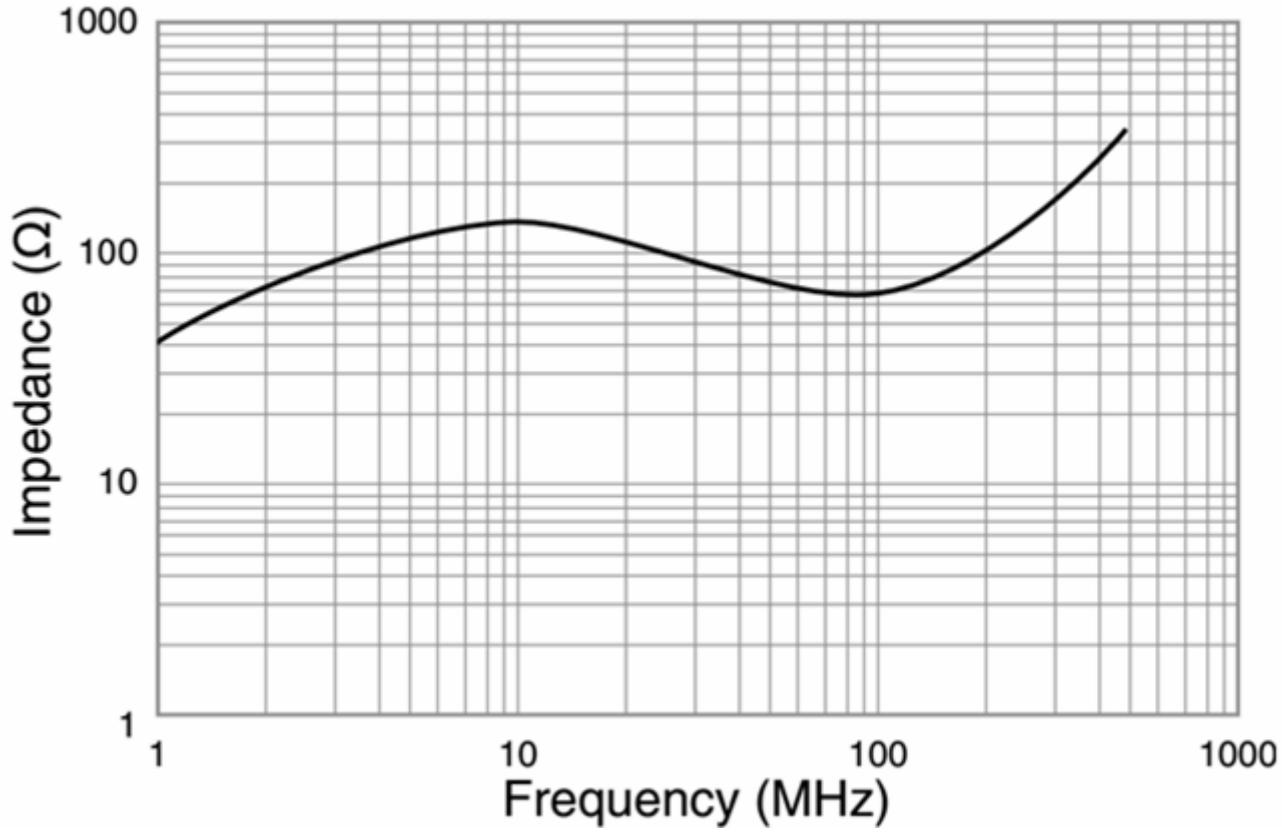

Figure 4-13: *B-20F-57 impedance vs frequency.*

4.1.4 High pass filter

Before the signal enters the fixed gain amplifiers, a HPF (Figure 4-14) is used to remove signals of frequencies below $100\ kHz$. Because there were not restricted requirements on the HPF cutoff frequency fc, it was decided to make $\mathrm{fc} = 75\ kHz$ to guarantee that the some deviation in the real circuitry parameters, R and C doesn't chance the system's frequency response and therefore fc becomes greater than $100\ kHz$.

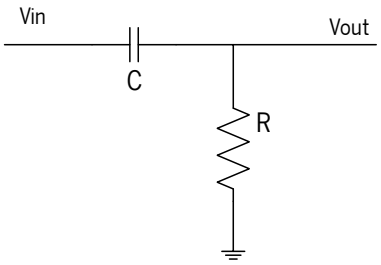

Figure 4-14: *HPF circuit.*

The HPF's transfer function is given by equation 8.

$$\mathrm{H(j\omega)} = \frac{j\omega RC}{j\omega RC + 1}. \tag{8}$$

And its cutoff frequency fc is represented by equation 9, thus making a $R = 140\ \Omega$ and $C = 15\ nF$ the HPF has a $fc = 75788\ Hz$ or $75.788\ kHz$

$$\mathrm{fc(Hz)} = \frac{1}{2\pi RC}. \tag{9}$$

Figure 4-15 represents the plotting of the bode diagram of the HPF's transfer function.

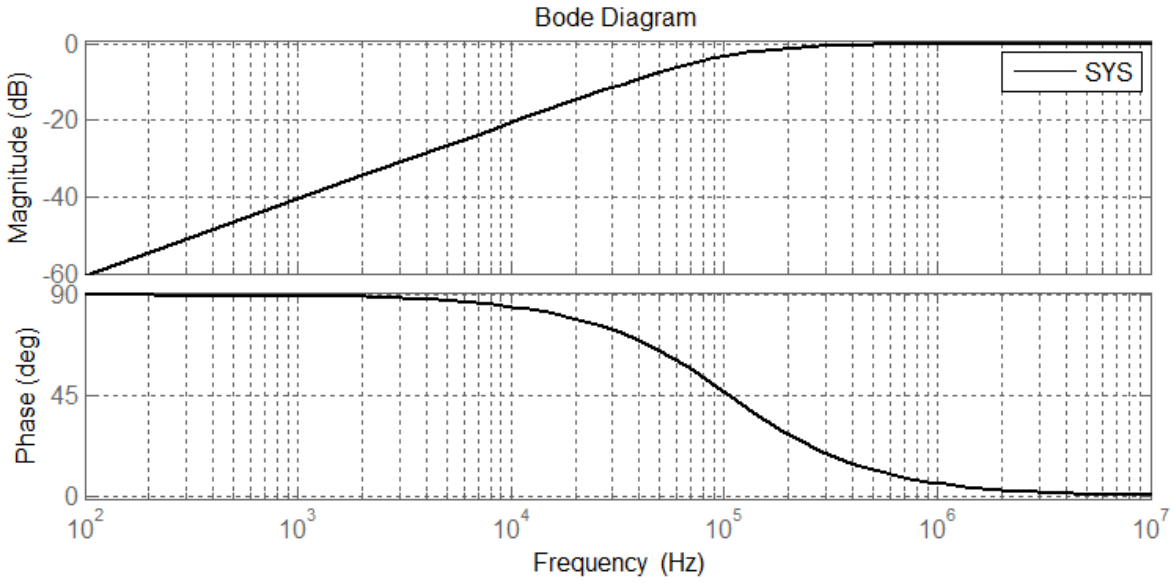

Figure 4-15: *Magnitude and phase of the HPF's transfer function.*

4.1.5 Hydrophone selection

The selected hydrophone, the C304XR, has an output impedance of $10\ \Omega$ and a preamplifier that amplifies the signal, adds an offset value, and provides enough current to drive a $100\ \Omega$ load. These characteristics make it possible to link the hydrophone directly to the HPF.

Other simple piezoelectric hydrophones, without internal preamplifier, work in a passive regime, not having any offset value nor being able to provide current to drive the HPF required.

The solution to use, in both types of hydrophones in the same system, is to make two parallel entry points in the hardware and use a switch to select which one drives the LPF. The standard hydrophone's signal is amplified, in power, by an instrumentation amplifier (IA) with low gain and then, if selected, drives the HPF.

This solution (Figure 4-16), increases the output current of the standard hydrophone and provides the C304XR with a direct link to the HPF to remove its offset value.

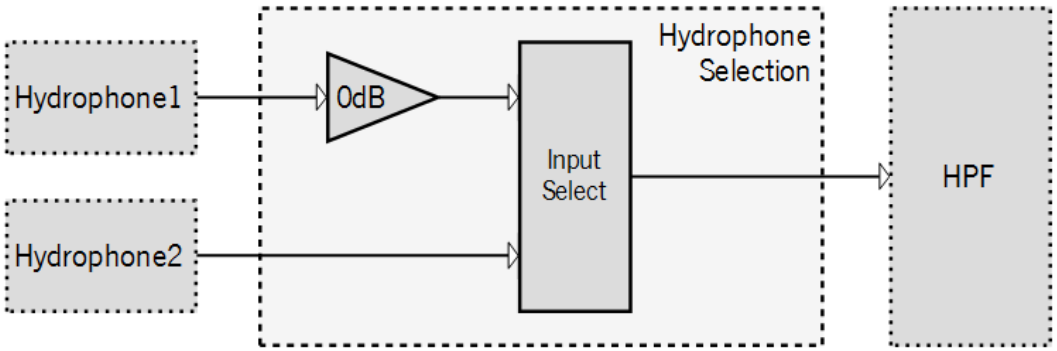

Figure 4-16: *Hydrophone selection system.*

4.1.6 DAC

To generate an analog signal a DAC was used. Because the analog signal has to be sampled at $fs = 24\ MHz$, the selected DAC has to be able to operate at that frequency. A DAC that meets this condition is the DAC904 from Texas Instruments.

The DAC904 is a 14-bit resolution DAC with a maximum of 165 MSPS. It generates a single-ended or differential analog signal in current, with amplitude of $20\ mA$ and operates on a single-supply between +2.7 V and +5.5 V. The close matching of the current outputs ensures good dynamic performance in the differential configuration, which can drive a transformer. In non-continuous operation, the power-down mode can be activated, resulting in a standby power consumption of only 45 mW.

4.1.6.1 Analog output

The DAC's analog output is the difference, in current, between the I_{out} and $I_{\overline{out}}$ depending on the input code sent to the IC through the data bus, as expressed in Table 4-4.

Table 4-4: *Input Coding versus Analog Output Current.*

Input Code (D13-D0)	I_{out}	$I_{\overline{out}}$	ΔI
11 1111 1111 1111	$20mA$	$0mA$	$20mA$
10 0000 0000 0000	$10mA$	$10mA$	$0mA$
00 0000 0000 0000	$0mA$	$20mA$	$-20mA$

Using an RF transformer (Figure 4-17) provides a convenient way of converting the differential output signal, in current, into a single-ended voltage signal with minimal components.

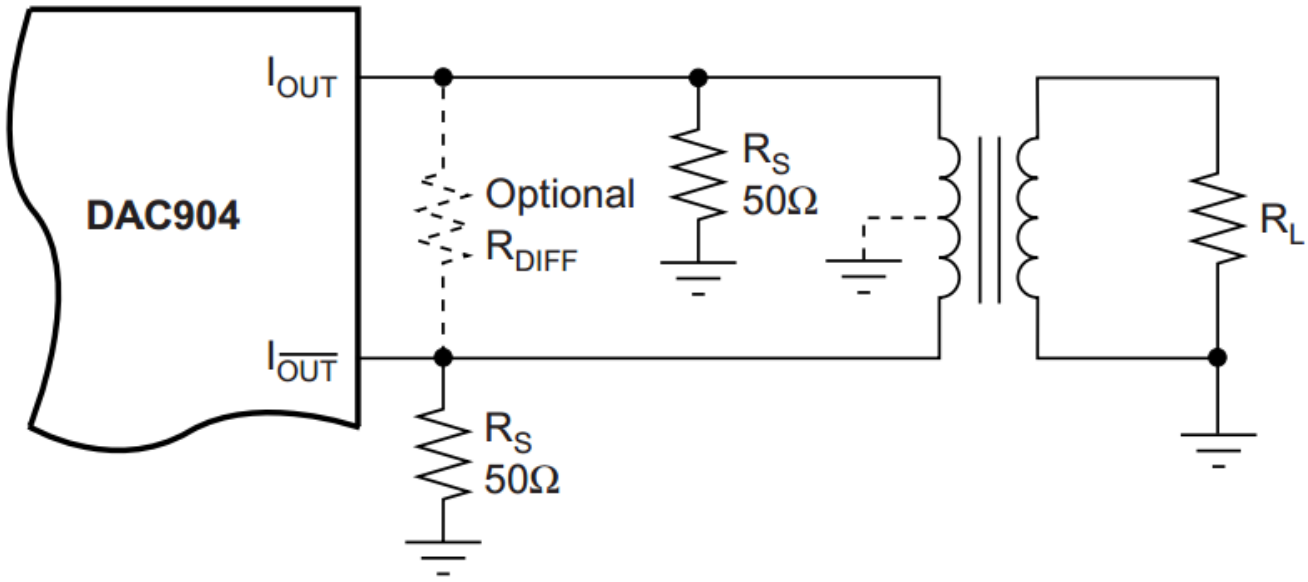

Figure 4-17: *Differential output configuration using an RF transformer.*

4.1.6.2 RF transformer

The RF transformer suitable for transforming the DAC's differential output current into a single supply has to pass signals of frequencies between 100 kHz and 4 MHz. The TTWB transformer family, from Coilcraft, meets the requirements of this system and therefore the TTWB2010L_ was used [11].

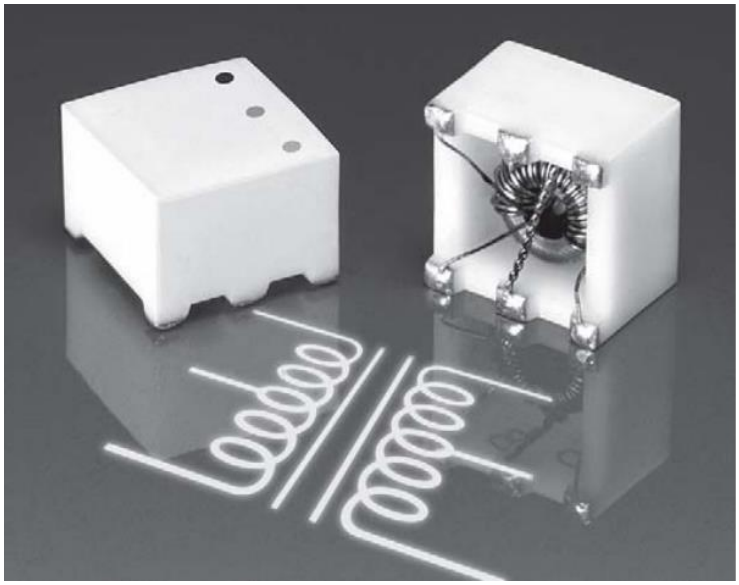

Figure 4-18: *Coilcraft TTW transformer family packaging.*

The TTWB2010L_ is a surface mount wideband transformer which has a 400 V isolation, 250 mA maximum current rating, a 1:1 impedance ratio and is 0 dB bandwidth is from 20 kHz to 30 MHz (Figure 4-19).

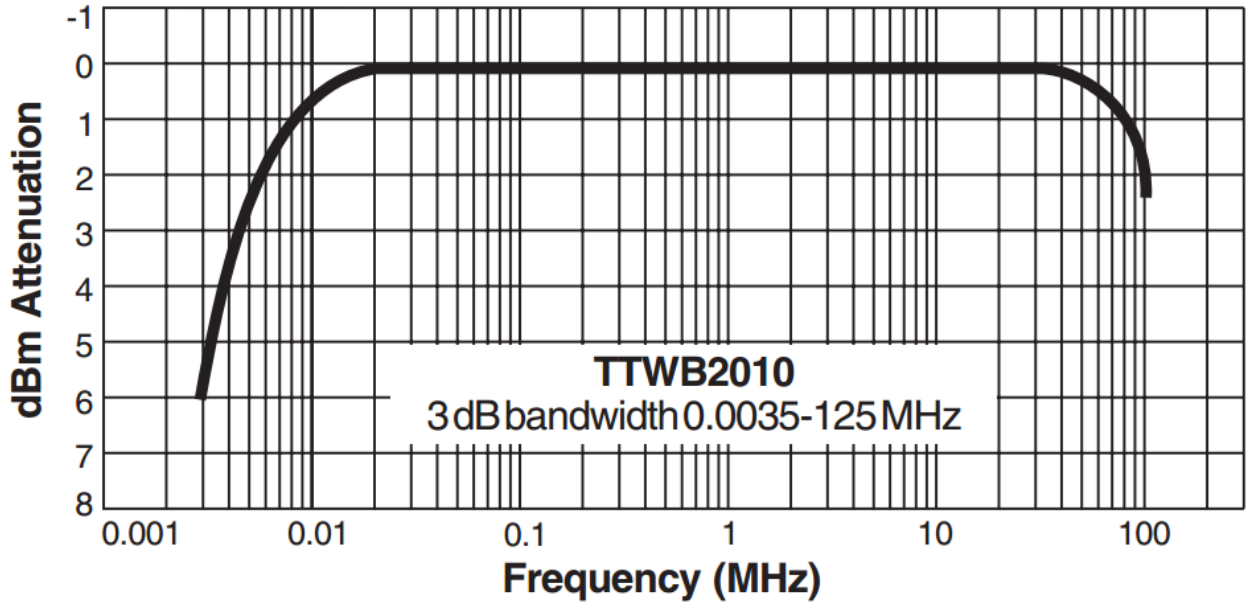

Figure 4-19: *TTWB2040 transformer frequency response.*

4.1.7 Voltage regulators

The voltage supply for the instrumentation circuits has to be lower or equal than ±6.3 V, because ICs like the previously chosen analog multiplexer (AD8184) supports a maximum voltage supply of ±6.3 V, thus, being ±5 V a common output voltage for linear voltage regulators, this value was chosen as the instrumentation voltage supply.

Because all the system has to be powered from a ≥12 V supply, a switched mode voltage converter was used to lower that voltage before the ±5 V linear regulation. Thus, to generate a 5 V voltage, a buck converter was used to convert 12 V to 7 V and then a linear voltage regulator to convert 7 V to 5 V. In a similar way, to generate a -5 V voltage, a Buck-Boost converter was used to convert 12 V into -7 V and then a linear voltage regulator to convert -7 V to -5 V. The inclusion of switched mode converters aimed to reduce the power loss, increase the efficiency and reduce the heat generated.

4.1.7.1 Buck Converter

Tor the Buck converter it was used a 3 A Step-Down voltage regulator, the LM2596 from Texas Instruments, which only needs an inductor, a capacitor, a diode and two feedback resistors to adjust the output voltage.

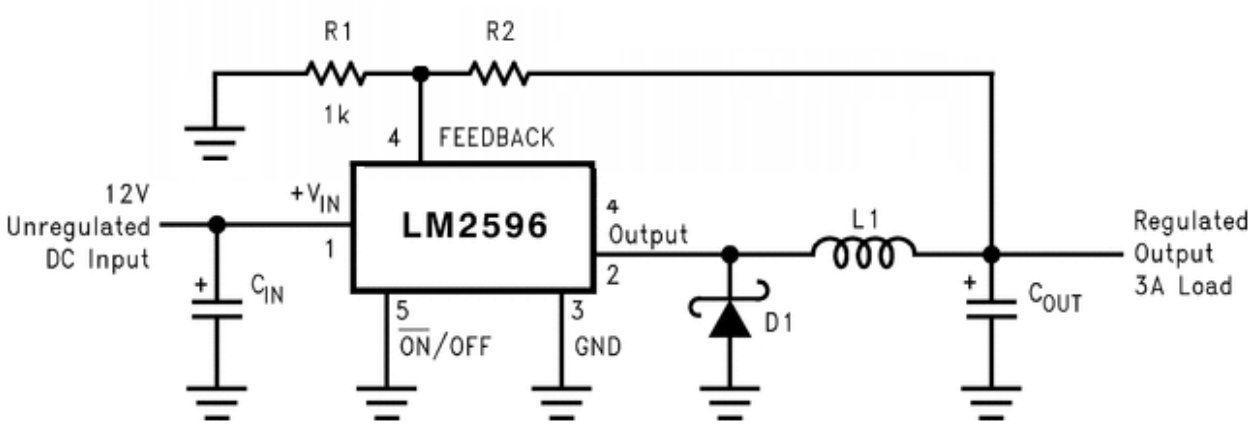

Figure 4-20: *LM2596 configuration circuit.*

The output voltage is configured, setting the value of R1 and R2, using equation 10 with $V_{Ref} = 1.23\ V$.

$$V_{Out} = V_{Ref}\left(1 + \frac{R2}{R1}\right) \tag{10}$$

4.1.7.2 Buck-Boost converter

To convert the 12 V supply voltage for a negative value, it was used an integrated switching regulator (ISR), the PTN78000A from Texas Instruments.

The PTN78000A provides high-efficiency, positive-to-negative voltage and operates in a wide-input voltage range, (7 V to 29 V) generating 1.5 A in a negative voltage between –15 V and –3 V and. Its efficiency is up to 84% and has an output current limit that shuts down in case of over temperature

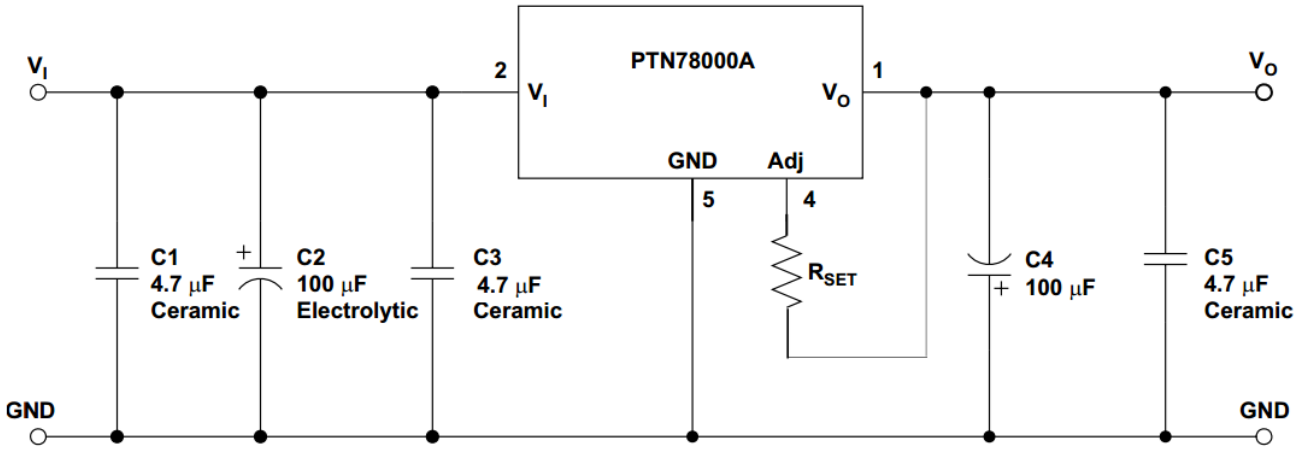

Figure 4-21: *PTN78000A configuration.*

4.1.8 Instrumentation cooling

To improve the heat dissipation in the system, a 12 V fan was used. To regulate the voltage for the fan, in case the power supply voltage is above 12 V, a switched mode converter was used.

For convenience, the Buck converter used was LM2596 from Texas Instruments because it has been used previously and therefore, reduces the development time. For the converter's output to be 12 V instead of 7 V, the only change in the circuit of Figure 4-20 is the value of the resistor $R2$.

4.2 High frequency power amplifier design

Based on the high frequency power electronics considerations (chapter 3) the ultrasonic emitter has to be driven with a 30 V sinusoidal signal.

Since the input voltage can be as low as 12 V, a Boost converter is required to transform the non-fixed input voltage into a fixed output voltage of 30 V. Because the system has to generate a sinusoidal signal of 30 V amplitude, a negative voltage of -30 V has to be created. To do so, instead of generating a -30 V voltage, an H-Bridge was found to be the most appropriate solution, inverting the existing 30 V supply for the negative semi cycle.

To drive the 30 V H-Bridge, a bipolar signal amplifier was used. This signal amplifier was built using operational amplifiers, which amplify signals in the range of ±15 V.

The analog signal, enters the power electronics through a LPF to remove possible high frequency noise and then, through a RF transformer which acts as a HPF, removing signals of frequencies bellow 100 kHz, and a single ended to differential converter.

The differential signals, generated by the RF transformer, are 180° out of phase from each other. These two signals are amplified each by an operational amplifier to drive the H-Bridge.

Figure 4-22 depicts the power electronics' modular representation.

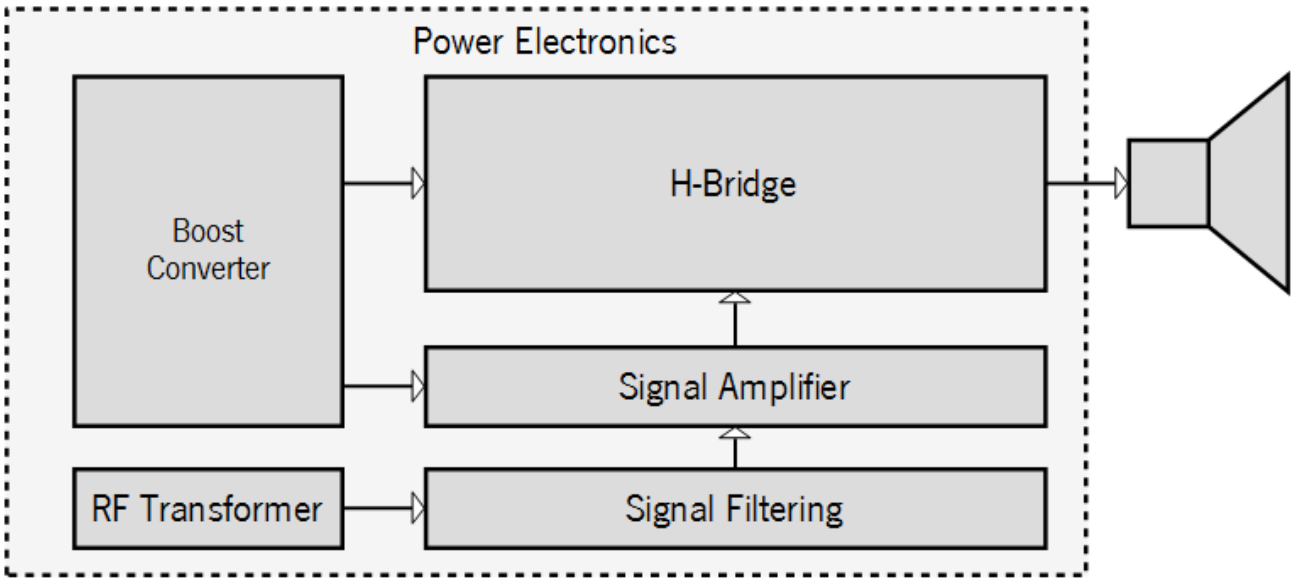

Figure 4-22: *Power electronics module diagram.*

4.2.1 Boost converter

To boost the input voltage for the 44 V required by the signal power amplifier, a generic DC-DC 600 W boost converter was used. This converter operates with an input voltage between 10 V to 60 V and generates an output voltage greater than 12 V and inferior to 80 V. The maximum input current that it sinks is 15 A, and the maximum output current is 10 A. The conversion efficiency is up to 95%. This boost converter is short circuit protected with a fuse.

The output voltage is adjustable with a potentiometer and the maximum output current is also configurable with a potentiometer, as it can be seen in Figure 4-23.

Figure 4-23: *600W 10-60 V to 12-80 V Boost Converter.*

This boost converter has an aluminum heat dissipater attached to it, to which the power semiconductors are in contact. This way, the most heating producing components aren't in contact with the PCB.

4.2.2 Power amplifier

In order to generate a bipolar voltage from a single voltage supply, an H-Bridge was designed using Bipolar Junction Transistors (BJT). The BJTs used are the MJE15030G and MJE15031G which are NPN and PNP, respectively. These transistors are designed for use as high frequency drivers in audio amplifiers. They are 50 W, 8 A power transistors with 30 MHz of current gain–bandwidth product.

Based on table 3-1, high frequency power electronics considerations section (at chapter 3), the emitter can consume currents as high as 7 A at 4 MHz. Therefore, the current gain at this frequency must be $7/0.1 = 70$, where 0.1 is the maximum current of the operational amplifier driving the H-Bridge.

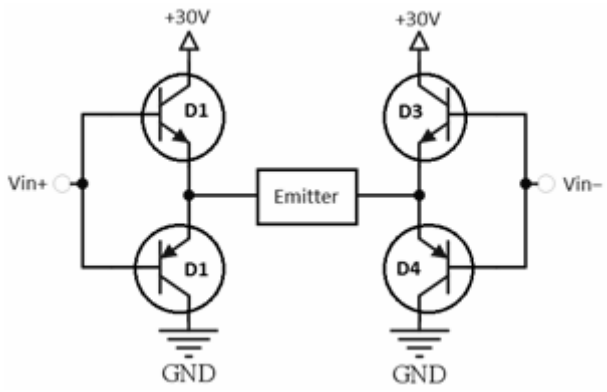

Figure 4-24: *BJTs H-Bridge.*

The MJE15030G and MJE15031G specification sheet doesn't specify the maximum gain that these transistors can apply at 4 MHz, and the collector current of 7 A. Considering that the MJE15030 and MJE15031 can apply a maximum DC gain of 25 and 30, respectively (Figure 4-25) even in DC, two BJTs have to be connected in series to form a Darlington (D) transistor and that way, provide the required gain.

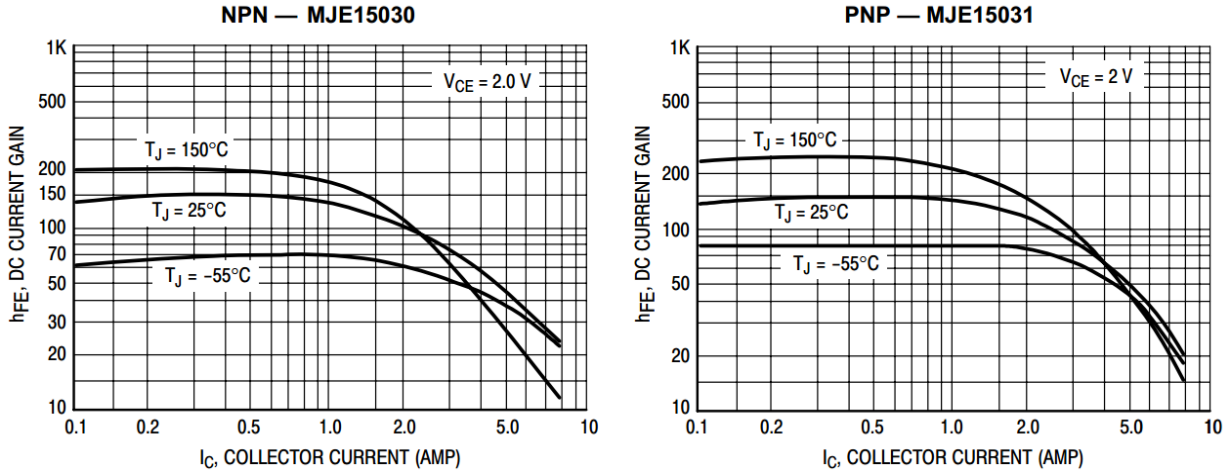

Figure 4-25: *MJE15030G (NPN) and MJE15031G (PNP) DC Current Gain.*

4.2.3 Input signal isolation and filtering

A LPF is required to remove high frequency noise in the analog input signal, which is 1.25 V. Although it could be implemented with passive components, Coilcraft provides a wide variety of LC LPFs, in the form of modules that perfectly meet this project's requirements. Thus the P7LP-605, a 6 MHz, 7th order LC LPF with less than 0.3 dB insertion loss and 50 Ω characteristic impedance was used. This filter allows signals of 6 MHz through and applies an attenuation greater than 60 dB to signals of frequencies above 9 MHz (Figure 4-26).

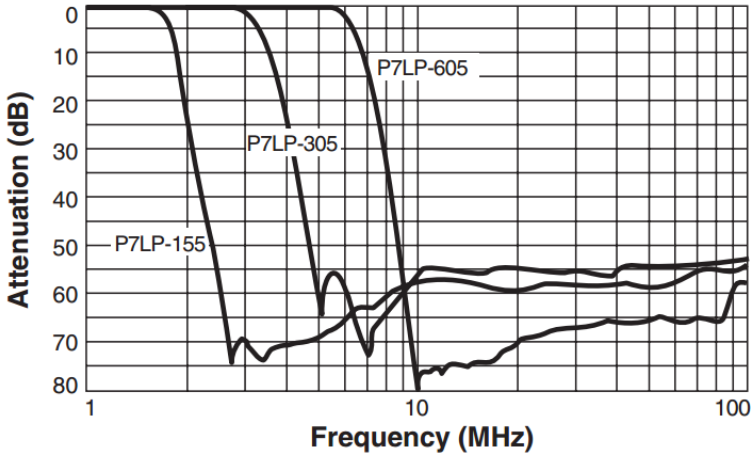

Figure 4-26: *P7LP-605 Attenuation vs. frequency.*

After low pass filtering the input signal, an RF transformer removes frequencies bellow 20 kHz and converts it from single ended to differential. The transformer used is the TTWB2010L_, which is the same used in DAC instrumentation and, consequently, it inserts a gain of 1 in the signal.

The differential signals generated by the RF transformer are 180° out of phase from each other (Figure 4-27). These signals are amplified by the operational amplifiers in the next stage.

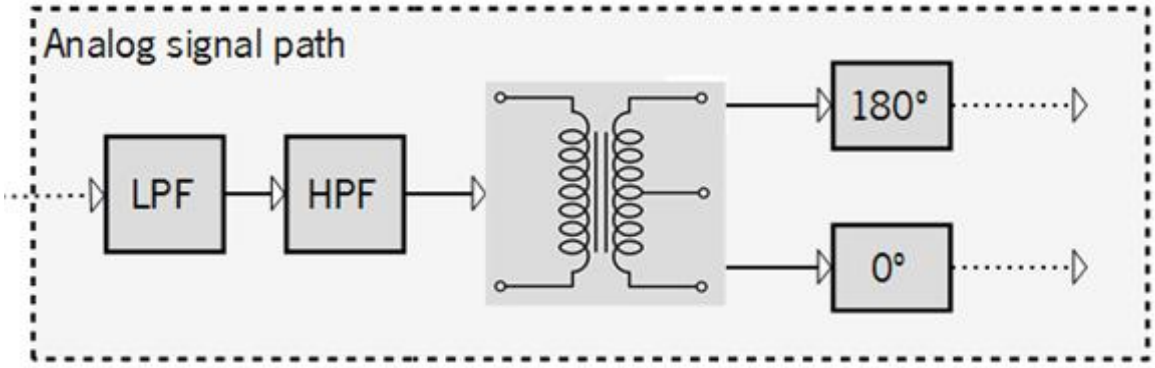

Figure 4-27: *Analog input signal path.*

4.2.4 Operational amplifiers

Being the analog input signal $0.8\ V$, the TTWB2010L_ secondary output voltage is also $0.8\ V$. Because the single ended to differential conversion, the voltage of each phase is $\frac{0.8}{2} = 0.4\ V$. These $0.4\ V$ signals have to be amplified in order to drive the H-Bridge. To do that, the LM7171 operational amplifier from Texas Instruments was used.

This operational amplifier has a voltage supply range of ±18 V, very high slew rate at 4100 V/µs, a wide unity-gain bandwidth of 200 MHz (Figure 4-28) and sources or sinks 100 mA of output current.

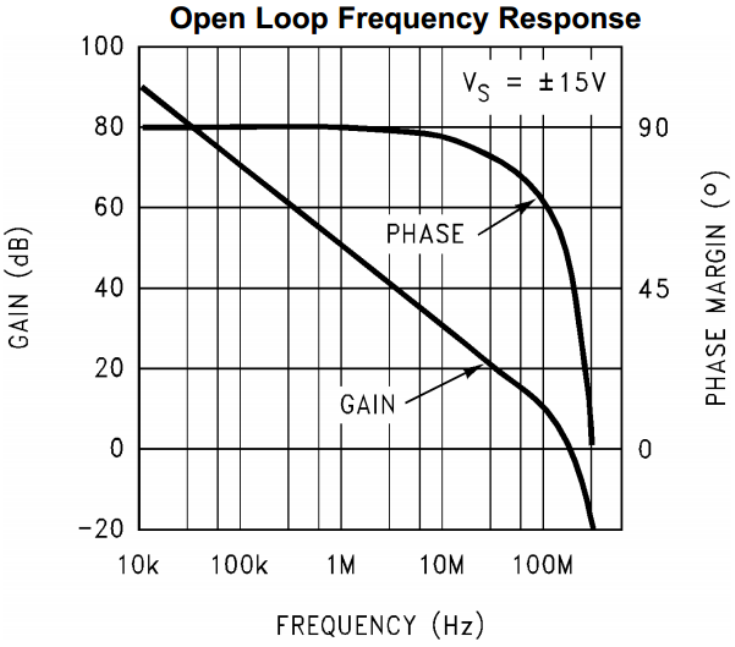

Figure 4-28: *LM7171 open loop frequency response.*

Supplying the LM7171 with $\pm 18\ V$, it can produce an output voltage of $\pm 15\ V$. Thus, to amplify the $\pm 0.4\ V$ to $\pm 15\ V$, a gain of $\frac{15\ V}{0.4} = 37.5$ has to be applied by the LM7171 (Figure 4-29).

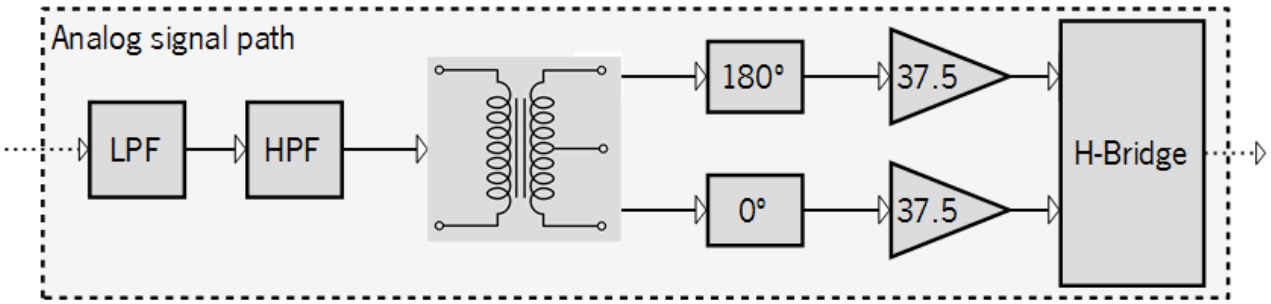

Figure 4-29: *Analog input signal path with the LM7171 gain.*

4.2.4.1 Virtual ground and voltage regulators

Because the power electronics receives a single DC voltage supply, and the operational amplifiers require a bipolar voltage to amplify the analog input signal, a virtual ground signal was created - GND. This GND signal is generated by a power operational amplifier, the LM675 from Texas Instruments and is capable of sourcing or sinking 3 A. It is implemented in a voltage follower configuration and, if $R1 = R2$, its output assumes the value of $(V_+ - V_-)/2$ (Figure 4-30).

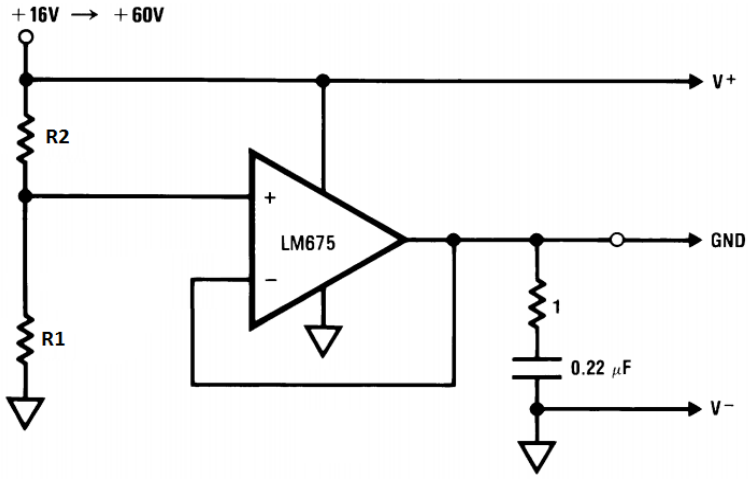

Figure 4-30: *LM675 in a voltage follower configuration.*

To generate a regulated $18V$ for the operational amplifier supply, the MC7818CTG was used. This IC provides an output current of 1 A, it doesn't require external components besides capacitors, has internal thermal overload protection and internal short circuit current limiting. Its input voltage must remain typically 2 V above the output voltage even during the low point on the input ripple voltage (Figure 4-31).

To generate $-18\,V$ for the operational amplifier negative voltage supply, the MC7918CTG was used (Figure 4-32). This IC also provides an output current of 1 A, it has internal thermal overload protection and internal short circuit current limiting. Its input voltage must remain typically 2 V below the output voltage.

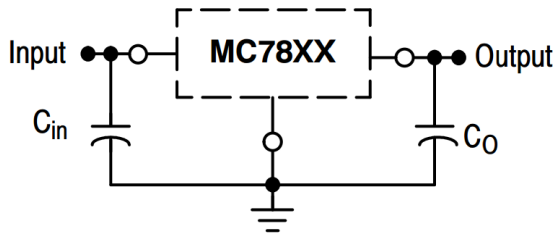

Figure 4-31: MC7818CTG configuration circuit.

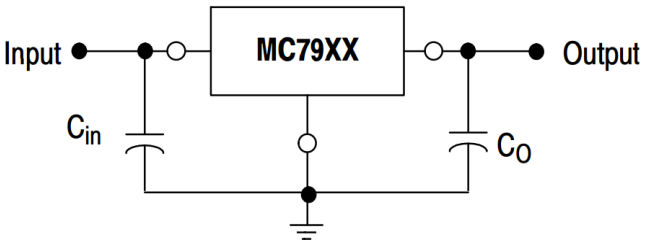

Figure 4-32: *MC7918CTG configuration circuit*

4.3 FPGA module

Instead of designing a system with a FPGA and a microcontroller from scratch, it was decided to use a commercial solution available in the market to reduce the complexity of the project.

The USB-FPGA Module 1.15d, (Figure 4-33), from ZTEX GmbH was found to be a suitable match for the requirements of this project, thus it was used. This module has a Spartan 6 FPGA and high-speed (480 MBit/s) USB2.0 interface via Mini-USB connector (B-type). The USB2.0 communication is handled by an EZ-USB FX2 Microcontroller from Cypress.

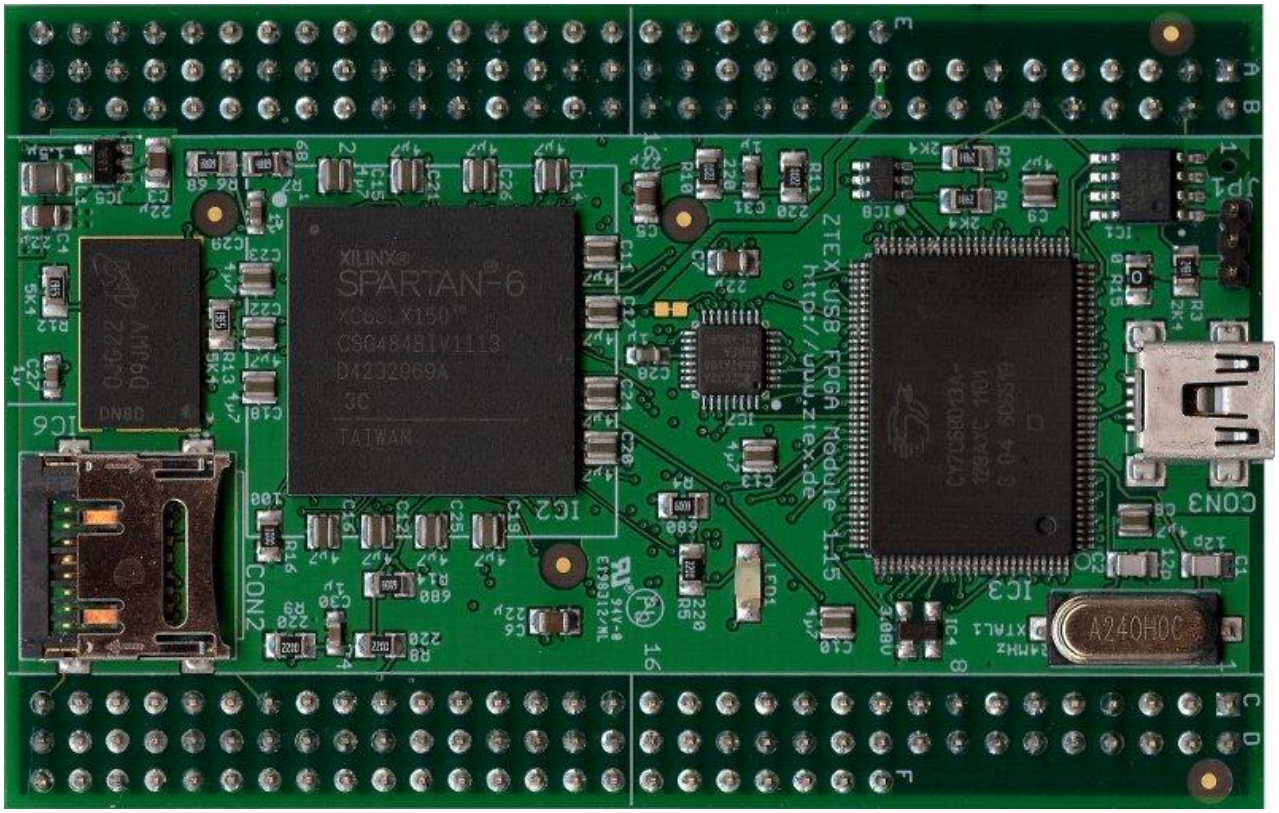

Figure 4-33: *USB-FPGA Module 1.15d with Spartan 6.*

This module has also a 128 MByte DDR2 SDRAM, 99 General Purpose I/O's (GPIO), 15 special I/O's (SIO), a MicroSD socket for extensible Flash memory, a CPLD for fast FPGA configuration, memory mapped IO between EZ-USB FX2 and FPGA, 128 Kbit EEPROM memory, which can be used to store the EZ-USB firmware and a 2 Kbit MAC-EEPROM containing a unique non erasable MAC-address.

A closer look into the ZTEX USB-FPGA Module 1.15d clock diagram at (Figure 4-34) can reveal that the USB data enters the USB-FPGA Module 1.15d module through the Cypress EZ-USB FX2 Microcontroller and

then is passed to the Spartan 6 through the FX2 FIFO interface in an 8-bit or 16-bit bit word format at frequencies up to 48 MHz.

It can also be seen that the Cypress EZ-USB FX2 Microcontroller has 8 GPIO's and 11 SIO's directly connected to the external I/O interface. This feature enables the microprocessor to directly interface electronics if required.

The Spartan 6 has 91 GPIO's and a JTAG connection directly to the external I/O interface, providing enough pins to interface all the electronics. The 128 MByte DDR2 SDRAM won't be used for this project, but future applications can explore its advantages.

To configure the FPGA there are several options, it could be done storing the x.bit file at the CPLD and it gets loaded by the FPGA at the power-up, the x.bit file could also be stored at the MicroSD card and it would proceed the same way or it be loaded through the microcontroller at the startup. This last solution was the used procedure to program the FPGA because it offers the most flexible approach, due to the fact that it only takes about 200ms and can be applied at the runtime whenever the user decides.

This flexibility of programing the FPGA makes it possible for the user to change the logic system on the fly, changing the system's behavior.

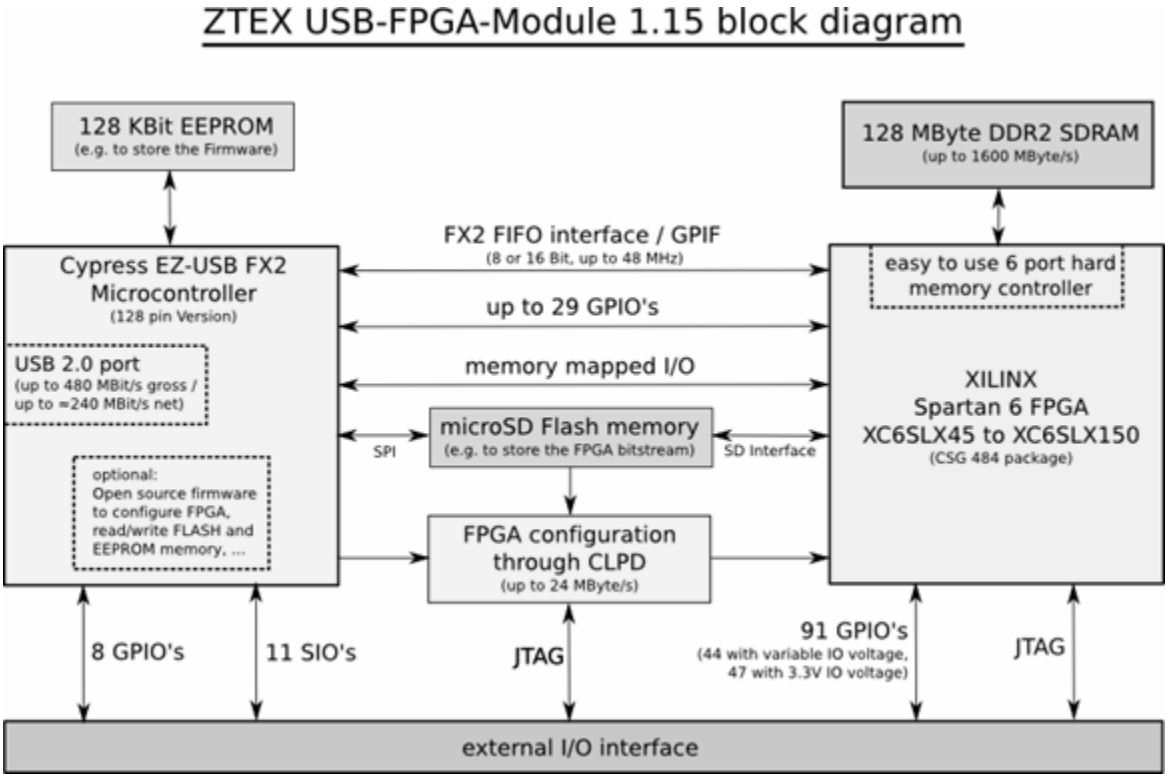

Figure 4-34: USB-FPGA Module 1.15d clock diagram [26].

The USB-FPGA Module 1.15d consumes a maximum of 23 $Watt$ at its peak performance and requires an external power supply, also from ZTEX GmbH, the Power Supply Module 1.2 (Figure 4-35).

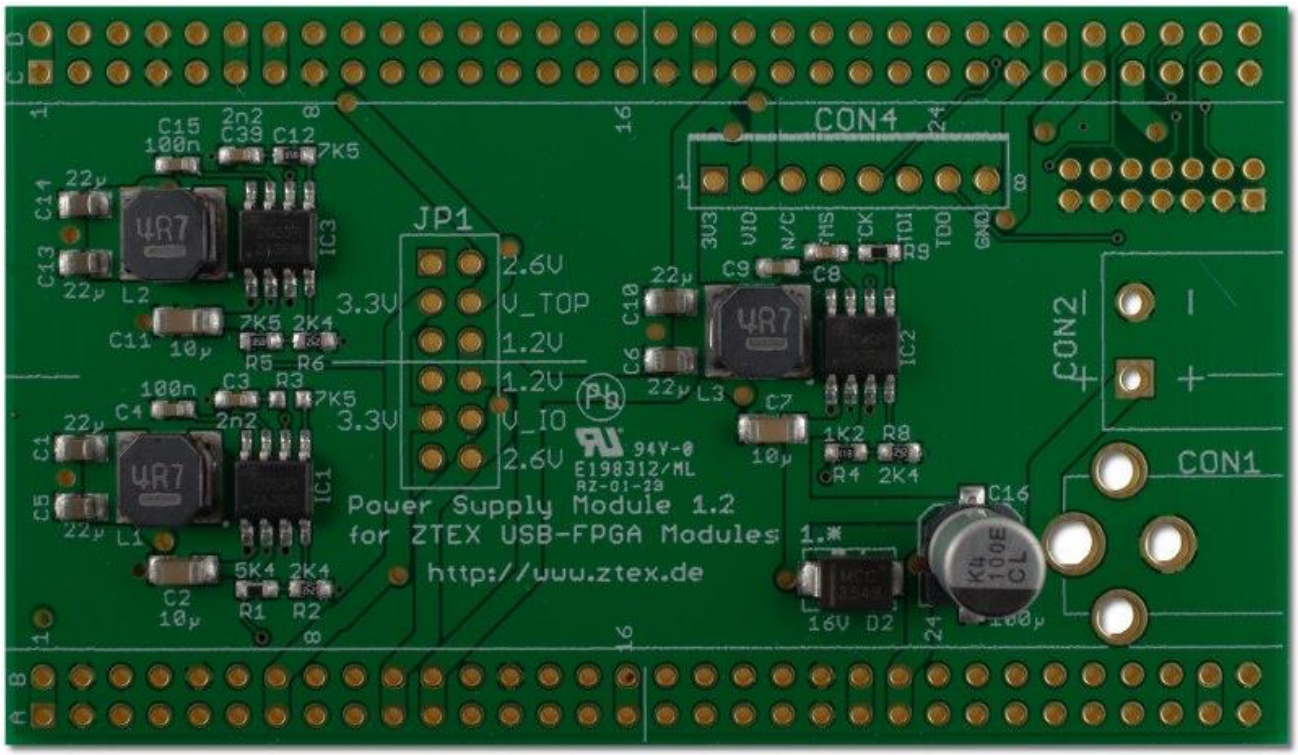

Figure 4-35: *Power Supply Module 1.2 from ZTEX GmbH.*

This power supply module receives an input voltage between 4.5 V and 16 V, and generates a 1.2 V, a 2.6 V and a 3.3 V voltage supply with a 2 A each. It has three switched mode DC/DC converters that transform the input voltage into those different outputs (Figure 4-36).

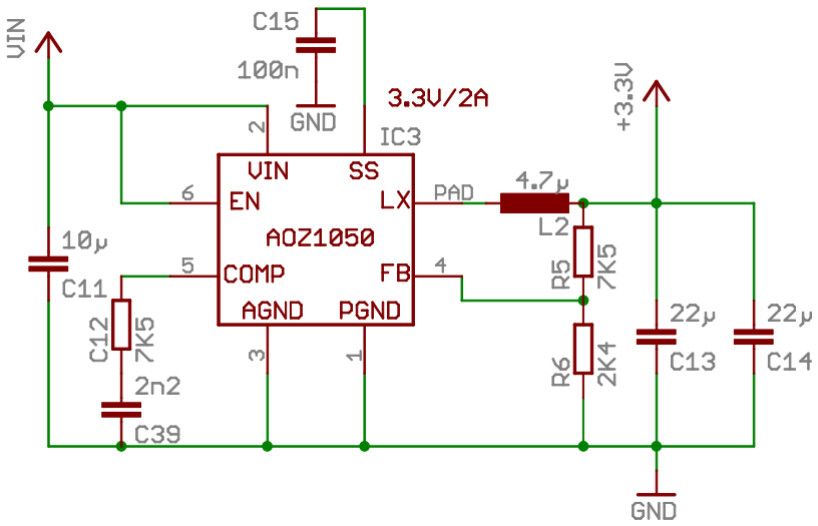

Figure 4-36: *USB-FPGA Module 1.15d 3.3 V DC/DC converter.*

4.4 Logic system design

The logic system is implemented in the FPGA and is divided into two layers. The interface layer and the data processing layer.

The interface layer includes the logics to interface the modulator and the demodulator with the external world, which is the microcontroller's interface logic, the variable gain unit, the DAC and the ADC, and its functionality is to route data in and out of the modulator and demodulator. The details of the modulator and demodulator units are out of the scope of this dissertation, therefore, were not implemented. Instead, the modules were left empty for future development.

To develop the logic system it was used the Xilinx System Generator which is included in Matlab. Thus a Simulink model was created containing the entire interface layer and the modules for further development of the modulator and demodulator, which are part of the data processing layer.

In order to synthetize the target x.bit file to deploy in the FPGA, the proper configurations have to be made in the Xilinx System Generator block, which must be included in the Matlab project.

There are compilation configurations, (Figure 4-37) and clocking configurations, (Figure 4-38). In the compilation configurations the target FPGA must be specified and in the clocking configurations the FPGA clock period has to be specified.

Figure 4-37: *System generator compilation settings.*

Figure 4-38: *System generator clocking settings*

Because the FPGA uses a 48 MHz external clock, connected to pin L22, the period is 20.833333 ns.

4.4.1 Demodulator

The demodulator is the module that interfaces the ADC and the microcontroller (Figure 4-39). This module sets the ADC's DFS and CLK signals and reads the ADC bus and the OTR pin. After reading de ADC values, it should apply a demodulation algorithm do generate a byte. This byte is then written to the Demodulator DATA output, which is connected to the microcontroller. After write the byte to the Demodulator DATA, the demodulator signals the event with Demodulator Request line, which can be used as an interruption in the microcontroller, which attends it, reads the byte and signals the end of reading with the Demodulator ACK signal.

The demodulator also sets the gain, in dB, of the instrumentation, through the VGA gain field.

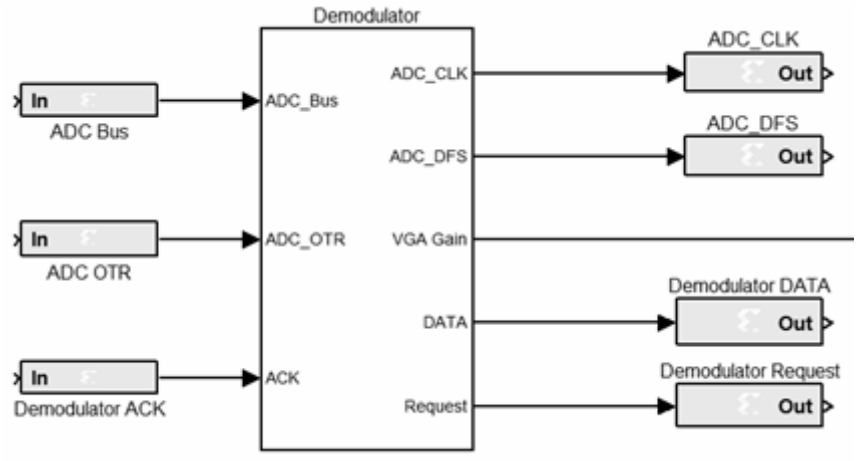

Figure 4-39: *Demodulator module interface.*

4.4.2 Variable gain controller

The VGA controller (Figure 4-40) consists in a module that receives the requested gain from the demodulator and sets the analog multiplexer and VGA pins with the convenient values.

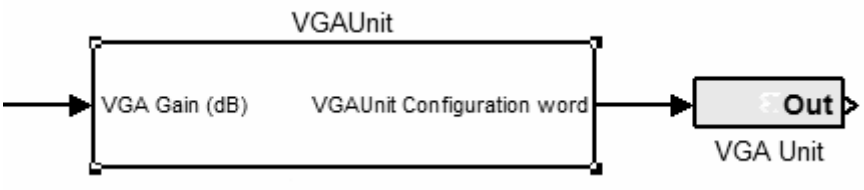

Figure 4-40: *VGA control unit module interface.*

This module has the intent to hide the VGA's unit hardware details from the demodulator. This way, the demodulator only requests the gain and the unit sets the configuration word.

4.4.3 Modulator

The modulator reads a Byte from the microcontroller and generates a sequence of 14-bit words to drive the DAC. To do this, it requests an 8-bit to the microcontroller, setting the Request output to logic HIGH and waits for the ACK signal to be driven HIGH, which is generated by the microcontroller to indicate that a valid word has been placed in the bus. After that, the modulation process reads the 8-bit word from the bus and starts driving the DAC with the corresponding values, which are modulation dependent.

Figure 4-41 represents the modulator module and its logic connections to the external environment.

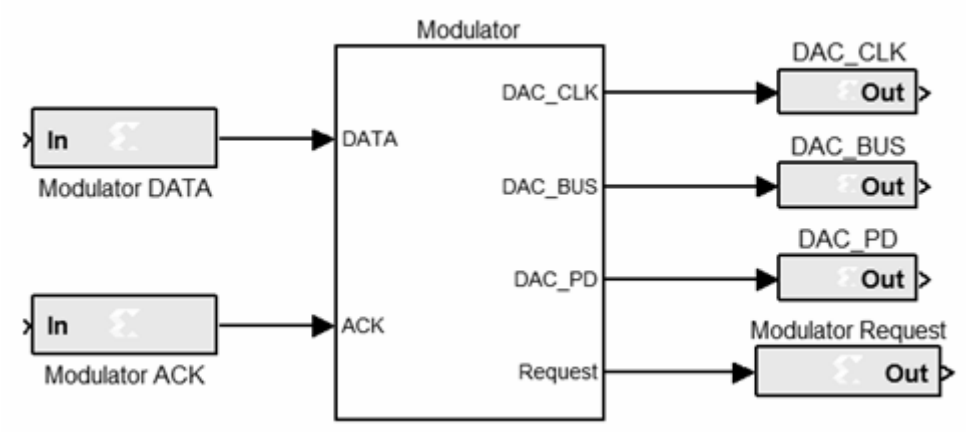

Figure 4-41: *Modulator module interface.*

4.4.4 Interface layer

Figure 4-42 represents the logic layer and its interface with the microcontroller and instrumentation.

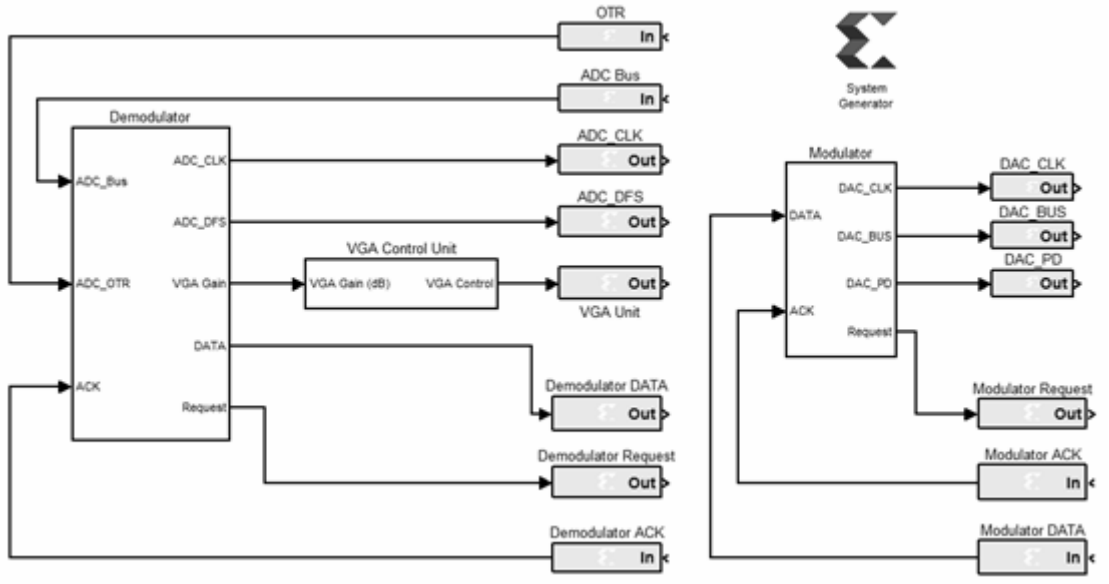

Figure 4-42: *Logic system interface.*

4.5 Software design

The host application task is to interface the user with the hardware. To perform this task, it opens a file, reads its content in 512-Byte packets and writes it to the USB port. To receive data it is performed the inverse task. The applications reads the 512-Byte USB packets and writes them to a file.

In the host application flowchart (Figure 4-43) it can be seen that the application sends and receives USB data packet until the exit condition is true.

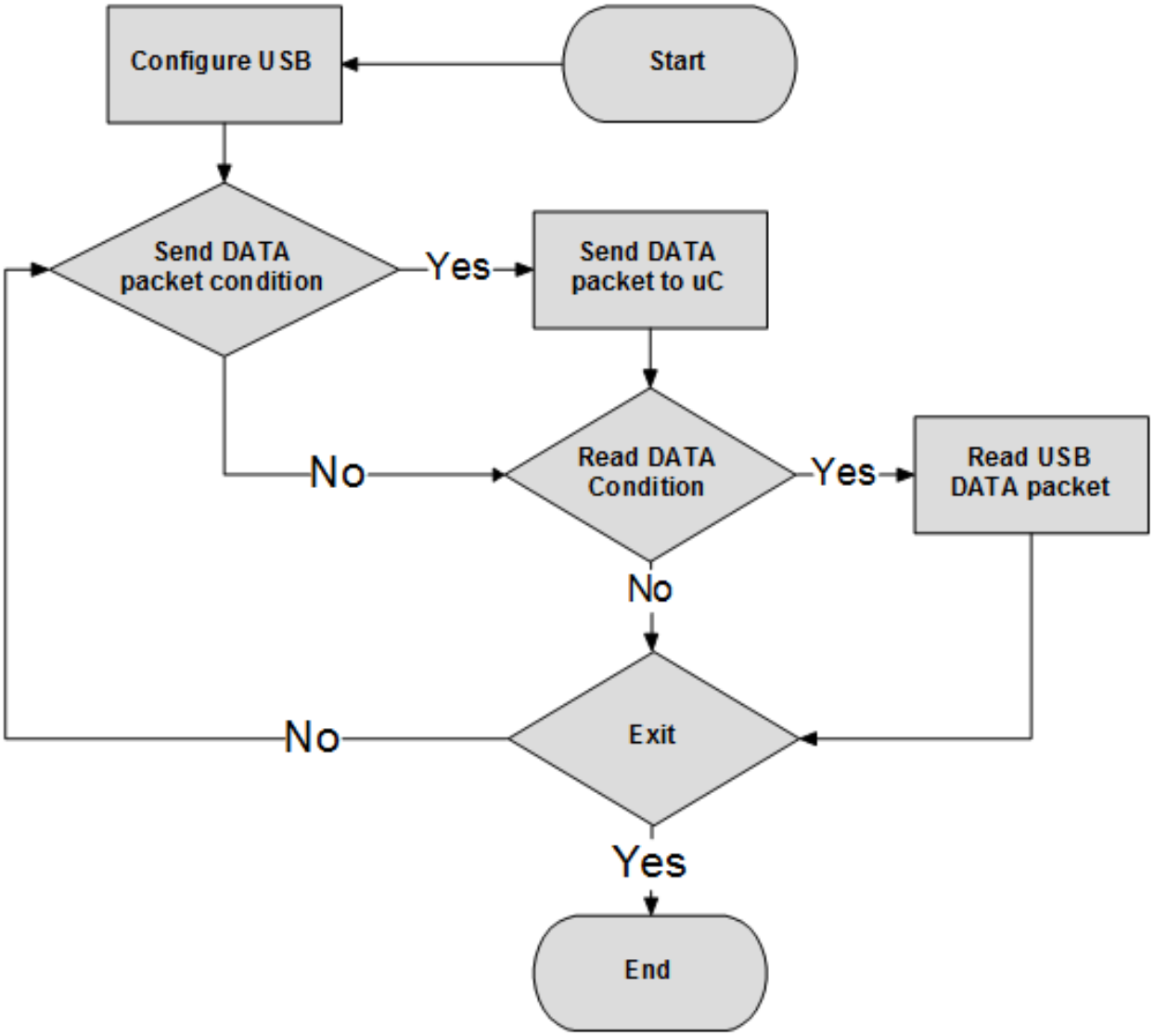

Figure 4-43: *Host application flowchart.*

4.6 Firmware design

The microcontroller task is to interface the application with the FPGA. To perform this task, it requests data from the application in packets and writes it in 8-bit words to the modulator. It also retrieves 8-bit words from the demodulator, inserts it in a FIFO memory and sends it to the application in packets.

In the microcontroller's execution flowchart (Figure 4-44) it can be seen that the microcontroller runs in an infinite loop verifying if there is data to be written to the modulator or retrieved from the demodulator.

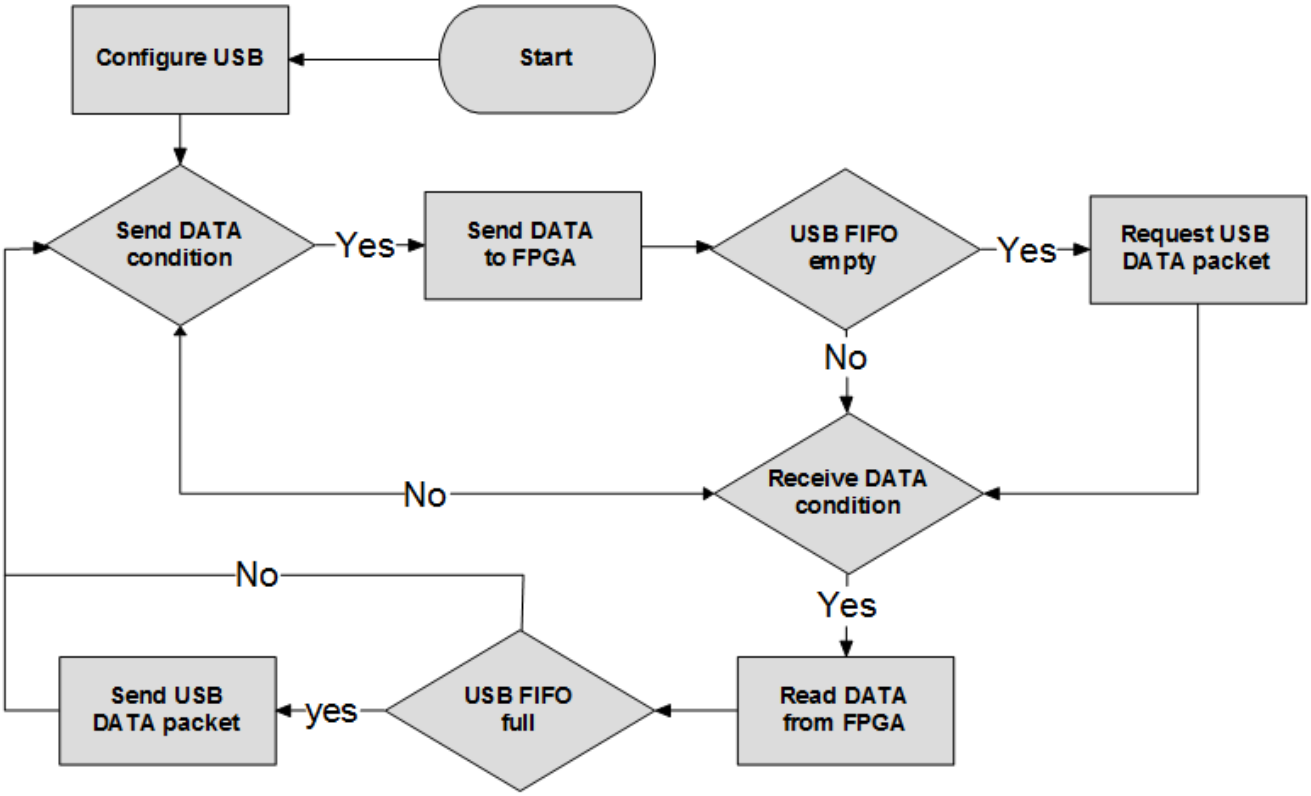

Figure 4-44: *Microcontroller firmware flowchart.*

Chapter 5

5 System implementation

The system was developed in several stages. Firstly, adaptor boards were made to convert the SOIC packaging of the ADC and the DAC to DIP for testing purposes. Then, these IC's were tested and a small prototype board was designed to test its external circuitry. After that a second prototype was designed to integrate the DAC, ADC and instrumentation circuited.

Once the instrumentation and power electronics was tested, a final system was developed, with a good quality PCB.

5.1 Single modules prototyping

Since the ADC (AD9244) and the DAC (DAC904) were SMD, an adaptor board was designed to convert it to DIP. This way it could be tested easily in a breadboard.

Figure 5-1 is the ADC's adaptor board and Figure 5-2 is the DAC's adaptor board.

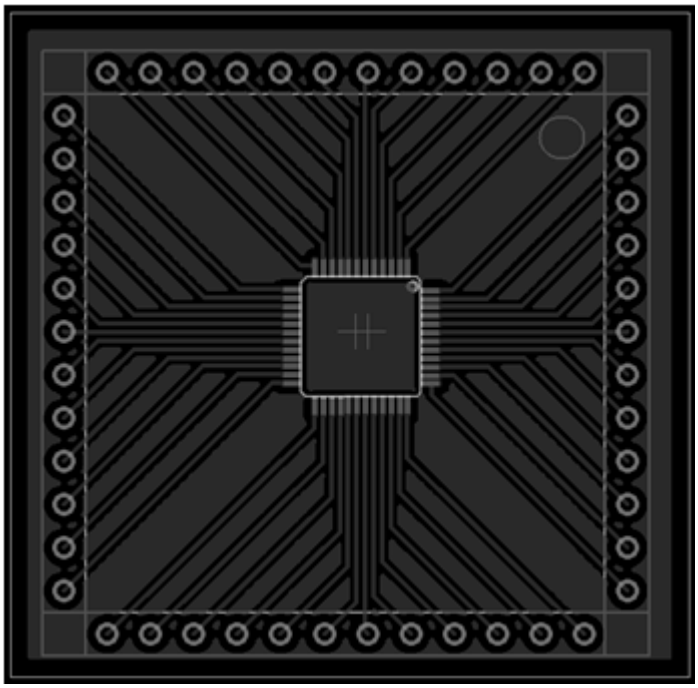

Figure 5-1: *ADC adapter board.*

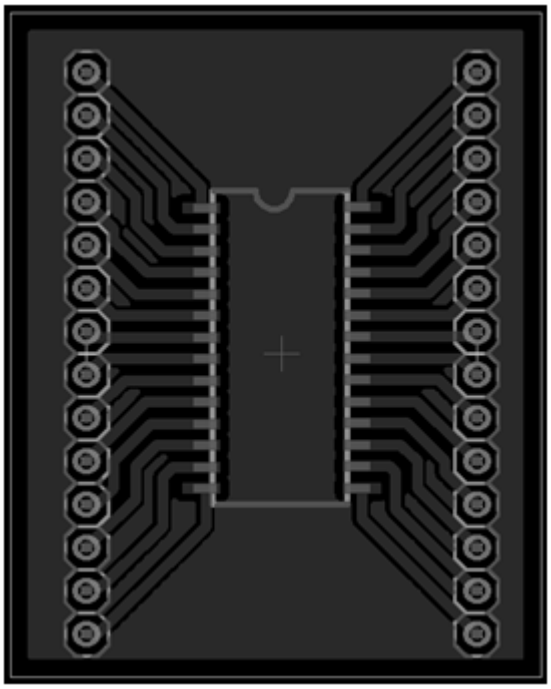

Figure 5-2: *DAC adapter board*

5.1.1 DAC prototype

After soldering the DAC in an adaptor Board, a second board was designed to implement the electronics needed for the DAC to work properly. This board's schematic (Figure 5-3), where it can be seen that the differential current from the DAC is converted into voltage by an operational amplifier configured in differential mode.

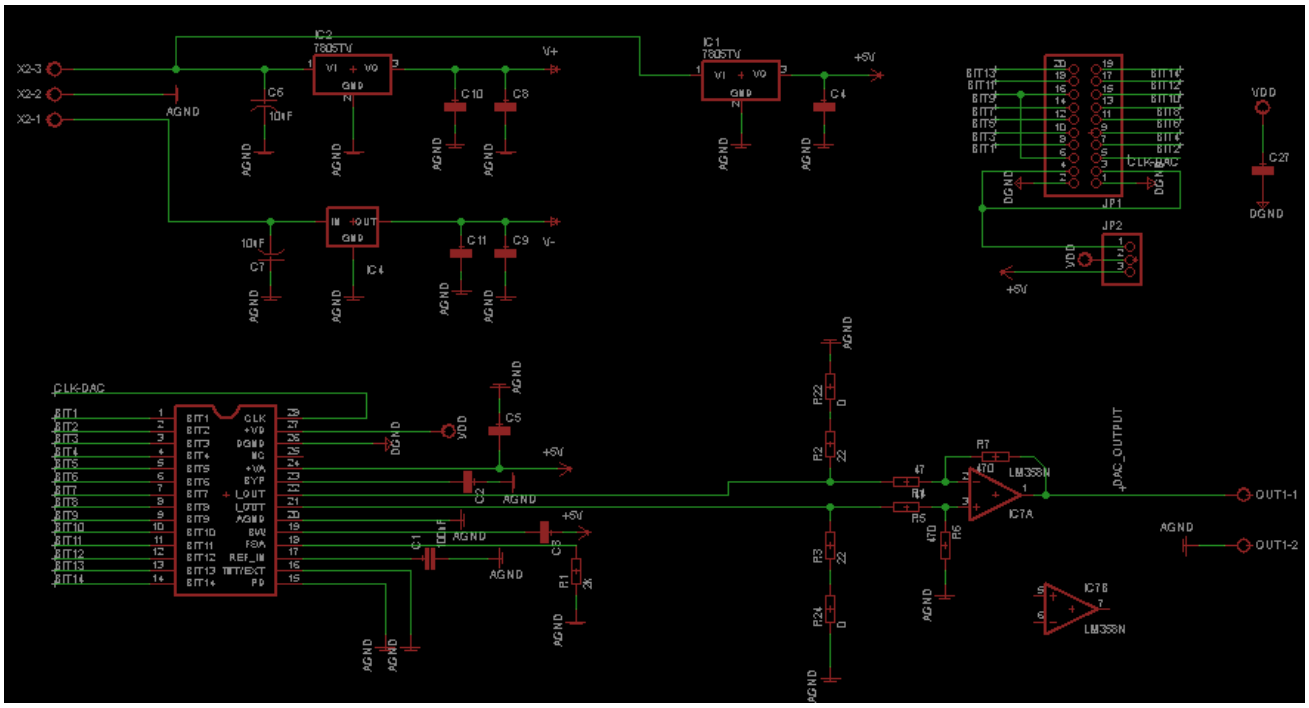

Figure 5-3: *DAC prototype circuit.*

The DAC's circuit was implemented in PCB as it can be seen in Figure 5-4 and Figure 5-5.

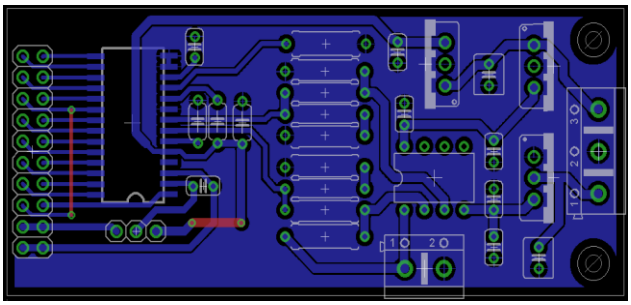

Figure 5-4: *DAC prototype PCB preview.*

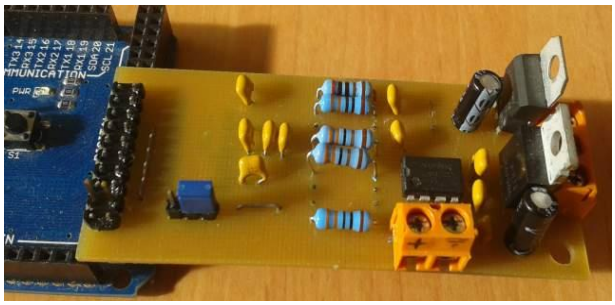

Figure 5-5: *DAC prototype PCB.*

As it can also be seen at Figure 5-5, an Arduino board was used to drive the DAC's digital pins to test its functionality.

5.1.2 ADC prototype

After soldering the ADC in the proper adaptor Board, a second board was also designed to implement the electronics needed for the ADC to work properly. This board's schematic can be seen in Figure 5-6.

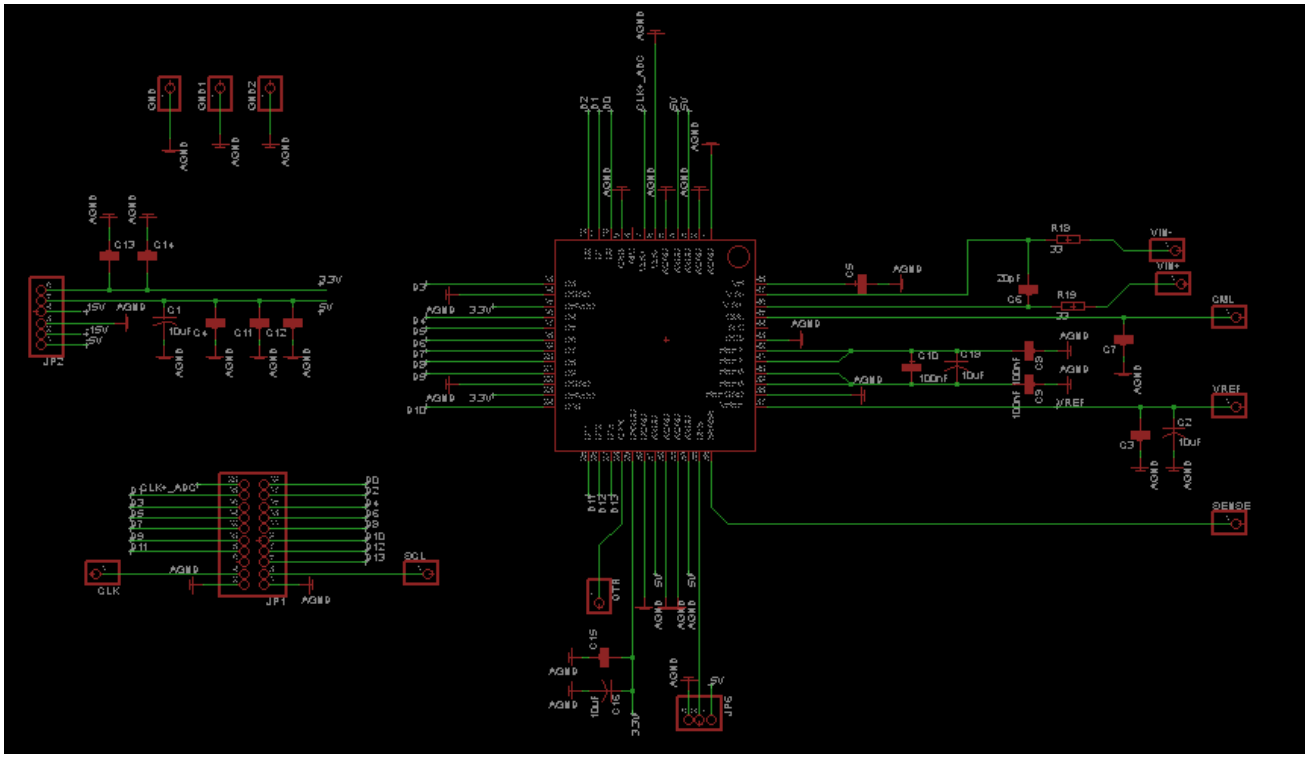

Figure 5-6: *ADC prototype schematic.*

The ADCs circuit was implemented in PCB as it can be seen in Figure 5-7 and Figure 5-8.

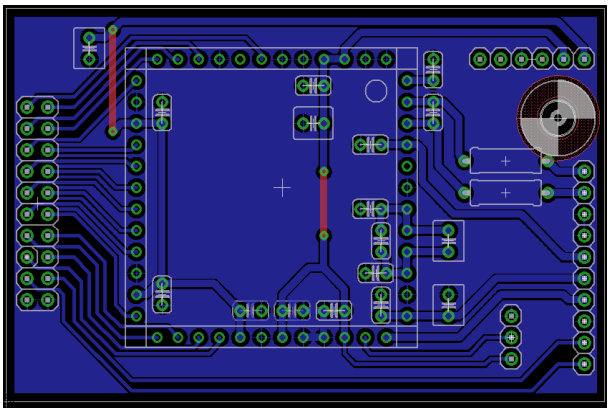

Figure 5-7: *ADC prototype PCB preview.*

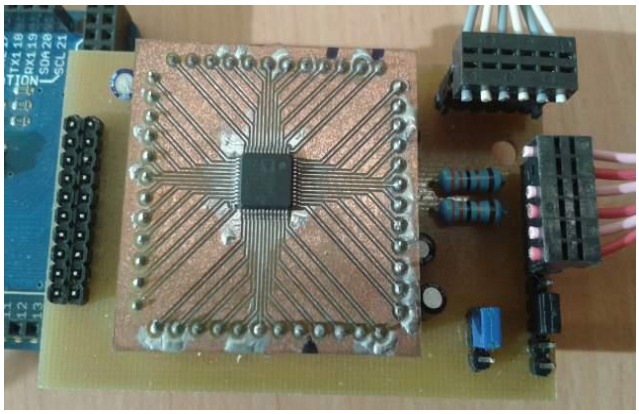

Figure 5-8: *ADC prototype PCB.*

As it can also be seen at Figure 5-8, the Arduino was used to read the ADC's digital pins and to test its functionality.

5.1.3 Voltage regulator prototype

The ADC, the ADC and its instrumentation required different voltages, therefore a generic voltage supply was designed to supply several voltages. This voltage supply (Figure 5-9) received a voltage of $\pm 18\ V$ and generated $\pm 15\ V$, $\pm 5\ V$ and $3.3\ V$.

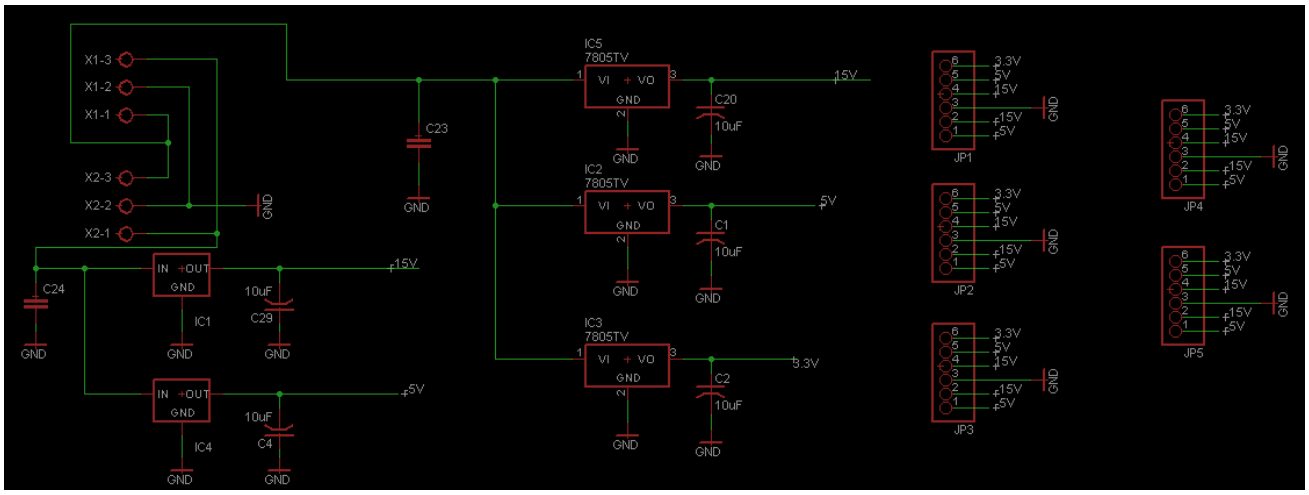

Figure 5-9: *Voltage regulator prototype schematic.*

This voltage supply was implemented in PCB as it can be seen in Figure 5-10 and Figure 5-11.

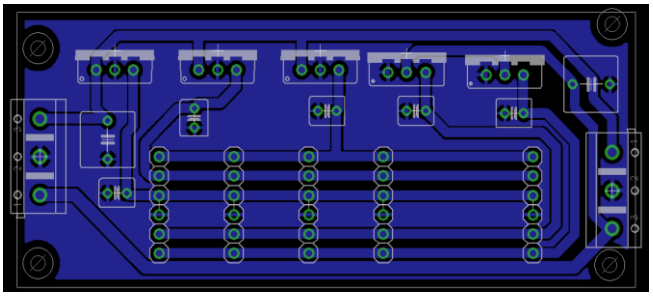

Figure 5-10: *Voltage regulator prototype PCB preview.*

Figure 5-11: *Voltage regulator prototype PCB.*

As it can also be seen in Figure 5-11, the voltage supply was able to provide power for several boards, making it essential during the prototyping phase. With the implementation of this boar, the necessity to configure a power circuit was eliminated, avoiding the overwhelming of wires in the circuit. This board reveled to be a good solution because it was very easy to use.

5.1.4 Power emitter prototype

The power emitter prototype was designed to be an H-Bridge. Therefore, it was required two operational amplifiers to amplify the signals. One for each push-pull. One of the operational was configured to apply a positive gain to the signal and the other, a negative, as it can be seen in Figure 5-12.

Although this solution wasn't the best because the mismatch of the two gains, it was acceptable for the prototype requirement. At the end it revealed to work perfectly and is yet used as a backup board.

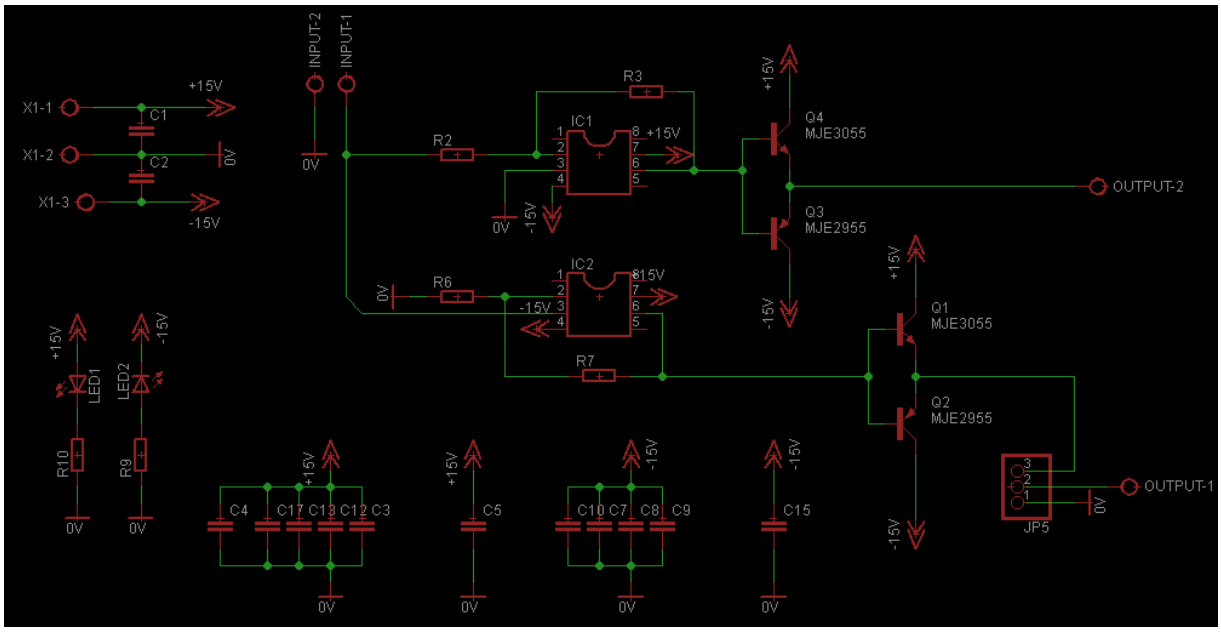

Figure 5-12: *Power emitter prototype schematic.*

This power amplifier was implemented in PCB as it can be seen in Figure 5-13 and Figure 5-14.

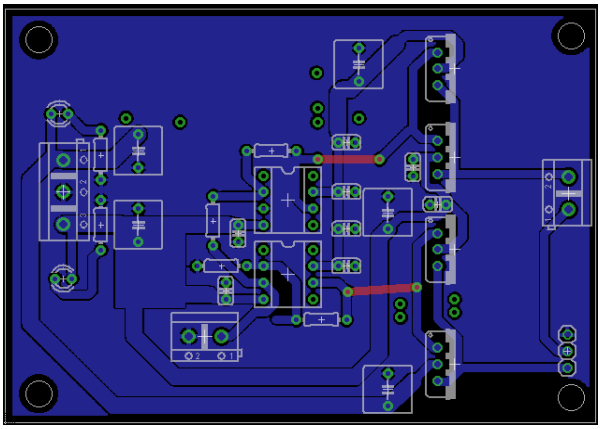

Figure 5-13: *Power emitter prototype PCB preview.*

Figure 5-14: *Power emitter prototype PCB.*

5.1.5 Spartan 3 prototype

Once the electronic was tested in the Arduino, the project moved to FPGA. A Spartan 3, existent in the lab was used. However, because the DAC and ADC's clock signals were 25 MHz, flying wires didn't worked properly. So, in order to make proper connection, between the electronics and the FPGA, a specific connector had to be designed.

Figure 5-15 depicts the developed connector. It can be seen a 48 pin DIP connector that connects the FPGA to the DAC and ADC's connectors, previously made.

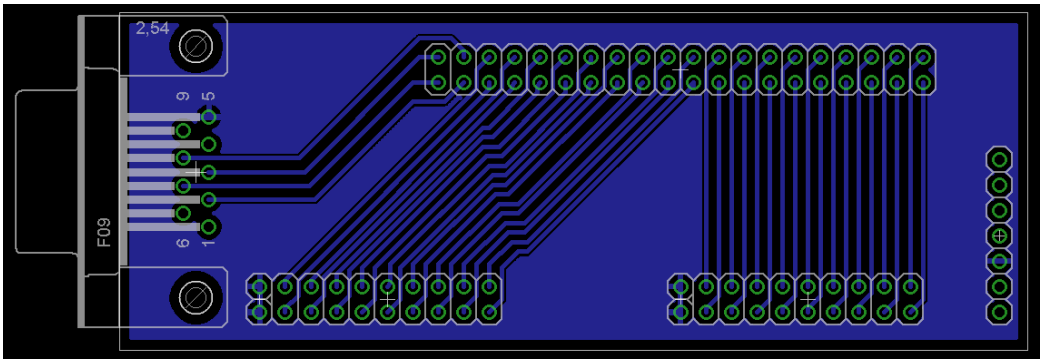

Figure 5-15: *Spartan 3 adapter for DAC and ADC prototypes.*

The Spartam 3 was connected to the generic adaptor board, the FX2-BB and all the electronics were connected to it, as depicted in Figure 5-16.

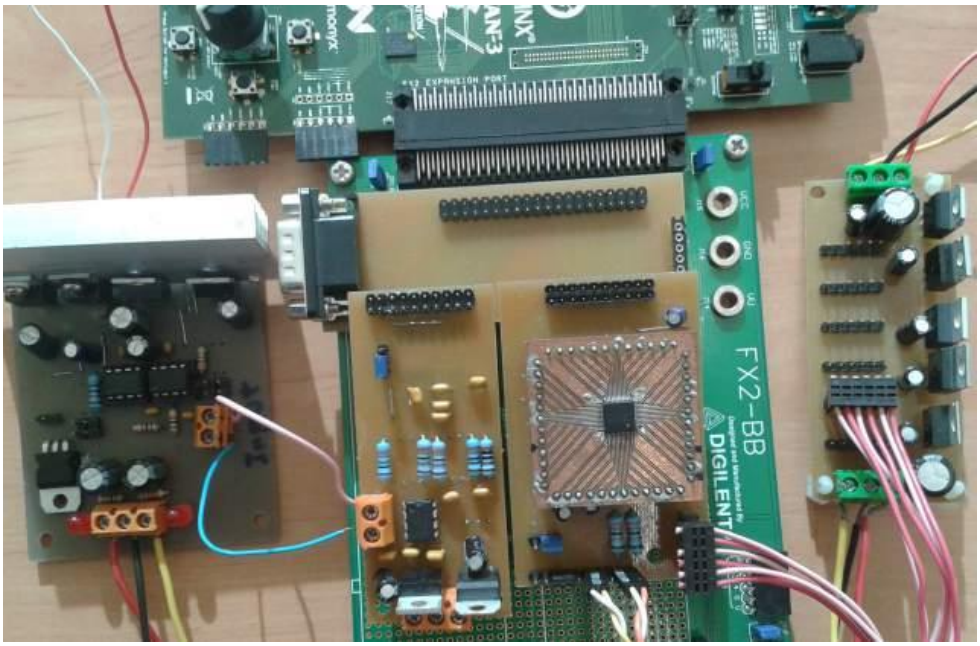

Figure 5-16: *Spartan 3 prototype setup.*

5.2 Full system prototype

After the DAC, ADC and Power amplifier testing, a final prototype was made. This prototype, also included all the instrumentation to receive, filter and apply gain to the hydrophone's signal.

5.2.1 Instrumentation circuitry

Although all the instrumentation were connected and worked as a sequence of IC's, its development were mad in several different steps, detailed in the next sub sections.

To test the instrumentation, firstly some more SMD to DIP adaptor boards were made. This task had to be done since the used ICs were all SMD. Thus an adapter board was made for the AD8429, the AD8184, the THS7001 and the LT6600-5, in Figure 5-17 (from left to right).

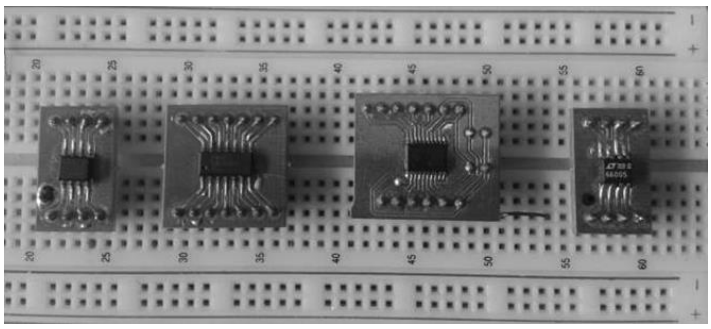

Figure 5-17: *Adapter boards for AD8429, AD8184, THS7001 and LT6600-5.*

5.2.1.1 DAC

The final version of the DAC (Figure 5-18) circuit replaces the differential amplifier used in the prototype by a RF transformer. This has proven to be a reliable solution because it requires fewer components and automatically converts the differential DAC's current to a single ended voltage. It can also be seen that the entire DAC and its instrumentation only requires a single $3.3\ V$ voltage supply.

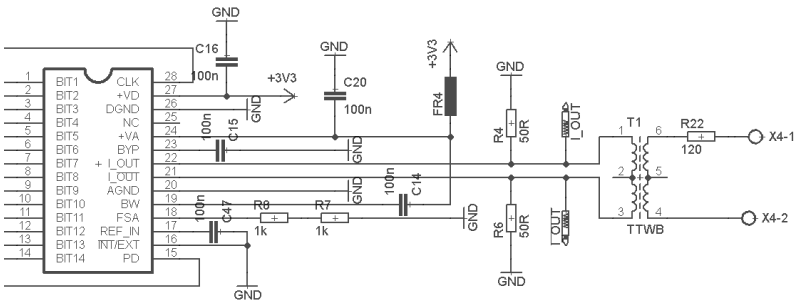

Figure 5-18: *DAC circuit.*

5.2.1.2 ADC

The ADC's circuitry final version, uses a differential configuration for the analog sampling, with an offset voltage of $2.5\ V$.

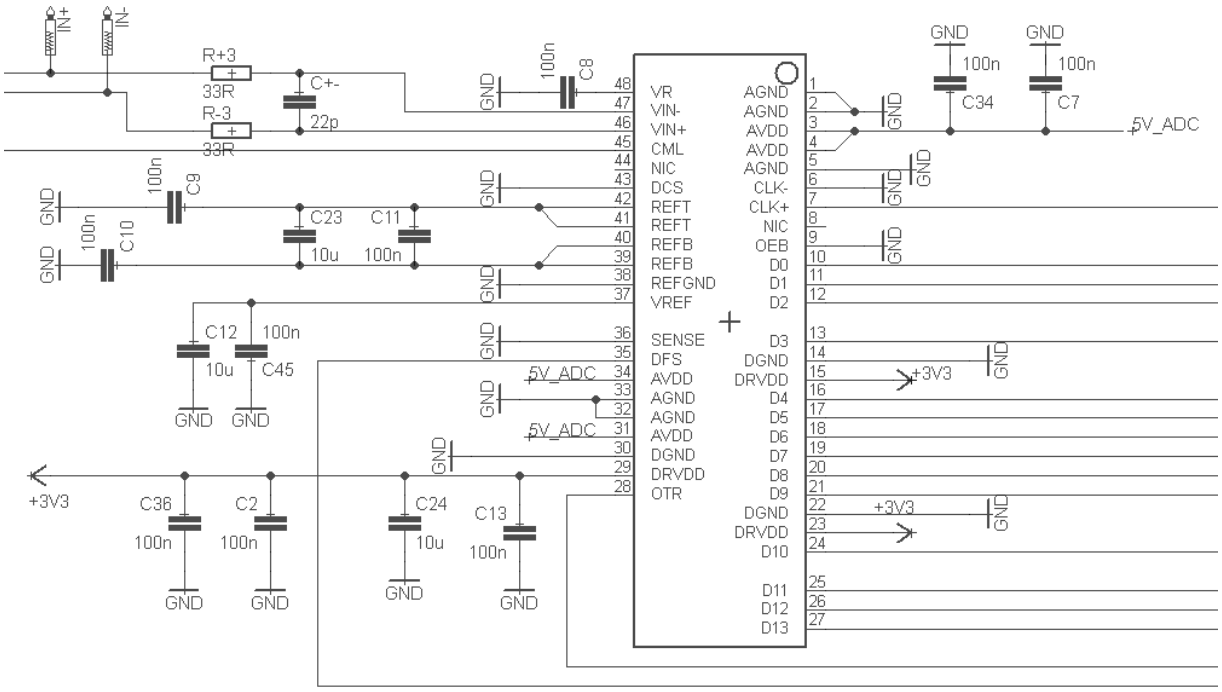

Figure 5-19: *ADC circuit.*

5.2.1.3 Antialiasing LPF

The antialiasing LPF, the LT6600-5 receives a single ended signal through the VOUT_PGA pin and applies a gain of 4, configured by the external resistors (Figure 5-20). It also inserts an offset determined by the V_COM pin, which is set by de ADC. Finally it filters the signal and converts it to differential.

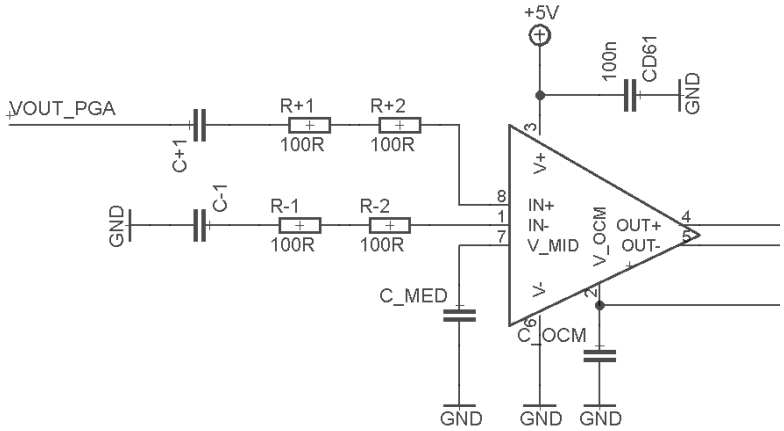

Figure 5-20: *Antialiasing LPF circuit.*

5.2.1.4 VGA

The THS7001 preamplifier is configured in inverted mode with a gain of 1, set by $R12/R11$ (Figure 5-21).

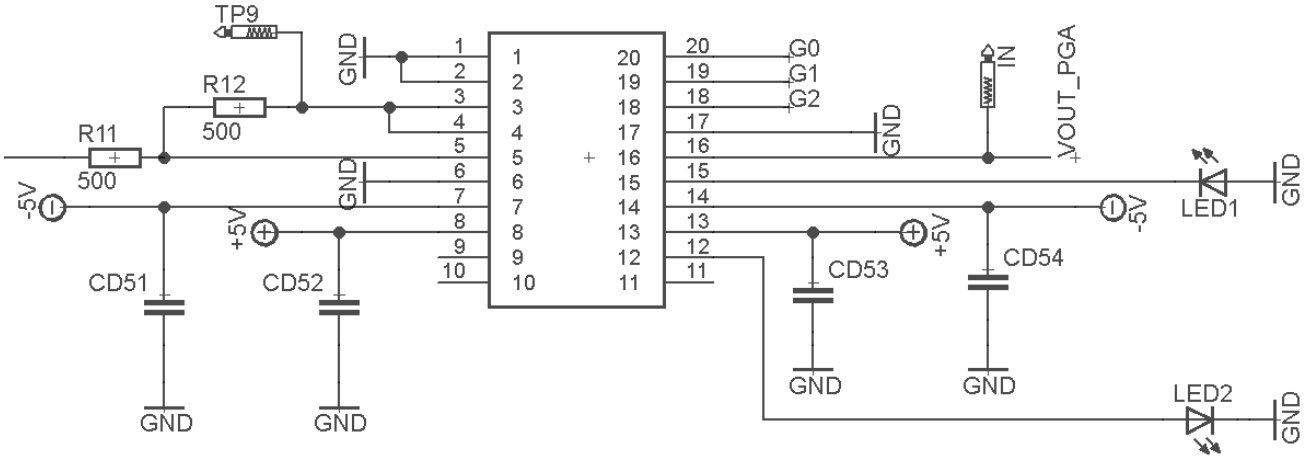

Figure 5-21: *VGA circuit.*

5.2.1.5 Analog multiplexer

The analog multiplexer, the AD8184, is implemented with no external electronics, besides two decoupling capacitors, as seen in Figure 2-22. This component implements the selection of which of the signals is passed to the VGA next to it.

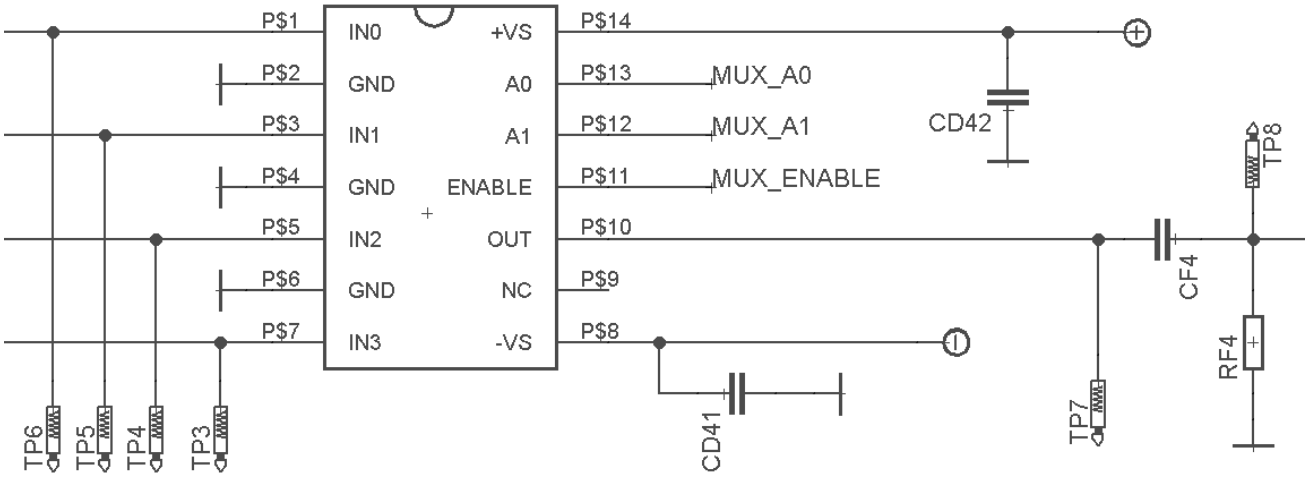

Figure 5-22: *Analog multiplexer circuit.*

5.2.1.6 Fixed gain amplifiers

The fixed gain amplifiers are implemented with a voltage divider, (for the case of attenuation) and with low noise instrumentation amplifiers AD8429. It can be seen in figure 5-23 two HPF, (CF2 and RF2) and (CF3 and RF3), which are used to remove the offset voltage inserted in the amplification process by the IA.

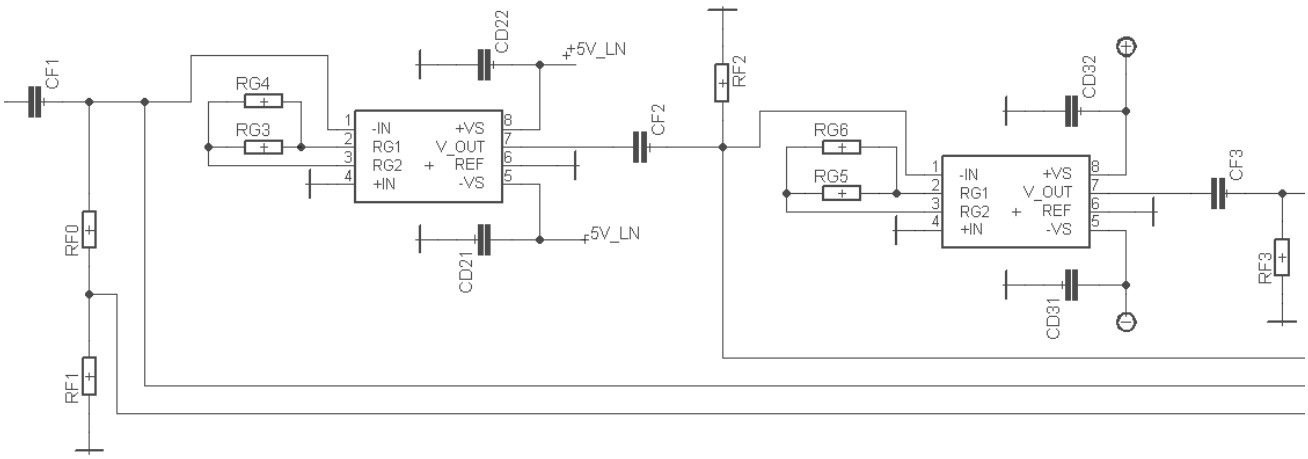

Figure 5-23: *Instrumentation amplifiers circuits.*

5.2.1.7 Hydrophone selector system

To select which hydrophone's signal passes to the HPF, a mechanical switch is used as a selector. This way, one hydrophone can be plugged to the system through the voltage buffer and other directly connected the HPF (Figure 5-24).

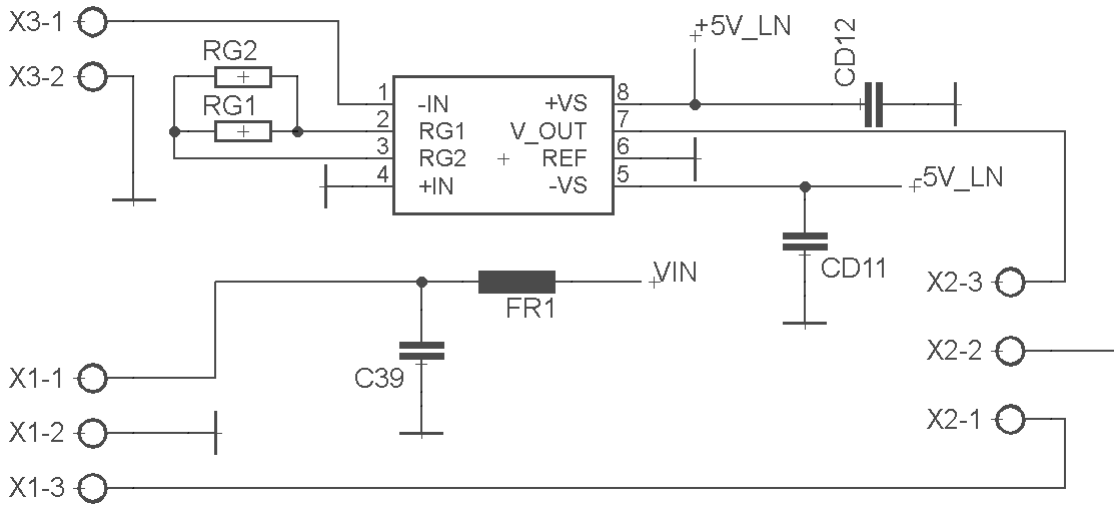

Figure 5-24: Hydrophone input selector switch.

5.2.2 PCB

The above circuits were designed and a PCB was made (Figure 5-25). This PCB was soldered and connected to a ZTEX adapter. Figure 5-26 depicts the PCB after soldering.

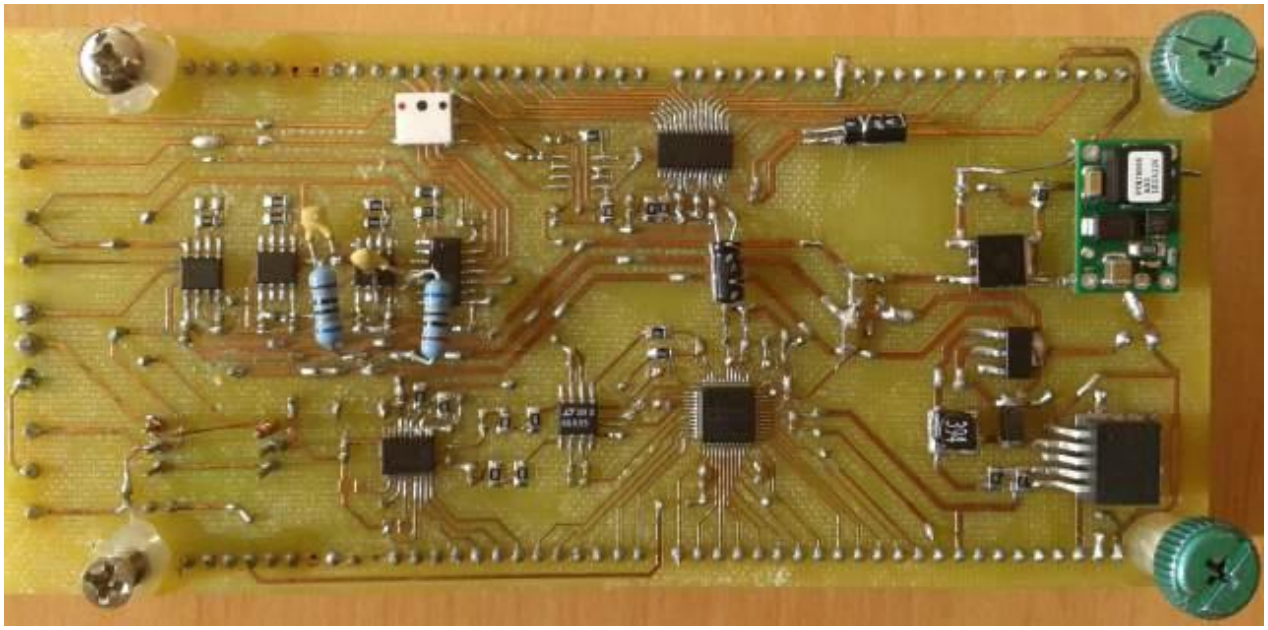

Figure 5-25: *Full system prototype PCB.*

To connect the final prototype to the new FPGA, a ZTEX experimental (Figure 5-26) board was used. This way, the system was connected to a more powerful and smaller FPGA.

The Full instrumentation prototype, in Figure 5-26 depicts the prototype final setup.

Figure 5-26: *Full system prototype setup.*

5.3 Final PCB design

After the successful testing of the final prototype (mentioned above), its circuit was redesigned (Figure 5-27) to make a definitive hardware version in an even smaller and more convenient board.

After the production, the board was hand soldered, (Figure 5-28).

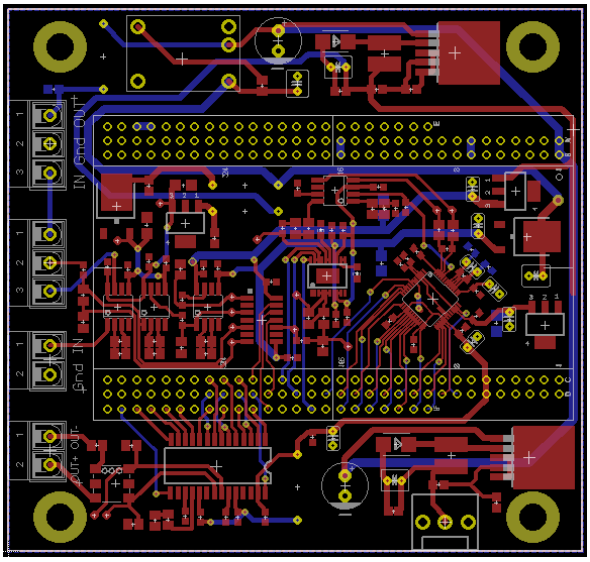

Figure 5-27: *Final system PCB preview.*

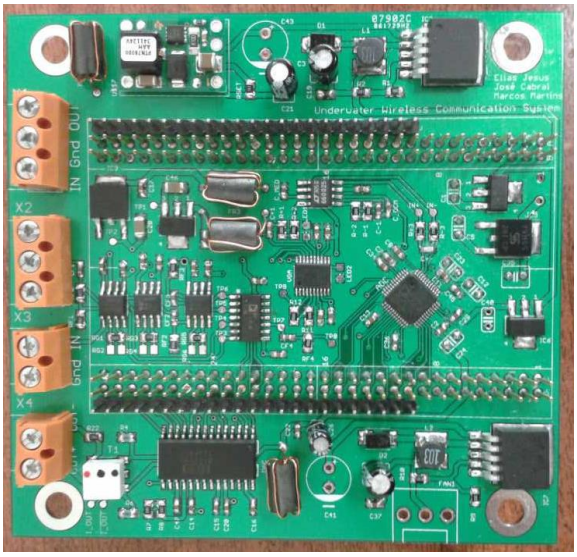

Figure 5-28: *Final system PCB.*

The final setup of the instrumentation can be seen in Figure 5-29. It can also be seen the wires to connect the hydrophones, the selector switch and the output signal from the RF transformer.

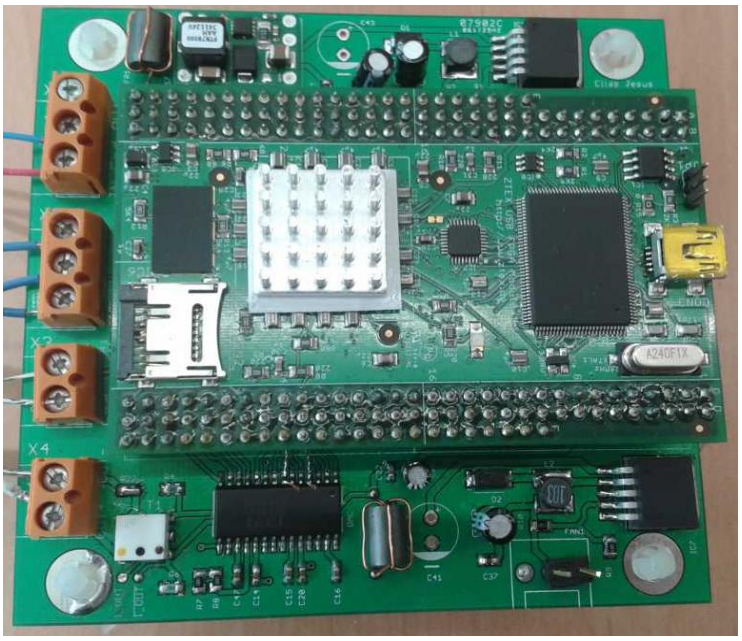

Figure 5-29: *Final system setup.*

5.4 Power emitter implementation

The power emitter was developed in a separate board to make it possible to be placed far from the instrumentation.

5.4.1 Power emitter circuit design

Figure 5-30 shows the signal entering the LPF and then being transformed by the RF transformer. At the secondary of the transformer, it can be seen that the middle output is connected to the ground, which configures it to operate in differential mode.

The RF transformer output signal is then amplified by the LM7171 which drives the push-pull, has Figure 5-33 depicts

At Figure 5-31 if can be seen the operational amplifier and the BJTs of the power push-pull. The two BJTs are set in a Darlington configuration to augment its current sourcing capabilities. It also provides extra protection for the operational amplifier.

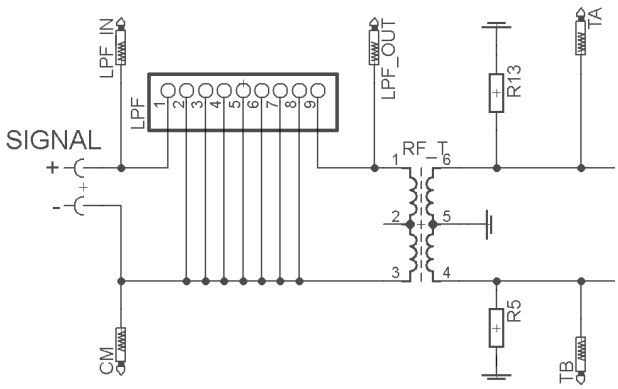

Figure 5-30: *Input LPF and RF transformer schematic.*

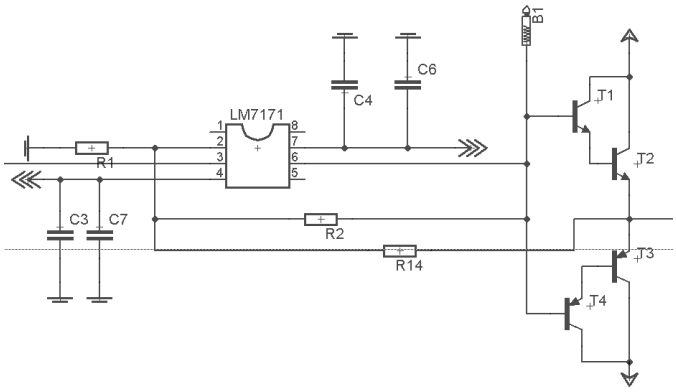

Figure 5-31: *Operational amplifier and power push-pull schematic.*

Figure 5-32 shown the schematic of the virtual ground generator circuit. It also shown the $\pm 18\ V$ regulators, producing a $\pm 18\ V$ voltage relatively to the virtual ground being generated.

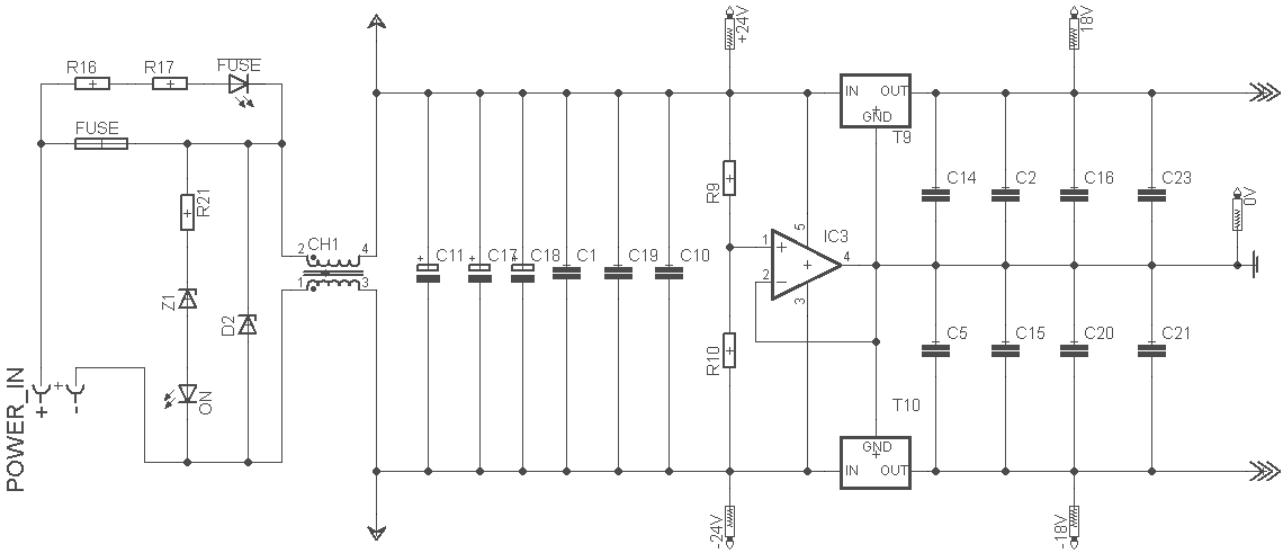

Figure 5-32: *Operational amplifier's voltage regulators and virtual ground schematics.*

5.4.2 Power emitter PCB design

The Final power amplifier circuit was designed in PCB, as it can be seen in Figure 5-33

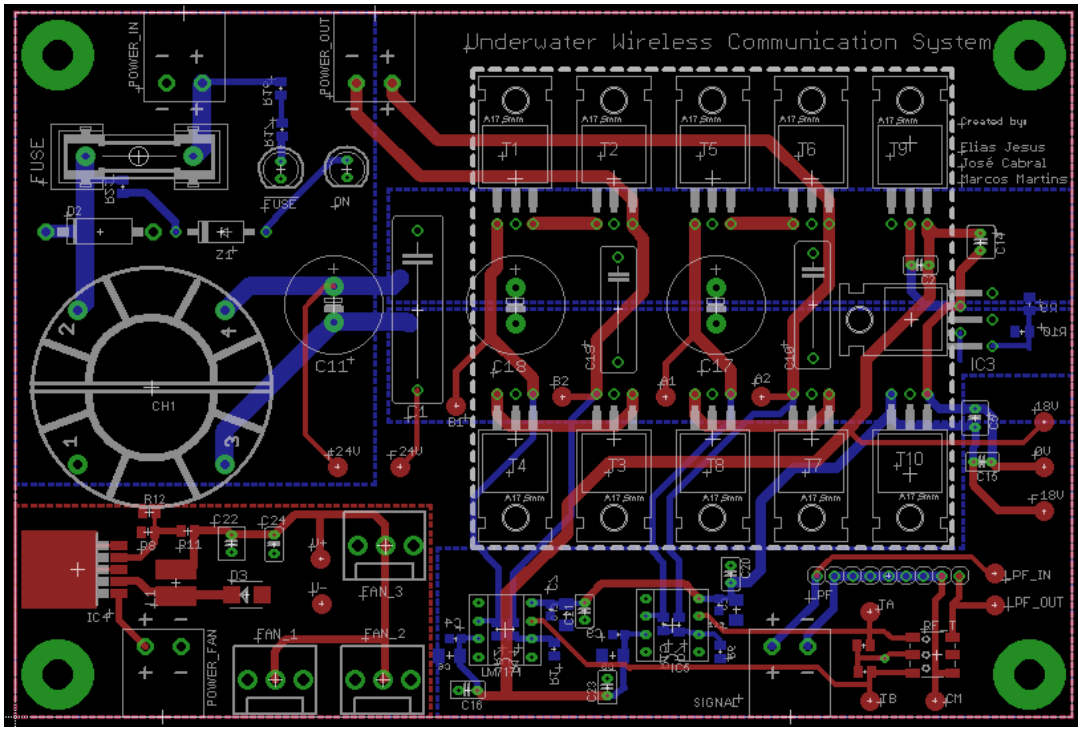

Figure 5-33: *Power amplifier PCB preview.*

After the PCB production, it was hand soldered (Figure 5-34.

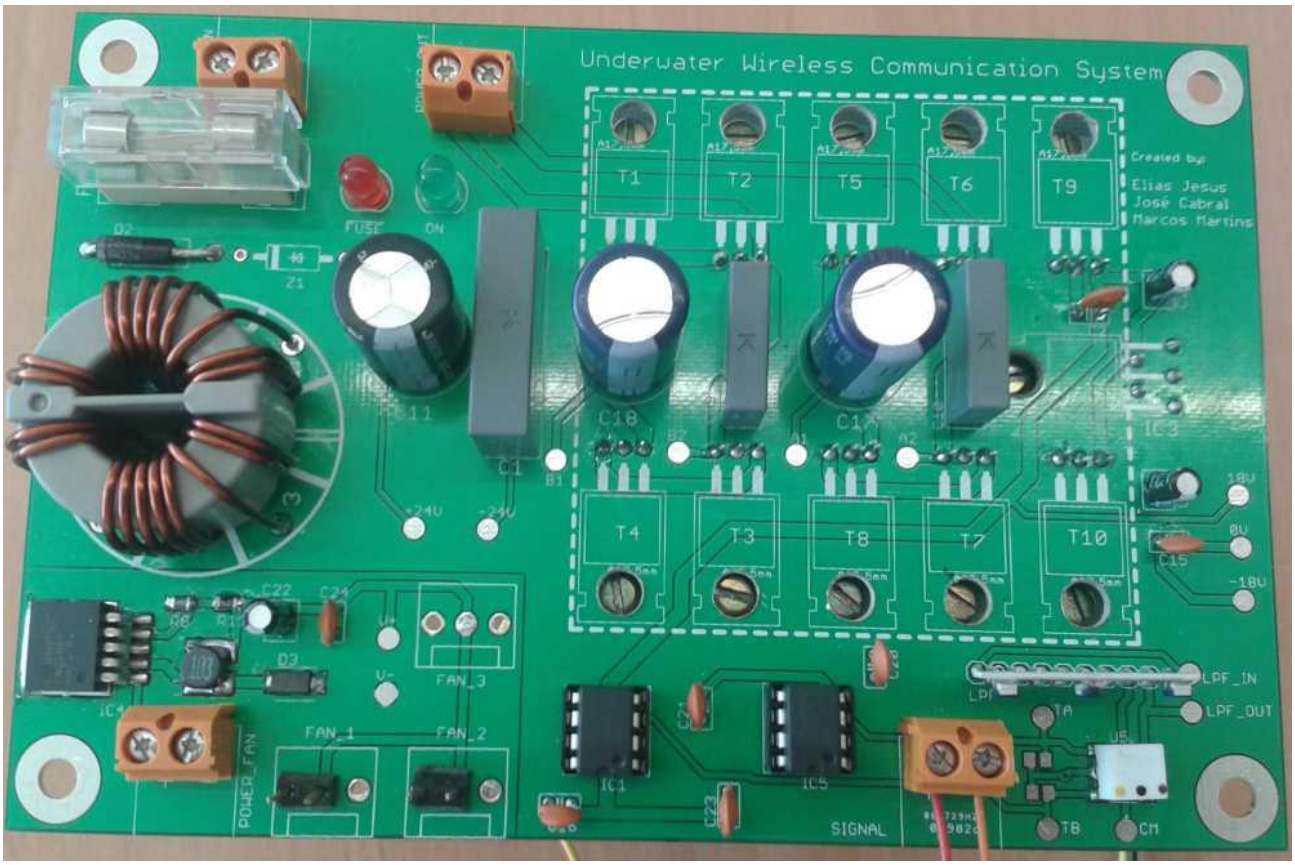

Figure 5-34: *Power amplifier PCB.*

Because of the heat generated by the Power BJT's, an aluminum heat dissipater was used and a computer fan was placed on it (Figure 5-37).

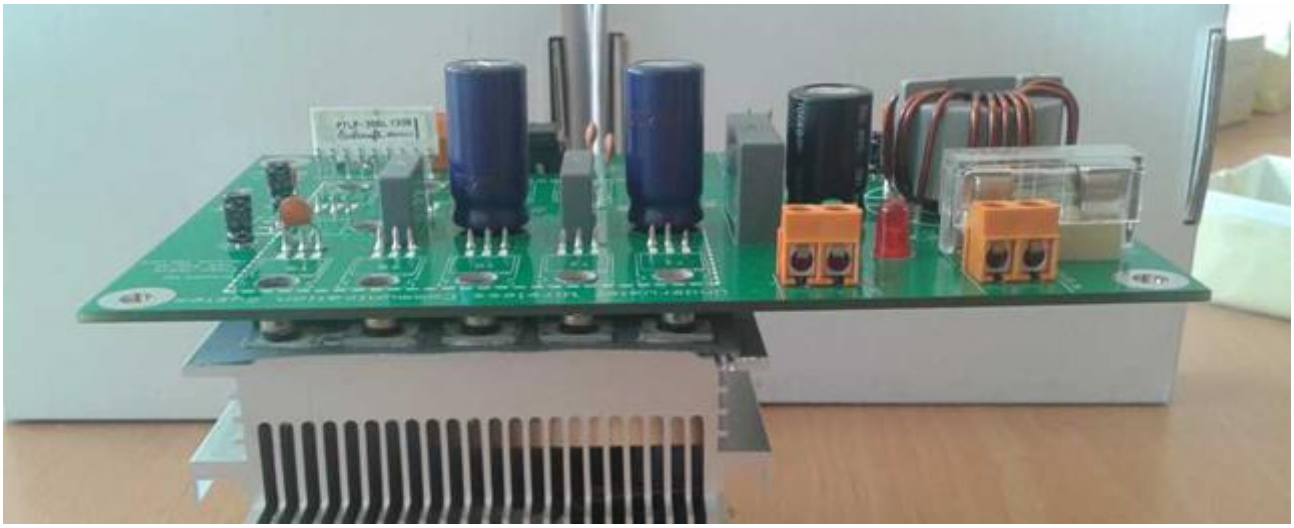

Figure 5-35: *Cooler and fan setup.*

5.5 Software implementation

To implement the host applications' algorithm, it was developed an application in Java, as it can be seen in Figure 5-36. The application reads the file to be sent, sends it in 512 Byte packets to the microcontroller and verifies it there is data to read from it. In case there is, the data is written to the receiving file.

When the sending of the file is finish, the application makes, yet, $listeningAttempts$, attempts to read data from the demodulator, to act as a passive listening device. Each attempt takes $5\ ms$, therefore the listening period S, in seconds is $S = 200 * listeningAttempts$.

This value represents "listening period" and can be change when convenient.

```
int USB_BLOCK_SIZE = 512;
byte[] inputFileBuffer = new byte[512];
byte[] usb_input_buffer = new byte[512];
while((nRead = inputStream.read(inputFileBuffer)) != -1) {
    // Fill the last DATA Packet with 0x00 to complete the commended block size, 512.
    if(nRead < USB_BLOCK_SIZE){
        for(int i = nRead; i < USB_BLOCK_SIZE; i++){
            inputFileBuffer[i]= 0x00;
            }
    }
    // Sending DATA Packets to the uC.
    int i = LibusbJava.usb_bulk_write(handle(), 0x04, inputFileBuffer, inputFileBuffer.length, 5);
    if ( i<0 )  { System.out.println("Modulator busy..."); }
    // Receiving DATA Packets from the uC.
    i = LibusbJava.usb_bulk_read(handle(), 0x82, usb_input_buffer, usb_input_buffer.length, 5);
    if ( i>-1 ){
        // Save the input DATA Packet to  the receiving file.
        try {
            FileOutputStream outputStream = new FileOutputStream(receiveFileName, true);
            outputStream.write(usb_input_buffer);
            outputStream.close();
        }
        catch(IOException ex) {
            System.out.println("Error writing to file '" + receiveFileName + "'");
        }
    }
    usbPacket++;
}
// Always close the file.
inputStream.close();
// continue to receive after the sending is done.
for( int a = 0; a < listeningAttempts; a++ ){
    int i = LibusbJava.usb_bulk_read(handle(), 0x82, usb_input_buffer, usb_input_buffer.length, 5);
    if ( i>-1 ){
        // Save the input DATA Packet to  the receiving file.
        try {
            FileOutputStream outputStream = new FileOutputStream(receiveFileName, true);
            outputStream.write(usb_input_buffer);
            outputStream.close();
            System.out.println(".");
        }
        catch(IOException ex) {
            System.out.println("Error writing to file '" + receiveFileName + "'");
        }
    }
}
```

Figure 5-36: *Java codding for the host echo application.*

5.6 Firmware implementation

In the ZTEX USB-FPGA Module 1.15d, the Cypress EZ-USB FX2LP microcontroller is hardwired to the Spartan 6 FPGA, through several I/O Port. As it can be seen in the ZTEX USB-FPGA Module 1.15d specification sheet, the I/O ports IOB, IOC and IOD are connected to the FPGA. For the purpose of this implementation, only these I/O ports are used, because they provide enough bits to the needs of this project. In Table 5-1 it can be seen the microcontroller pins being used and the signals they represent.

Table 5-1: *Microcontroller pinout.*

Name	Pins [MSB:LSB]	Type
dDATA	IOB[7:0]	Input
dDATA Available	IOD[0]	Input
dDATA Clear	IOD[1]	Output
mDATA	IOC[7:0]	Output
mDATA Available	IOD[2]	Output
mDATA Request	IOD[3]	Input

Considering the previous pinout, in Table 5-1, the microcontroller's firmware was developed in C to implement the microcontroller's firmware flowchart, depicted in the firmware design section. In Figre 5-37 it can be seen that the microcontroller verifying if there is any data request from the modulator or from the demodulator.

```
if ( run && !(EP4CS & bmBIT2) ) {   // if there is a packet to be delivered to the modulator...
    EP4State = (EP4BCH << 8) | EP4BCL;
    // loops the data packet to deliver to the modulator..
    EP4Index=0;
    while(EP4Index<EP4State){
        // if the modulator requests data..
        if(IOD3 == 1) {
            IOD2 = 0;
            IOC = EP4FIFOBUF[EP4Index]; // data from EP4 is sent to the modulator...
            IOD2 = 1;
            EP4Index++;
            while (IOD3 == 1) {}
        }
        // if there is data do collect from the demodulator...
        if (IOD0 == 1) {
            EP2FIFOBUF[EP2Index] = IOB;
            IOD1 = 1;
            IOD1 = 0;
            while (IOD0 == 1) {}
            EP2Index++;
            // If the Buffer is full, then request to send data to the host
            if(EP2Index == 512 ){
                EP2BCH = EP2Index >> 8;
                SYNCDELAY;
                EP2BCL = EP2Index & 255;
                EP2Index = 0;
            }
        }
    }
    // After sending all packet to the modulator, requests more data to the host,
    SYNCDELAY;
    EP4BCL = 0x80;
}
```

Figure 5-37: *microcontroller's firmware implementation in C.*

5.7 Logic system implementation

At the logic layer level, it was convenient to decompose each of the modulator and demodulator units into smaller modules within those, to provide a reduction in complexity. This decomposition is detailed in the following section.

5.7.1 Demodulator unit implementation

The demodulator unit is composed by an upper module which specifies the unit's connection with the microcontroller. It can be verified that this unit has one input and two output connections, as listed in Table 5-2.

Table 5-2: *Demodulator unit I/O interface.*

Name	Description	Type
DATA Clear	Flag to indicate that the microcontroller has received the Byte.	Input
DATA Available	Flag to indicate that there is a Byte to be read from the demodulator.	Output
DATA	Out coming Byte from the demodulator to the microcontroller.	Output

These three I/O signals from the demodulator unit are connected to the microcontroller through the FPGA I/O pins, listed in Table 5-3.

Table 5-3: *Demodulator unit microcontroller interface.*

Name	Pins [MSB:LSB]	Type
dDATA	{'Y9','Y6','W6','AB8','AA8','W13','V13','Y17'}	Output
dDATA Available	{'V21'}	Output
dDATA Clear	{'V22'}	Input

The overall demodulator unit module is depicted in Figure 5-38, where it is seen the connections between the demodulator unit and the microcontroller interface. Details about the FPGA I/O pins are in Table 5-3.

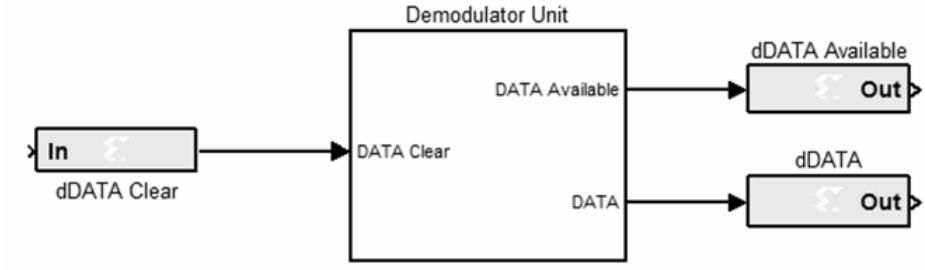

Figure 5-38: *Demodulator unit microcontroller interface.*

Inside the demodulator unit, there were implemented modules such as the OTR unit, the Demodulator, the VGAUC and the 24 MHz ADC clock as well as the required logic to interface these modules, as figure 5-39 shows.

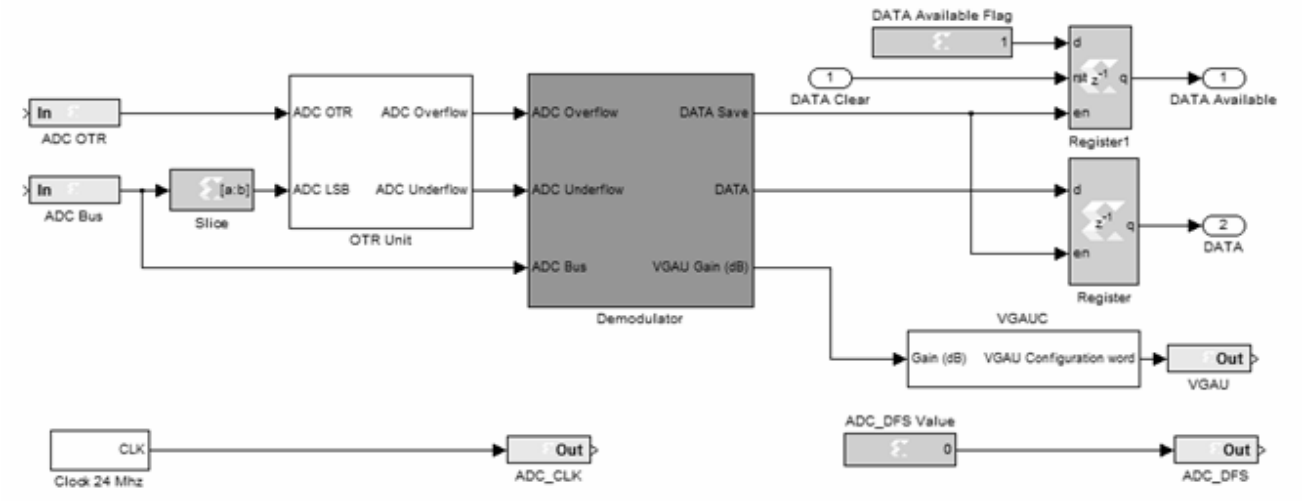

Figure 5-39: Demodulator unit details.

Figure 5-39 also shows the connections between the logic signals and the hardware electronics. The FPGA I/O pins through which these connections are made are listed in Table 5-4.

Table 5-4: *Demodulator unit electronics connections.*

Name	Pins [MSB:LSB]	Type
ADC_CLK	{'Y15'}	Output
ADC_DFS	{'V20'}	Output
ADC_OTR	{'Y22'}	Input
ADC_Bus	{'AA22','AA21','Y21','AB21','W20','Y20','AA20','AB20','V19','AB19','Y19', 'AB18','V18','AA18'}	Input

The demodulator module is the module which isn't yet implemented, therefore only its skeleton and its connections were implemented. Those connections are listed and described Table 5-5.

Table 5-5: *Demodulator interface.*

Name	Description	Type
ADC Overflow	Indicates the ADC Overflow	Input
ADC Underflow	Indicates the ADC Underflow	Input
ADC Bus	ADC 14-Bit Bus	Input
DATA Save	New Byte to save indication flag	Output
DATA	DATA Byte	Output
VGAU Gain	$-21\ \mathrm{dB} \leq$ Analog gain $\leq 110\ \mathrm{dB}$	Output

The VGAUC module is completed and its FPGA I/O pins interface pins are listed in Table 5-6.

Table 5-6: *VGAU hardware interface.*

Name	Pins [MSB:LSB]	Type
VGAUGain	{'AA14','AB14','Y10','Y11','V15','AB15'}	Output

5.7.1.1 VGA controller unit implementation

Based on the VGAUC design section, it has to convert the gain requested from the demodulator to a VGAU configuration word, which is implemented in hardware. To do that, the VGAUC stores the VGAU configuration words in a memory and uses the gain values, from the demodulator, to access the corresponding memory index. This way, when the demodulator requests a certain gain, it is actually selecting which position's word is sent to the hardware VGAU.

Based on Table 4.3, the VGAU can apply an analog gain between $106\ dB$ and $-21\ dB$ in intervals of $6\ dB$. Therefore, it was found convenient to implement a signed 8-bit interface between the demodulator and the VGAUC, this way, the demodulator can request a gain between $-128\ dB$ and $127\ dB$, being truncated to $-21\ dB$ and $106\ dB$ by the VGAUC.

Because the gain is set in $6\ dB$ steps, the 256 possible gain values generated by the demodulator correspond to only $256/6 \approx 43$ different configuration words, thus, and algorithm is implemented to convert the requested gain into the VGAU configuration word. This algorithm can be seen in Figure 5-40.

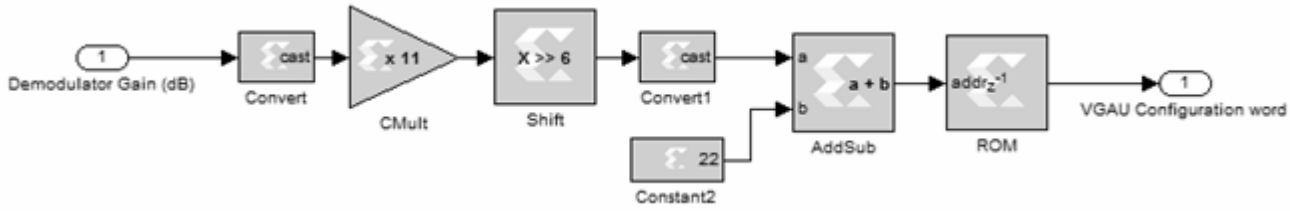

Figure 5-40: *VGAU configuration word selection.*

In Figure 5-41 it can be seen the VGAU analog as function of the VGAUC memory selected index.

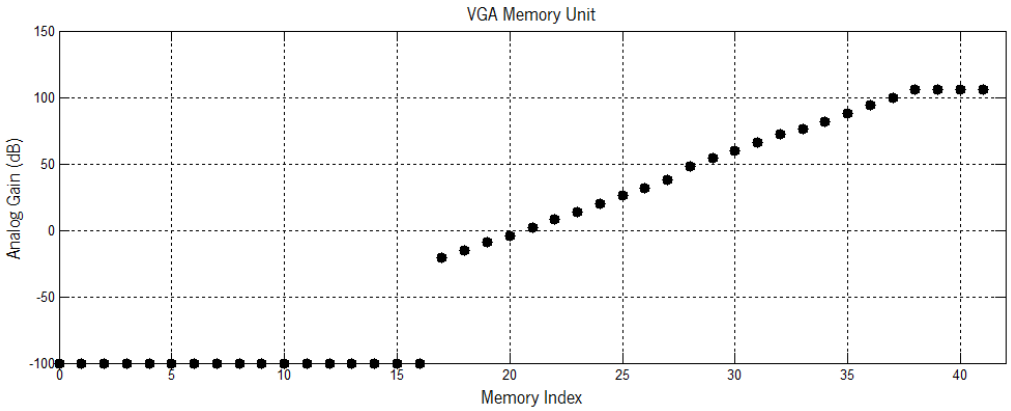

Figure 5-41: *Analog gain vs. selected memory index.*

5.7.2 Modulator unit implementation

The modulator unit is also composed by an upper module which specifies the unit's connection with the microcontroller. It can be verified that this unit has two inputs and one input connection, as listed in Table 5-7.

Table 5-7: *Modulator unit microcontroller interface.*

Name	Pins [MSB:LSB]	Pin
mDATA Available	{'U20'}	Input
mDATA	{'H18','H19','H20','G19','AB9','Y5','T20','G20'}	Input
mDATA Request	{'U22'}	Output

These three I/O signals from the modulator unit are connected to the microcontroller through the FPGA I/O pins. The overall modulator unit module is depicted in Figure 5-42 where it can be seen the connections between the modulator unit and the microcontroller interface.

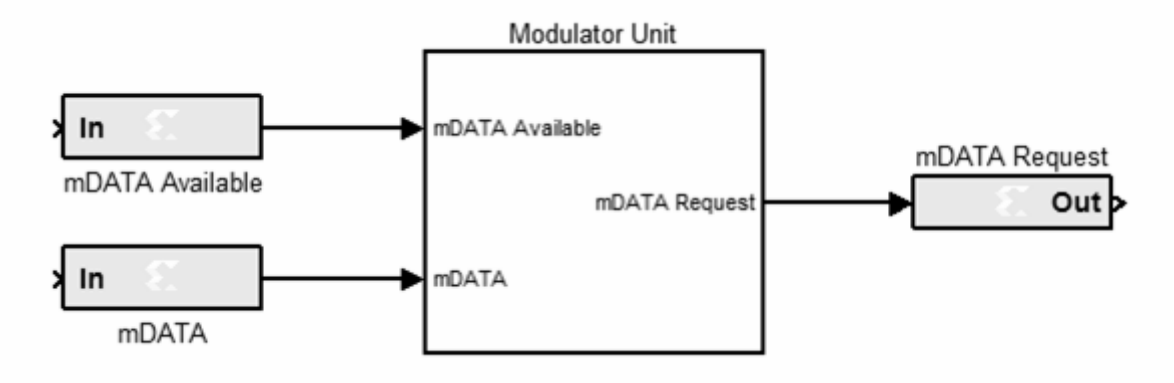

Figure 5-42: *Modulator unit microcontroller interface.*

Inside the modulator unit, it was implemented the modulator module and, the 24 MHz ADC clock and the required logic to interface these modules, as Figure 5-43 shows.

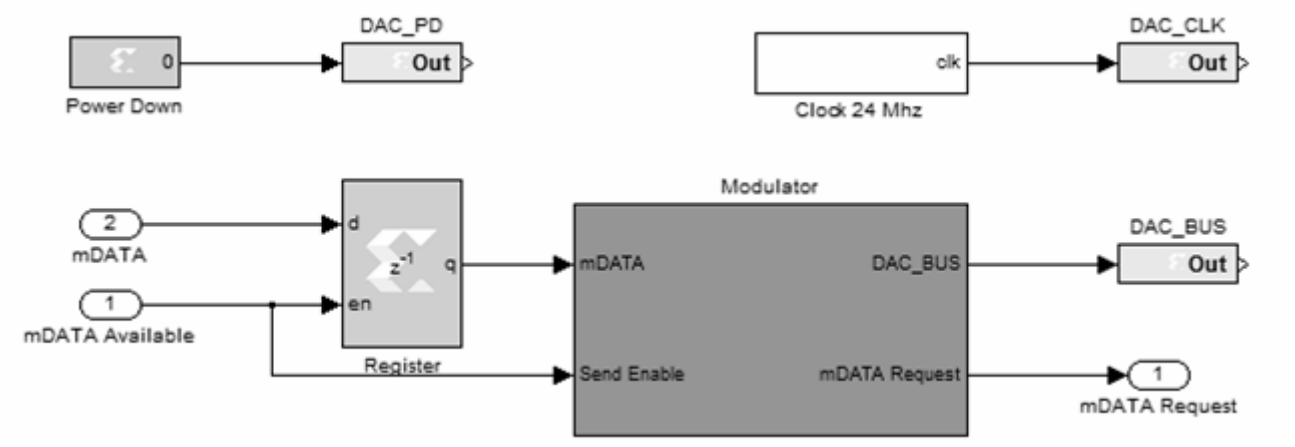

Figure 5-43: *Modulator unit details.*

Figure 5-43 also shows the connections between the logic signals and the hardware electronics. The FPGA I/O pins through which these connections are made are listed in Table 5-8.

Table 5-8: *Modulator unit electronics connections.*

Name	Pins [MSB:LSB]	Type
DAC_CLK	{'AB12'}	Output
DAC_PD	{'AA6'}	Output
DAC_Bus	{'AB11','AB10','AA10','W11','Y13','T14','U14','W9','W12','Y12','Y8', 'AB7','Y7','AB6'}	Input

The modulator module is the modulator unit's module which isn't yet implemented, therefore only its skeleton and its connections were implemented. Those connections are listed and described Table 5-9.

Table 5-9: *Modulator interface.*

Name	Description	Type
mDATA	Byte to be modulated.	Input
Send Enable	Start the modulation process flag.	Input
DAC_Bus	14-bit DAC bus	Output
mDATA_Request	DATA request flag, from the modulator to the microcontroller.	Output

5.8 System integration

The final system integration can be seen Figure 5-36, where it can be seen that he emitter and receiver circuits can be used separately and the signal is transmitted through a BNC cable.

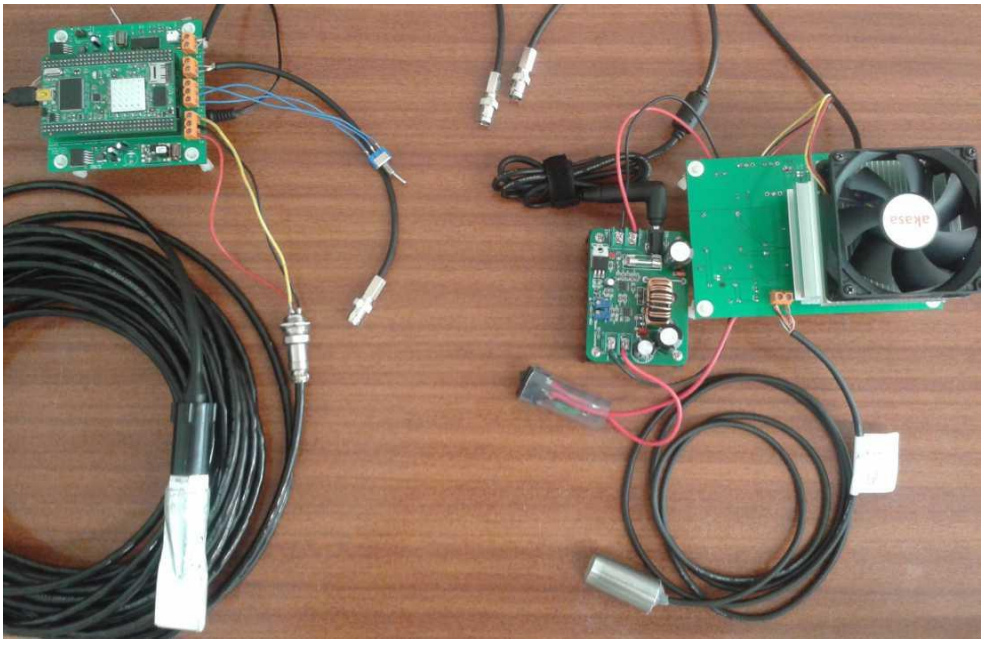

Figure 5-44: *Final system integration.*

Chapter 6

6 Tests and results

For the purpose of evaluate the system's performance, some tests were made to determine the system behavior in some key features. Since the system was built in modules, those modules were firstly tested and then testes to the all system were performed.

This way modular testes were made to the host application, the microcontroller firmware, the logic system, the signal acquisition circuitry and the power electronics. These modular tests, aimed to measure the user interface, microcontroller, modulator and demodulator performances as well as the signal acquisition, signal generation and power electronics subsystems response.

Meaning while, to test the system's performance as an all, the system was configured to work as an ultrasonic emitter and receiver. This last test was performed in water tank, simulations the underwater environment.

To record the results of the tests mentioned above, it was used a digital oscilloscope from the Pico Technology's PicoScope 2200 Series (Figure 6-1). This oscilloscope has two channels, a bandwidth of 10 MHz with 100 MSPS for each channel, an input impedance of 1 MΩ and it is USB pluggable to the computer.

Figure 6-1: *PicoScope 2200 Series.*

6.1 Host application results

The host application was designed to parse a file, split it into 512 Bytes blocks and send those to the microcontroller through the USB2.0 connection. In the case that the microcontroller sends data to the host application, it does it also in 512 Bytes packets and the host reads then and writes it to a file.

To test this functionality, the microcontroller was programed to reflect back the received data packets implementing an echo function. This way the application opened a file, sent it to the microcontroller trough the USB2.0 connection, received it back from the microcontroller and wrote it to a file. This test was performed with success.

6.2 Microcontroller results

The microcontroller function was to forward the data from the host application to the modulator and from the demodulator to the host application.

To test these two different functionalities, a "short circuit" was made in the FPGA between the modulator and the demodulator, this way, the data sent to the modulator was received from the demodulator. With this testing setup, the microcontroller received several 512 Byte packets and sent them to the modulator, received the same packets from the demodulator and sent them to the host application. Although this context was not useful for practical applications, it emulates the logic layer for testing purposes. This test was also successfully concluded.

6.3 Logic system results

Because the logic system includes modules that are not yet developed, such as the modulator and the demodulator, which are out of this dissertation's scope, these modules were not tested. However, to ensure the proper functioning of the modulator and demodulator units, a test to each of these units was performed.

To test the demodulator unit, a logic counter was implemented in the demodulator modules to simulate the demodulation process. In this test, the bytes generated by the counter were received in the Java application and stored to a file.

To test the modulator unit, the modulator was configured to emit a single cycle sine wave, each time a new byte entered the module. With this test, it was possible to verify that the modulator received the data sent by the microcontroller.

6.4 DAC results

To measure the performance of the DAC and the RF transformer, a sine wave of three different frequencies (200 kHz, 1 MHz and 4 MHz) was reproduced, and the out coming signal was registered at the transformer terminals.

The 200 kHz and 1 MHz signals, represented in Figure 6-2 and Figure 6-3 present a reasonable sine shape, however there is a difference in amplitude. The 200 kHz signal, has shown an attenuation of $20 * log_{10}\left(\frac{0.75}{1.25}\right) = -4.44\ dB$ in voltage compared to the pretended 1.25 V. The 1 MHz signal of Figure 6-2 is as expected.

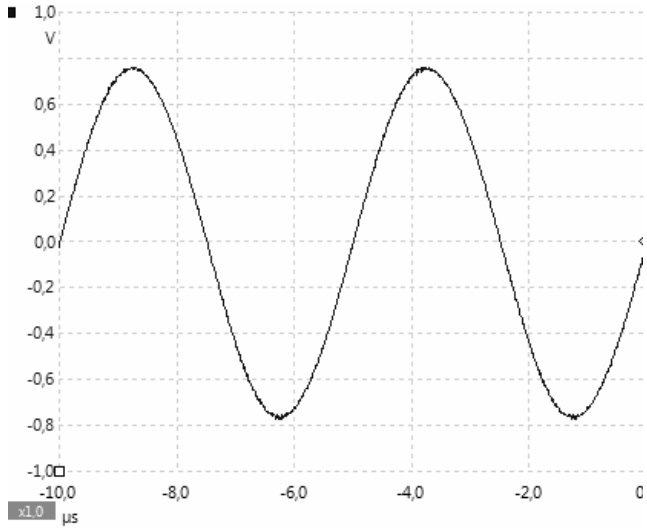

Figure 6-2: *DAC output at 200 kHz sine wave.*

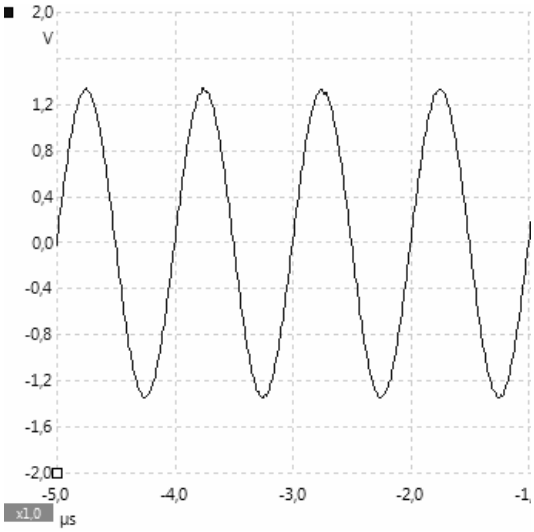

Figure 6-3: *DAC output at 1 MHz sine wave*

The 4 MHz sine wave represented in Figure 6-4 presents a huge distortion in shape and amplitude. This result is expected because the sampling frequency is 24 MHz and it means that there is only 6 samples per cycle, thus distortion is expected, according to the Nyquist theorem.

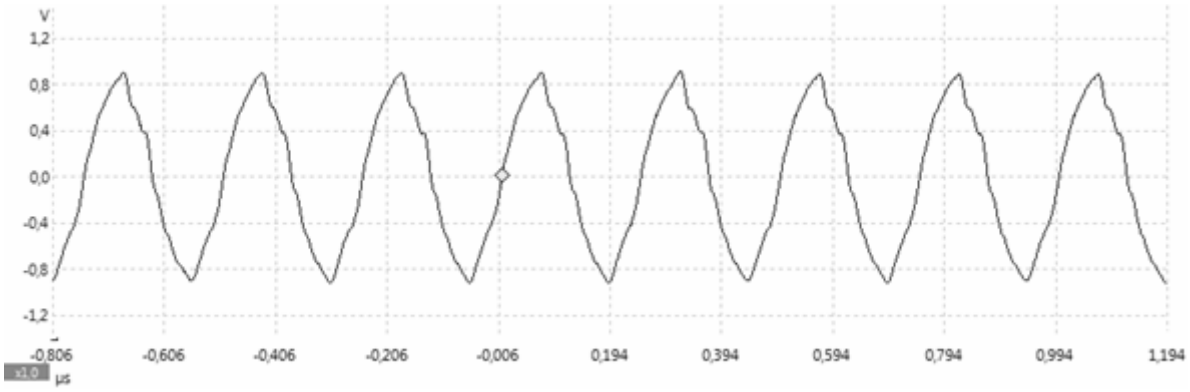

Figure 6-4: *DAC output at 4 MHz sine wave.*

6.5 Instrumentation results

To measure the performance of the signal acquisition system, several sine waves of different frequencies were inserted in the signal amplifier subsystem and the differential voltage at the ADC's input was registered. Thus, for the purposes of this test, the VGA gain was digital set and a signal was applied to the input, replacing the hydrophone.

Although frequencies of 100 kHz, 500 kHz, 1 MHz, and 2 MHz were tested, only results of 1 MHz and 2 MHz are presented because those of 100 kHz and 500 kHz were equal to the 1 MHz.

6.5.1 Maximum attenuation

To measure the VGA's capability to attenuate the input signal when it is higher than the zero dB gain equivalent input, wish is 250 mV, the gain was configured to the minimum (maximum attenuation) and a signal of 6 V was applied to the input. As it can be seen in Figure 6-5 in red, the differential voltage at the ADC's input is 500 mV, thus, doing the calculation $20 * log_{10}\left(\frac{0.4}{6}\right)$ the gain is $-21.58\ dB$. This result was the same in all tested frequencies.

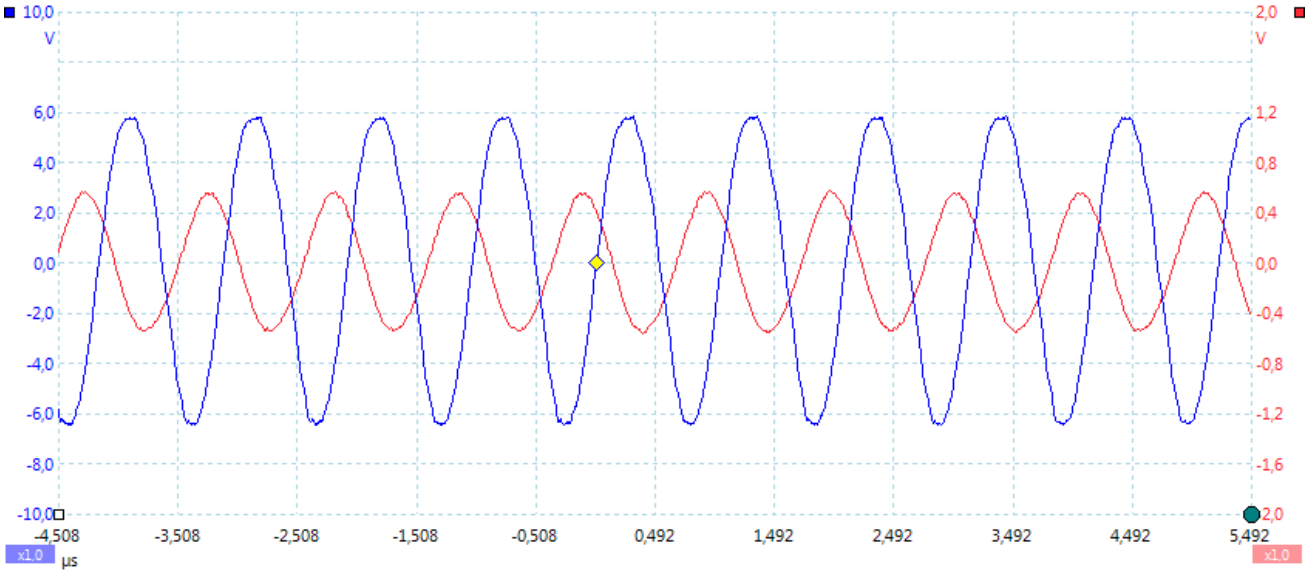

Figure 6-5: *VGA unit as attenuator.*

6.5.2 Small Gain

To measure the VGA's capability to apply gain to the input signal, it was set to have a gain of 14 dB, and two signals were applied at the input; a 1 MHz and a 2 MHz sine wave.

The 1 MHz input signal, in blue, ate Figure 6-6 is 100 mV and the VGA unit's output voltage, in red, is 600 mV, thus, by doing $20 * log_{10}\left(\frac{0.6}{0.1}\right)$ the applied gain is $15.54\ dB$, which is close to the expected.

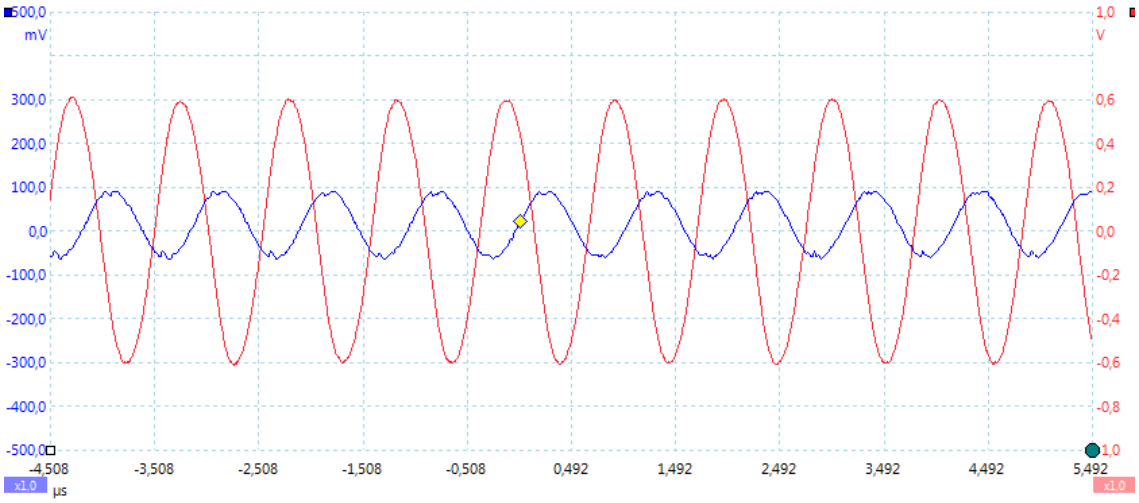

Figure 6-6: *VGA unit as 14 dB amplifier at 1 MHz.*

The 2 MHz input signal, in blue, at Figure 6-7 is 270 mV and the VGA unit's output voltage, in red, is about 600 mV, thus, by doing $20 * log_{10}\left(\frac{0.6}{0.27}\right)$ the applied gain is $6.94\ dB$, which is not the expected.

This deviation between the theoretical gain and the real gain is due to the attenuation curve of the VGA's inner circuitry and only has influence in signals above 1 MHz.

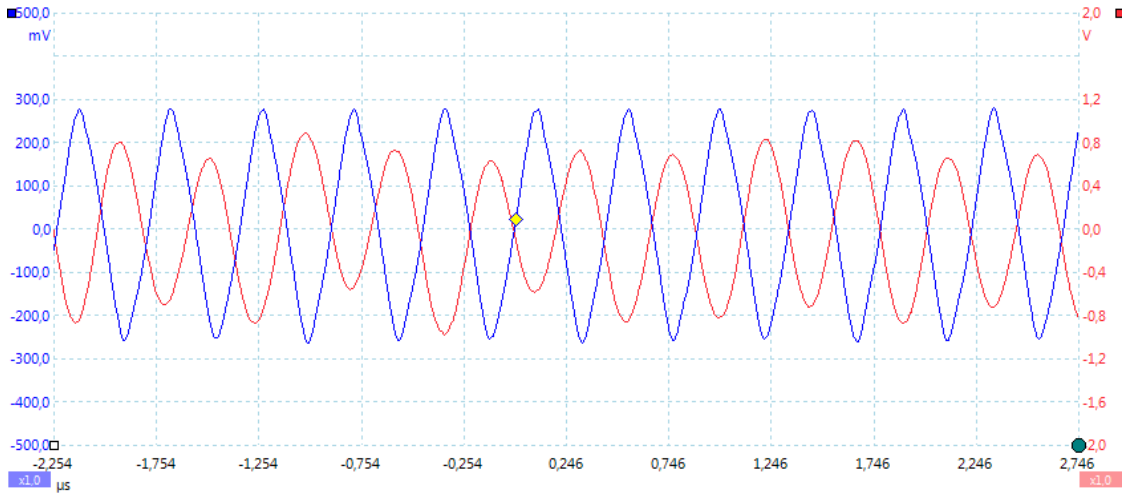

Figure 6-7: *VGA unit as 14 dB amplifier at 2 MHz.*

6.5.3 Large gain

To measure the VGA's capability to amplify very small signals, a small signal was applied to the input and the result was registered. Due to the fact that there wasn't any small signal generator available at the testing time, a resistive voltage divider was implemented to divide the signal generator's voltage, (blue graph in Figure 6-8) in 12000. This way, the input signal was $170\ mV\ /12000\ =\ 14\ \mu V$. Performing the gain calculation, $20 * log_{10}\left(\frac{1.4}{14E^{-6}}\right)$ the gain was $100\ dB$.

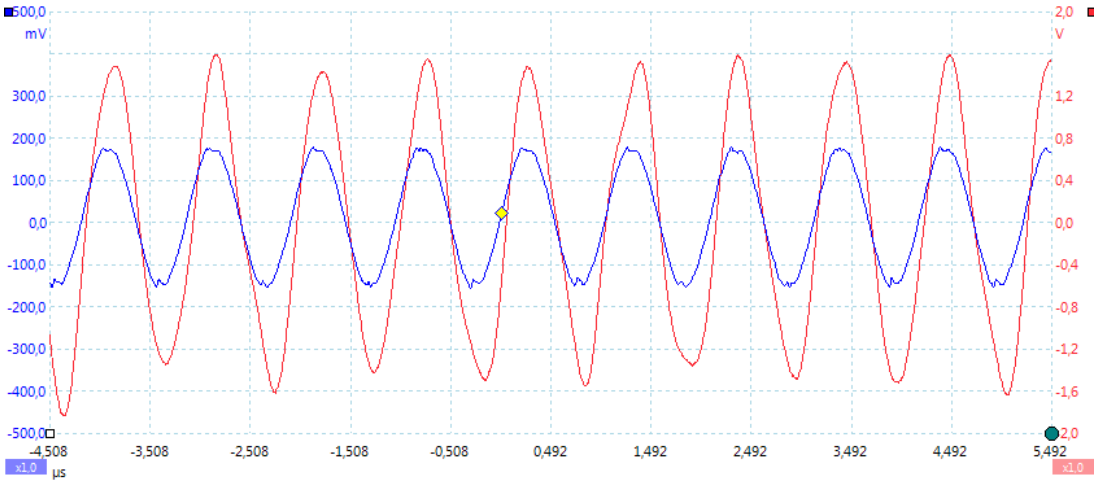

Figure 6-8: *VGA unit as 100 dB amplifier at 1 MHz.*

6.6 ADC results

Appling a signal to the ADC's input out of the acquisition range, blue in Figure 6-9, it triggers the ADC's OTR pin HIGH to indicate the event. In the same Figure it can be verified that the OTR signal indication, in red, is not symmetric. This fact indicates that the offset voltage of the antialiasing LPF has to be reduced.

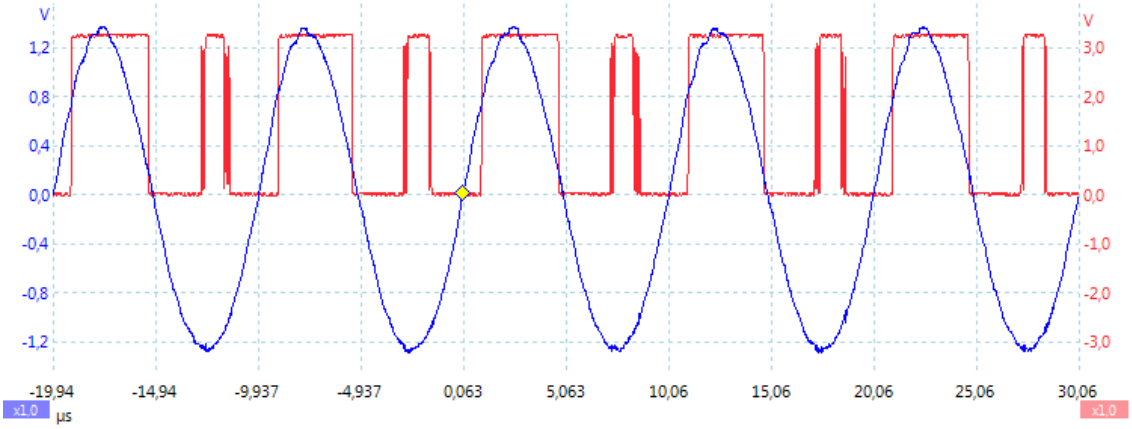

Figure 6-9: *ADC's OTR signal.*

6.7 Power amplifier results

Because the power amplifier receives more than 50 V from the 600 W Boost converter, special precautions are required before turn the circuit on [27]. This precautions range from the desk cleanness to the circuit handling and power up procedure.

Among the common hazards when working with power electronics the electrical shocks are the most dangerous because it can provoke immediate death, but nor the explosion of a component, nor a fire due to component overheating should be negated. Thus, placing the circuit inside a proper case and not touching it should be the first priority.

Figure 6-10 is the electrical caution signal and safety precautions should be taken when dealing with devices with it stamped on.

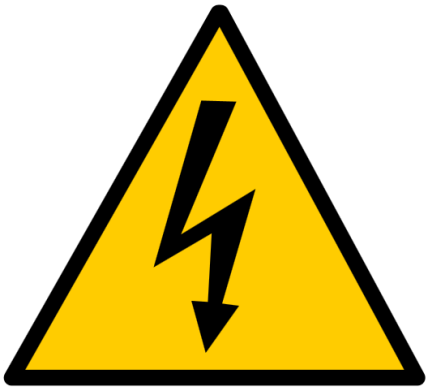

Figure 6-10: *Electrical safety sign.*

6.7.1 Recommended safety precautions

- Keep the work area neat and clean;
- Never work alone;
- Always wear safety glasses when working with the circuit at high power or high voltage;
- Included a switch in each supply circuit;
- Switches should be quickly accessible for emergency cases;
- Always include the proper fuse in the circuit;
- Be sure to be relaxed and lucid;
- Read the lab safety manual;
- In case of doubt, consult a specialist.

6.7.2 Power amplifier frequency response

Although the power amplifier was designed to source a maximum current of 7 A, for safety precautions mentioned above, tests were planned to sink a maximum of $\frac{30\ V}{16\ \Omega} = 1.875\ A$. Following those precautions, the power amplifier's fuse, which was planned to hold a 5 Amps fuse, was replaced for a 2 Amps and the power Boost converter was set to limit its maximum current to 1.9 A, before the fuse actuates.

To test the power amplifier it was decided to drive different resistive loads at different frequencies and measure the maximum output voltage and current. Tests were conducted using 100 Ω, 47 Ω, 31 Ω and 16 Ω resistive loads ate frequencies of 1 MHz and 2 MHz. Because all the results of the 100 Ω, 47 Ω, 31 Ω loads, at both frequencies, were equal to the 16 Ω at 1 MHz result (Figure 6-11), it was decided not to include them.

In Figure 6-11 and Figure 6-12, at blue, it can be seen the power amplifier's output voltage for a 16 Ω load. For protection of the oscilloscope, its probes were set to 10X attenuation, thus, to obtain the real output voltage, the values of the scale should be multiplied by 10. This way, the maximum output voltage for the 16 Ω load (and consequently for 100 Ω, 47 Ω and 31 Ω) was 33 V at 1 MHz, and 24 V for the 16 Ω at 2 MHz.

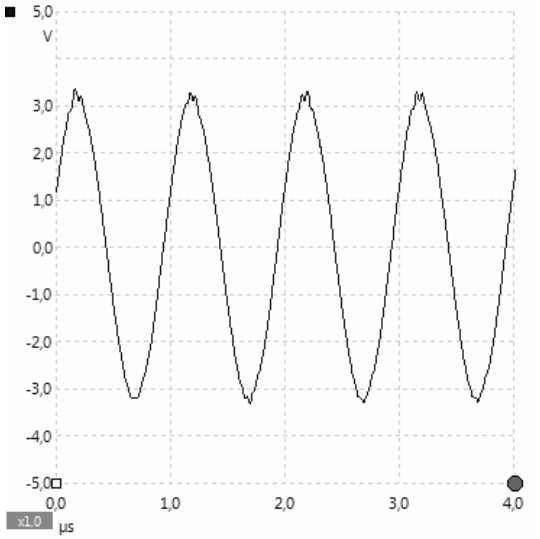

Figure 6-11: *Amplifier output voltage at 1 MHz.*

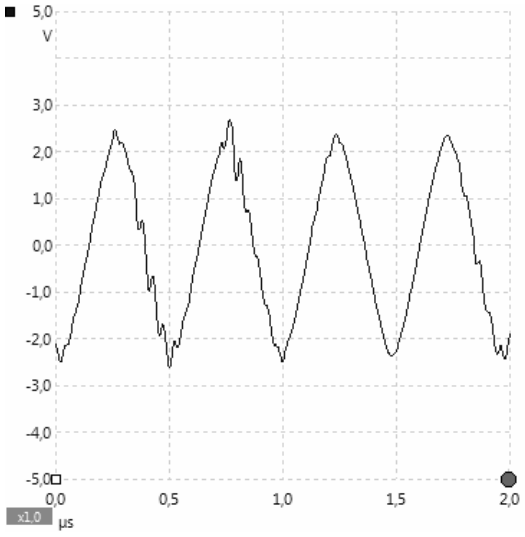

Figure 6-12: *Amplifier output voltage at 2 MHz.*

It should be stated that the decrease in the output voltage while the increasing of the frequency from 1 MHz to 2 MHz was due to the resistors parasitic capacitance, because the Boost's 1.9 A limiting circuit was activated. Making the calculation, $1.9 - \frac{24\ V}{16\ \Omega} = 0.4\ A$ it can be concluded that the extra 0.4 A are consumed in a parasitic component or in the operational amplifier based signal amplifier, the LM7171.

6.8 On the field results

To test the applicability of the system in real conditions, with an ultrasonic transducer, some tests were made in an aquarium, which intended to simulate the open sea.

This test consisted on the emission and acquisition of an ultrasound pulse with a PZT emitter (Figure 6-13) which has $6.58\ nF$ and an hydrophone.

Figure 6-13: *PZT 2 mm.*

The ultrasound pulse was a 6 cycle sine wave of 30 V applied to the PZT 2mm emitter. As it can be seen in Figure 6-14, despite the application of only 6 sine cycles to the emitter, far more collected by the hydrophone, as well as several echoes, which are the reflection of the acoustic wave by the glass of the aquarium walls.

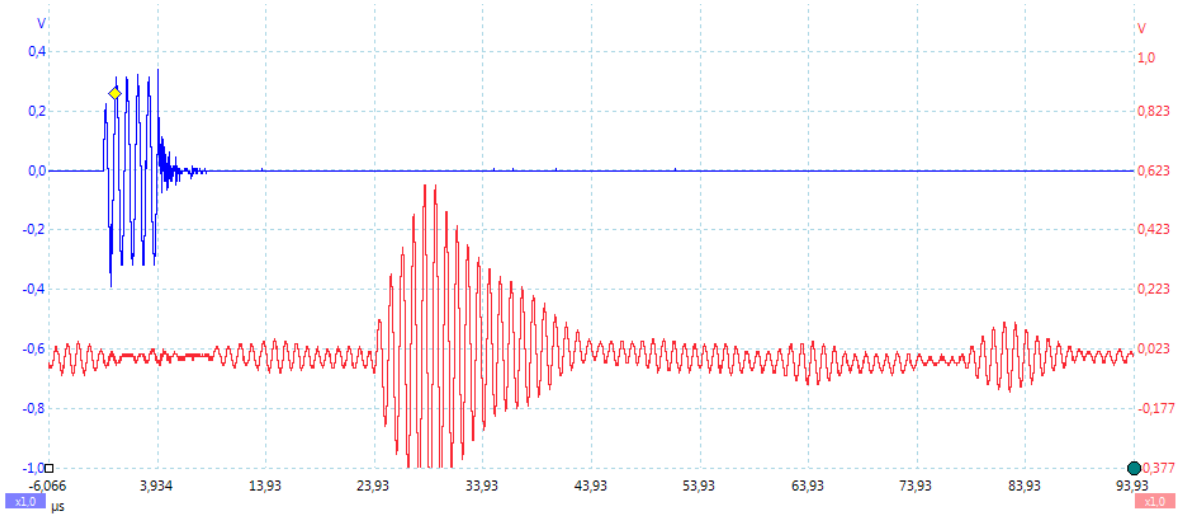

Figure 6-14: *Emitter 5 at 20 V 1 MHz pulse.*

To further understanding the harmonic content of the pulse generated by the hydrophone, it is suggested the reading of [11].

6.8.1 Power amplifier noise reduction

Despite the inclusion of a 10 A ferrite core common mode choke, to reduce differential noise in the power circuit, it was verified that the noise performance wasn't as expected (Figure 6-15).

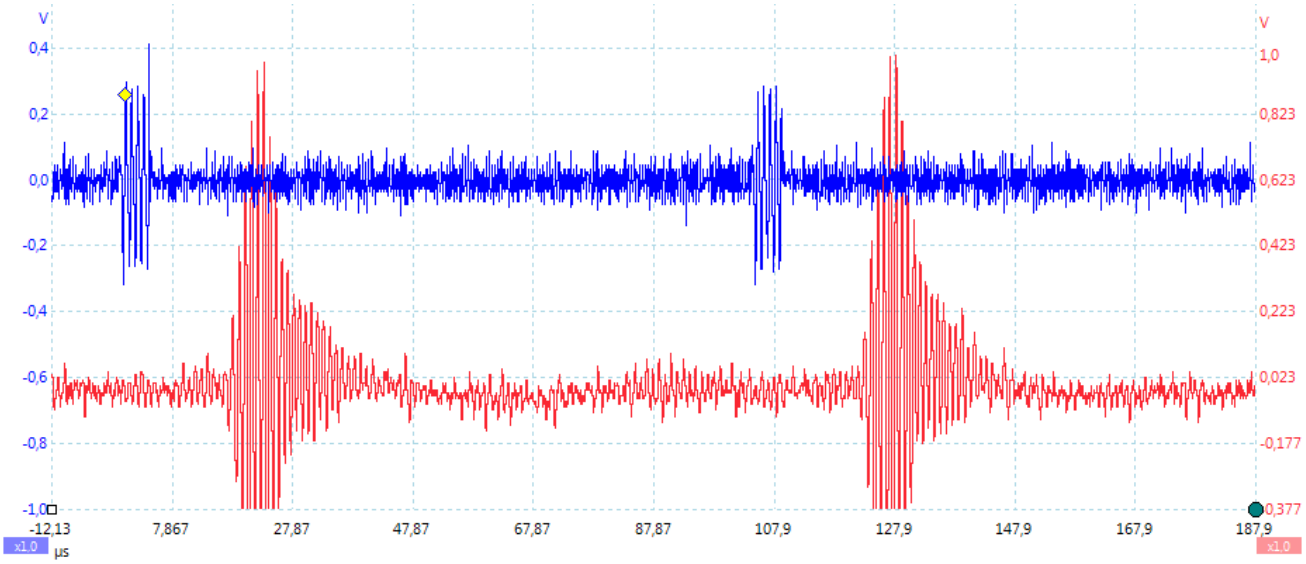

Figure 6-15: *Power supply noisy operation mode.*

Thus, a 5 Ω power resistor was tested in series with the Boost converter output, and the overall noise that propagates to the signal amplifier's output is substantially reduced, as it can be seen in Figure 6-16.

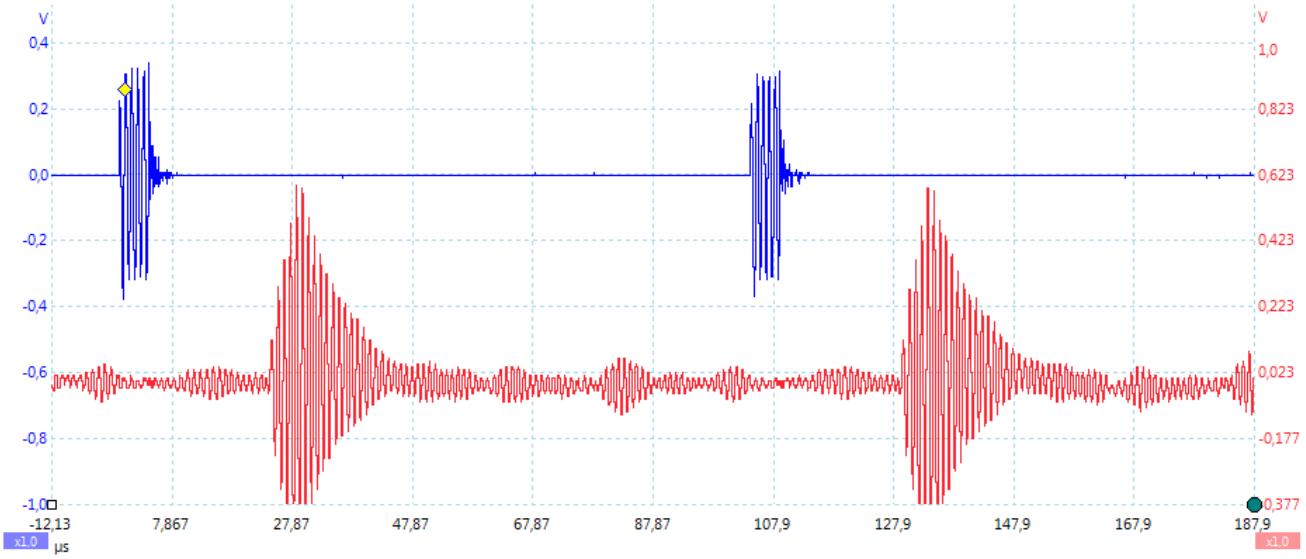

Figure 6-16: *Power supply silent mode.*

Chapter 7

7 Conclusions and future work

7.1 Conclusions

The objective of this project was to develop an electronic system capable of driving the piezoelectric ultrasound emitters developed by Marcos Silva Martins and acquire the signal of hydrophone.

Those transceivers had be driven by a power circuit that could generate sinusoidal signals of 30 Vpp at 4 MHz. The system had also to acquire acoustic signals using a hydrophone which generates a frequency between 100 kHz and 4 MHz with 11.2 V maximum amplitude.

To meet these goals it was necessary to do the following tasks:

- Research of the underwater acoustic communication systems state of the art, its technologies and transducers types;
- Research the important theoretical concepts, required to develop high frequency electronics, as well as the challenges faced when developing high speed mixed signal electronics, such as: power amplifiers, instrumentation and logic circuits;
- Design of a solution for the entire system;
- Implement a desktop application in Java, a microcontroller firmware in C, the logic programing in Matlab/Simulink, the signal amplification and the power electronics;
- Test the system for functionality and robustness and characterize it;
- Draw conclusions about the achieved results and pave the way for future works;

Underwater acoustic communications systems are used in a variety applications which range from military devices to medical imaging and industrial applications. Although its applications may vary, its working principle is almost the same. Some devices uses sound waves to navigate, detect objects on or under water, such as other submarines and fish, others, like the ultrasonic industrial emitters use them for cleaning, mix and mill in various chemical procedures.

The functional and non-functional requirements of the project were analyzed and the system was conceptually divided into three main parts, namely: an application layer, logic layer and hardware layer. The application layer performed the user interface. The logic layer was the interface between the application layer and the hardware layer.

The design of high speed mixed signal electronics posed particular challenges and major attention has to be paid issues such as clock signals, propagation delay crosstalk, sampling rates, component and PCB traces placement, differential signals, transmission lines, decoupling capacitors, power and ground planes, return currents and loop areas.

Before the implementation, several simulations were made with tools like, Multisim for instrumentation simulations, PSIM for power electronics simulation, FilterPro, from Texas instruments for filters and Matlab/Simulink for various simulations and calculus.

After simulations, the circuits were designed in Cadsoft Eagle software, to design the PCB's layout. A MinGW virtual machine was created to develop and run the java application and compile the firmware for the microcontroller using SDCC compiler. The FPGA logic system was developed with Xilinx System Generator, included in Matlab/Simulink. This tool reveled to be an extremely productive tool and easy to learn.

After the system development, it was extensively tested to verify its strengths and weaknesses. There were performed two types of tests. The first, was a test to verify the modular functionalities of the system and, the second, to verify the overall performance, from the user's point of view, Thus, the overall system, working as a single device, can provide an output signal of 3 A, 60 Vpp at 2 MHz, which is a very satisfactory result and is also able to receive a hydrophone signal as low as 14 μV, which is also a very good result.

7.2 Future works

The results achieved in this work are by far a success, but, it can yet be improved. Thus, some changes would be welcome. This way, several changes at different levels are suggested.

At application level

- Migrate the application from the MinGW to Windows

At the microcontroller level

- Configure the microcontroller to use the General Programmable Interface (GPI) instead of the IO Ports, to transfer data from the USB FIFOs to the FPGA. This method improves the transmission rate between the microcontroller and the FPGA because it provides a 16-bit bus at 48 MHz.

At the FPGA logic level

- Implement the modulator
- Implement the demodulator

Ate the signal generator level (DAC subsystem)

- Nothing to be done.

At the power emitter level

- Design a cylindrical shaped case to the power electronics, this can be done with 120 mm diameter metal plumbing pipe and two terminators properly isolated.
- Redesign the power board's layout to fit in the new case.
- Design an output impedance to match for each transducer to reduce the power consumption.

At the signal receiver level,

- Nothing to be done.

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