Design of a High-Performance Single-Phase Offline UPS with Reduced Switching Time

Delfim A. Pinto
Industrial Electronics Department
University of Minho
Guimarães, Portugal
a48394@alunos.uminho.pt

M. João Sepúlveda
Industrial Electronics Department
Algoritmi Research Centre
University of Minho
Guimarães, Portugal
mjs@dei.uminho.pt

***Abstract* — A high performance single phase offline UPS with reduced switching time is proposed in the present paper. The proposed UPS can protect loads from supply outage, overvoltage and undervoltage. A bidirectional DC-DC converter takes part of the presented model, in order to reduce the system size. Thus, the converter has the capability to charge the battery and to keep a regulated voltage for the inverter's DC-link. In order to provide a regulated output voltage for any type of load, a PWM (Pulse-Width Modulation) inverter with a multi-loop control strategy, using capacitor current as feedback variable, is also developed. By using the sliding window method, to detect long period voltage disturbances in real time, the switching time between mains and UPS can be significantly reduced. Moreover, simulation and practical results in different mains conditions are analyzed.**

***Keywords*– Uninterruptible Power Supply; Static UPS; Bidirectional DC-DC Converter; Sliding Window Technique.**

I. INTRODUCTION

Offline Uninterruptible Power Supply (UPS) are fairly used nowadays, mostly for low power and low cost applications [1]. This topology is able to protect loads from long period power disturbances, such as power failure, overvoltage, and undervoltage. This is explained by the switching time from the main supply that usually takes one quarter to half of a grid cycle, which makes this topology being recommended to protect less sensitive loads [2]. Such loads are mostly devices working with DC (Direct Current), i.e. personal computers, and for that reason it is common to find Offline UPS presenting a square or a semi-sinusoidal waveform output voltage. By doing this simple modification, companies can significantly reduce the equipment's cost once it simplifies the inverter module. Besides simplifying its involved control, it also reduces the concerns about the power semiconductors.

At a first glance, powering a DC device with a non-sinusoidal waveform seems to be a good practice, but in fact these devices are projected to work with a pure sinusoidal voltage. The actual power quality standards enforce loads connected to the grid to have a low THD (Total Harmonic Distortion) input current. Thus, recent DC devices on the market usually have any PFC (Power Factor Correction) circuit or some type of filter at its main entrance. The presence of such circuits reveals how important it is to maintain a stabilized sinusoidal supply voltage otherwise it may lead to device malfunction.

II. PROPOSED UPS CIRCUIT

The proposed Offline UPS is able to protect loads from power failure, overvoltage, and undervoltage. This model has two modes of operation – normal and backup. In normal mode, the voltage from the main supply is found regulated enough to directly power the loads while, in backup mode, when a long period disturbance affects the main supply, the UPS becomes the voltage source of the loads. The transitions between both modes of operation are carried out softly and synchronized, to reduce undesirable voltage transients. The switching time during power outages is fairly improved due the recurrence of sliding window technique to calculate in real time the voltage RMS (Root Mean Square) value. Another characteristic of this model is a pure sinusoidal output voltage, protecting different types of load rather than DC devices only.

The schematic of the proposed UPS is presented in Figure 1. It consists of a battery bank (E_{batt}), a bidirectional DC-DC converter (S_1 and S_2), an inverter (S_3 to S_6) and a static bypass switch (Q_1 and Q_2). As it is common in most UPS system, this model is supposed to use a lead-acid battery as the energy storage element. The bidirectional DC-DC converter is not new on the UPS systems and has been applied in [3]. In the proposed system, this module has the responsibility to deal with conversions of DC voltage levels between the battery and inverter. The single phase inverter generates the PWM (Pulse-Width Modulation) output voltage. Finally, the static bypass switch, when is active, connects the loads to the main supply.

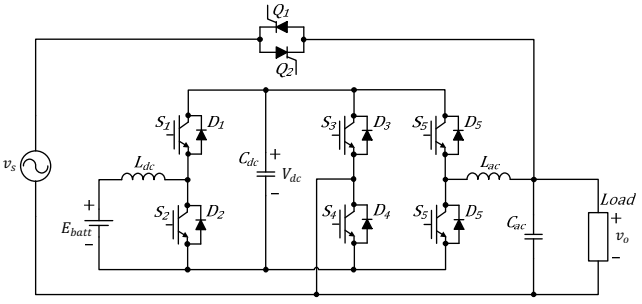

Figure 1. Schematic circuit of the proposed UPS.

For a better understanding of the UPS function, the two different modes of operation are explained next:

1) Normal Mode: The loads are powered by the main power supply (v_s) through the bypass switch ($Q_1$and Q_2) and the battery bank can be charged at this time. In case of charging, the inverter is used as a rectifier while the bidirectional DC-DC converter steps down the voltage from the C_{dc} capacitor to charge the battery bank. The UPS stays at this mode as long as the supply voltage remains in preset values.

2) Backup Mode: The energy comes from the battery bank and the bidirectional converter is controlled to work as a boost converter supplying the DC voltage needed by the inverter to feed the loads. The output filter, composed with L_o inductor and C_o capacitor, keeps a sinusoidal voltage over the loads, reducing the harmonics generated by the inverter's PWM commutation. This mode ends when the battery is completely discharged or the main supply is back again in required conditions.

III. System Description

A. Bidirectional DC-DC converter

In this UPS system the bidirectional DC-DC converter can either operate as a buck converter, charging the battery, or as a boost converter to feed the inverter's DC link. Therefore, the energy can flow in two opposite directions as it is showed in Figure 2.

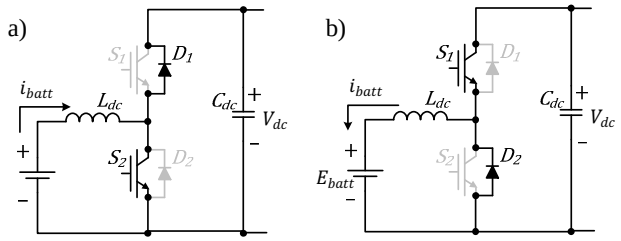

Figure 2. Bidireccional DC-DC converter modes: a) Boost converter mode; b) Battery Charger Mode

In the first case (Figure 2-a)), controlling S_2 switch with a constant duty cycle D, the L_{dc} inductor will store the current from the battery, during T_{on} period. For the release time T_{off}, the same current will follow the path through D_1 to be stored in C_{dc} capacitor. At a certain period of time, the capacitor voltage becomes higher than battery voltage, if a correct duty cycle is chosen. This configuration, known as boost converter, has the conversion ratio done by (1).

$$\frac{V_i}{V_o} = 1 - D, \qquad D = \frac{T_{on}}{T_{on}+T_{off}} \tag{1}$$

For the case presented in Figure 2-b), if a constant duty cycle control is applied on S_1 switch, a similar process will take place. Here, during T_{on} period, the current coming from C_{dc} capacitor will charge the battery and will be stored in L_{dc} inductor. But, during T_{off} period, only the current stored in the inductor will charge the battery, through D_2 diode. Thus, the output voltage expected will be smaller than V_{dc}, making this circuit known as buck converter. The conversion ratio can be obtained by (2).

$$\frac{V_i}{V_o} = D \tag{2}$$

As it can be concluded, this bidirectional configuration allows the reduction of passive components (capacitor and inductor) which would be needed for booth converters separately.

B. Inverter

The single phase PWM inverter of the proposed UPS system is presented in Figure 3. The two legs switches modulate the sinusoidal output voltage and a LC filter attenuates undesirable harmonics. Different methods to calculate the filter elements have been proposed. In this project, it will be used the method proposed by *A. David et al.*[4].

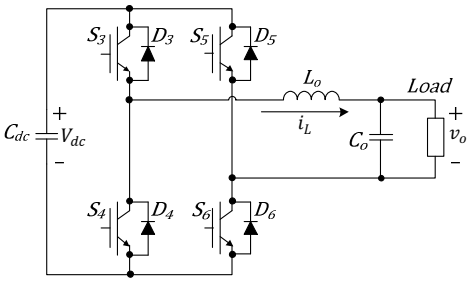

Figure 3. Inverter module circuit.

Initially it is calculated the inductor value using (3) which depends its maximum current ripple Δi_{Lmax}, input DC voltage V_{dc}, output peak voltage $V_{o_{peak}}$, and switching PWM frequency f_{sw}.

$$L_o = \frac{1}{2 \cdot f_{sw} \cdot \Delta i_{Lmax}} \left[\frac{(V_{dc} - V_{o_{peak}}) \cdot V_{o_{peak}})}{V_{dc}} \right] \tag{3}$$

Then the capacitor value is iteratively calculated using expressions (4), (5) and (6). The first condition asserts that the cut-off frequency of the filter (f_c) must be at least a decade below twice of switching frequency (f_{sw}). For the second condition it is necessary the switching frequency (f_{sw}) to be at least one decade above of the fundamental output frequency (f_o).

$$f_c = \frac{1}{2\pi\sqrt{L_o C_o}} \tag{4}$$

$$C_{o_{min1}} = \frac{\Delta i_{Lmax}}{16 \cdot f_{sw} \cdot \Delta v_{o_{max}}} \tag{5}$$

$$C_{o_{min2}} = \frac{100}{(2\pi f_o)^2 \cdot L_o} \tag{6}$$

IV. CONTROLLER DESIGN

A. Battery Charger/Boost Converter Control Strategy

The control strategy for the proposed converter is presented in Figure 4. It consists in a closed-loop control system with a PI compensator to maintain the output voltage regulated. The control can be applied for both boost converter mode and battery charger mode. The $G(s)$ represents the transfer function of the circuit in Laplace domain.

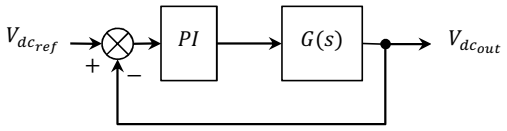

Figure 4. Control strategy applied to the bidirectional DC-DC converter.

B. Inverter Control Strategy

To control the inverter module different approaches must be considered. Figure 5 shows a diagram of the developed model. For synchronized transitions between main supply and UPS a PLL (Phase-Locked Loop) circuit was add to generate the reference ($v_{o_{ref}}$) of the inverter control. Also, a disturbance detection block was introduced to enable the comparator PWM generator.

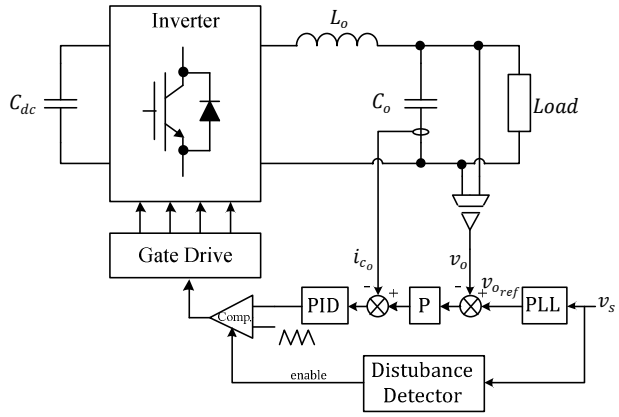

Figure 5. Inverter control strategy.

In order to supply the loads with low THD voltage, the inverter is controlled with a multi-loop control system. The robustness of this control strategy has been proved in [5] and [7] and it is characterized by using, in the internal loop, the current of one of the output filter elements. For this case it was chosen capacitor current since it is the element that filters the output voltage. Also, it was applied a PID (Proportional, Integral and Derivative) compensator at this subsystem for a better response while, on the outside loop, a single Proportional compensator was added to generate the capacitor current reference.

To detect long period voltage disturbances on the main supply is proposed RMS value calculation using sliding window technique. This technique is implemented in discrete-time domain by sampling the voltage and storing samples in an array until it gets full. The value is then determined by using (7). After that, for each new acquired sample the RMS value is recalculated, giving its variation in real time [8]. Figure 6 shows a representation of this procedure.

$$V_{RMS} = \sqrt{\frac{1}{N}\sum_{n=0}^{N-1} V_s[n]^2} \tag{7}$$

For a faster response, the RMS value is calculated for a half wave, since this value is the same as for a full sinusoidal wave. If the calculated voltage crosses the preset upper or lower boundaries it is considered that a disturbance is affecting the main supply and an enable signal activates the comparator and the inverter begins feeding the loads.

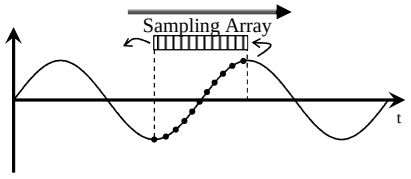

Figure 6. Representative schematic of sliding window technique used to calculate the RMS value.

V. SIMULATION RESULTS

Computer simulations were carried out using PSIM software in order to verify the proposed UPS system response. Defined parameters during simulations are described in Table I.

TABLE I. DEFINED UPS PARAMETERS USED DURING SIMULATIONS RESULTS

Parameter	Value
AC Supply Voltage (v_s)	115 Vrms (50 Hz)
Battery Bank Voltage (E_{batt})	96 V
DC Link Voltage (V_{dc})	200 V
Switching Frequencies (f_{sw})	20 kHz
Output Inductor (L_o)	220 µH
Output Capacitor (C_o)	10 µF
DC Link Capacitor (C_{dc})	500 µF
DC Link Inductor (L_{dc})	330 µH

In the first case it was tried out a transition from normal mode to backup mode during a power outage in the presence of a diode rectifier as the nonlinear load. Simulation results can be visualized in Figure 7. To get the maximum delay time of UPS entrance, the outage occurs at zero voltage point which is the worst case for the sliding window RMS calculation. This happens because the next lower voltage values acquired affect less the RMS equation and the disturbance detection will take a longer time. As shown in Figure 7, the main supply fails at 80 ms and the UPS begins feeding the load after 3,4 ms which is less than a quarter of the grid cycle. If the supply fail happened at the peak of the voltage the UPS response could be even faster. In the same figure can also be seen that the inverter control has a good response supplying nonlinear loads.

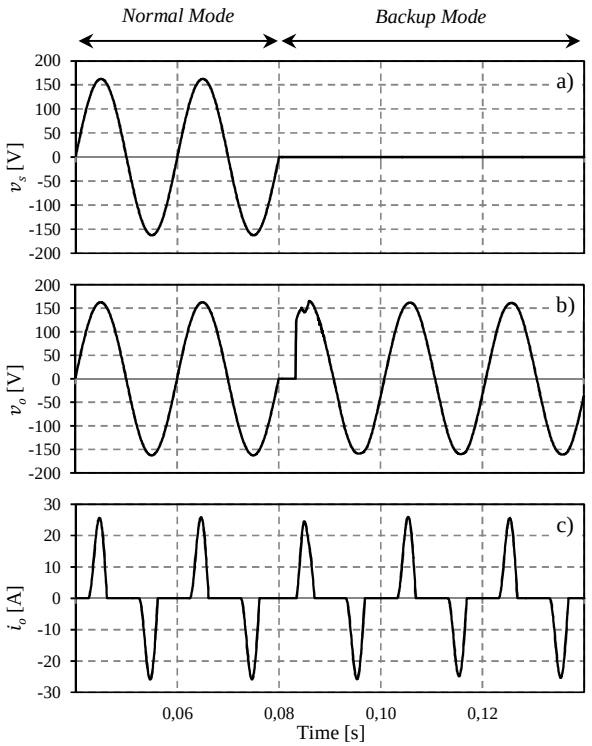

Figure 7. Simulation results in the presence of a nonlinear load during a power outage at 80ms: a) Main supply voltage (v_s);b) Load voltage (v_o); c) Load current (i_o).

Figure 8 presents the simulation results in occurrence of an overvoltage. The event occurs at 80 ms and the UPS detects it around 4 ms after. The transition only happens at zero voltage crossing due the uncontrolled turn-off characteristic of the thyristorized switch.

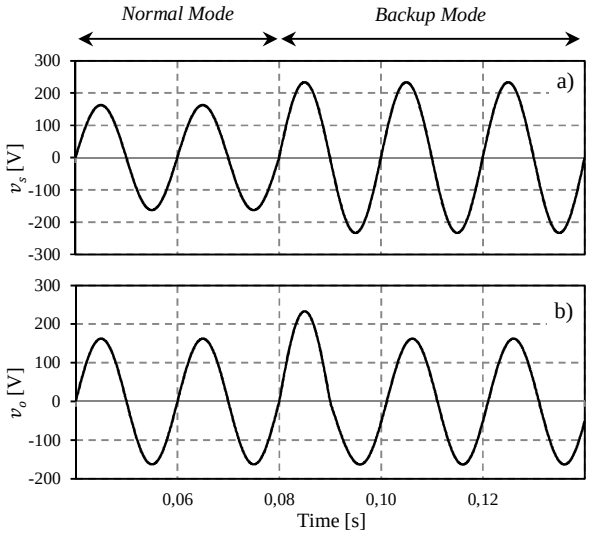

Figure 8. Simulation results during an overvoltage occurrence at 80 ms: a) Main supply voltage (v_s); b) Load Voltage (v_o).

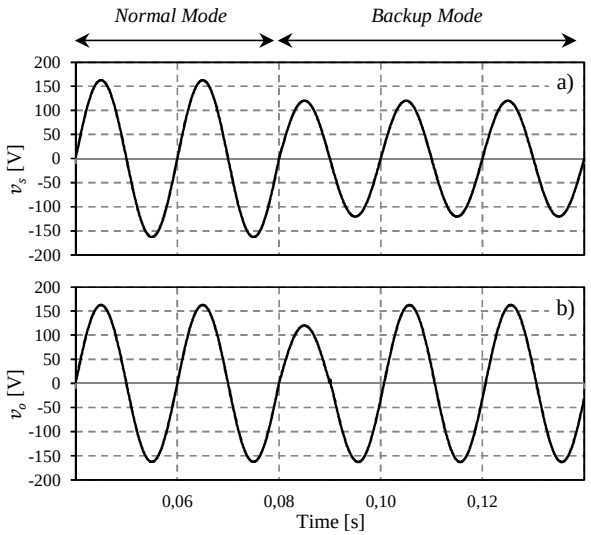

Figure 9. Simulation results during an undervoltage occurrence at 80 ms: a) Main supply voltage (v_s); b) Load Voltage (v_o).

Similar simulation was carried out in the occurrence of undervoltage event. Results are illustrated in Figure 9. It can be seen that the system takes the same actuation time for the same reason of the previous simulation.

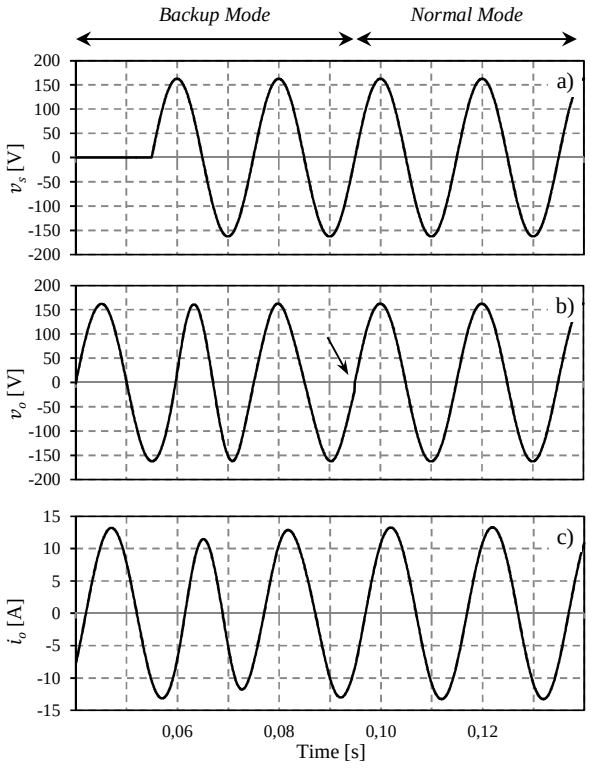

Figure 10. Simulation results in the presence of a RL load during the return of main supply at 55 ms: a) Main supply voltage (v_s); b) Load voltage (v_o); Load current (i_o).

Finally, simulations were performed in order to analyze the transition from backup to normal modes of operation, meaning the return of the main supply (v_s) to its nominal values. Figure 10 presents the obtained results. Looking to Figure 10-b), the UPS inverter is normally powering a RL load until the mains return at 55 ms, 90º ahead of the load voltage phase. From that moment, the PLL initiates synchronization and takes about two cycles (at 85 ms) to load voltage get in phase with mains. In the developed algorithm the switching process only happens after synchronization is achieved and for the next voltage zero-crossing point. The transition point is displayed by an arrow mark in the same figure.

VI. Experimental Results

For the UPS discussed so far, part of its system has been implemented in laboratory, in order to prove its reliability to protect the loads. Thus, it has been built an inverter prototype, since it is the module responsible to directly supply the loads. The applied control at this part was a single loop system with a proportional compensator. A static bypass switch, composed with a Triac semiconductor, was also added to the module to allow the transitions between both UPS modes of operation. The main control of this simple configuration was implemented in a dsPIC30f2010 microcontroller (Microchip). The load type, used in the following results, was a resistive one. In Table II can be found listed all the parameters and elements used in the developed prototype.

TABLE II. Defined UPS parameters used during experimental results

Parameter	Value
AC Supply Voltage (v_s)	24 Vrms (50 Hz)
DC Link Voltage (V_{dc})	60 V
Switching Frequencies (f_{sw})	20 kHz
Output Inductor (L_o)	220 µH
Output Capacitor (C_o)	10 uF
Mosfet	BUK453-100B
Thysristor	BT152-400R

Figure 11 presents the experimental results during a power outage occurrence. As it can be seen, the applied control takes about 2,5 ms for disturbance detection and inverter initialization. It can also be noticed that when the inverter begins to supply the load, it is done completely synchronized, as a consequence of the applied PLL.

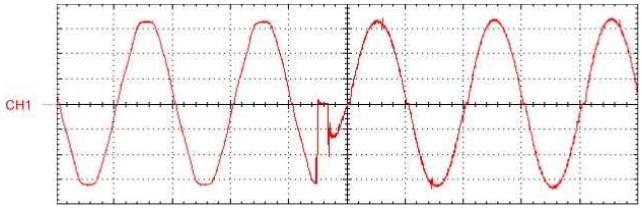

Figure 11. Experimental results of the load voltage under a power outage. (10ms/Div – 10V/Div)

Similar to the previous simulations, an undervoltage disturbance was under experiment at this time. The results can be found in Figure 12, where CH1 and CH2 are the load and mains voltages, respectively. Taking a look to the mains voltage (CH2), it suffers a gradual decrease on its amplitude value over time. In CH1, it can be visualized that the load supply initially comes directly from the mains. Right after the control detects that this voltage is above the preset required value, the inverter is enabled, but only starts after the next zero crossing point, when the Triacs turned off. In this case, the UPS commutes from normal to backup operation mode. The precise instant of the switching action is signed with an arrow mark on CH1 waveform, where can be noticed a small transient. Analogous results were obtained during experimental of overvoltage disturbance.

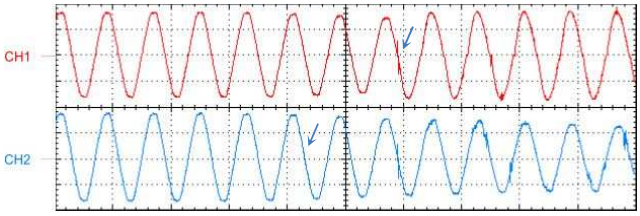

Figure 12. Experimental results during an overvoltage, with CH1 the load voltage and CH2 the mains voltage. The arrow mark indicates the switching occurrence. (25ms/Div – 20V/Div).

The last experiment, showed in Figure 13, was carried out in order to prove the UPS transition between backup to normal operation mode. From the same figure, CH1 and CH2 represent both load and mains voltage, respectively. In CH1, the inverter is feeding the load while the mainsvoltage is out of service. When the mains voltage returns (90º delayed), the PLL's inverter is initialized to get the synchronization after three grid cycles. On the developed algorithm, the load is then released to the mains supply on the fifth cycle and on zero crossing point for safety reasons (arrow mark). It can be notice the interference on the mains voltage (CH2), caused by the inverter switching frequency before being disabled.

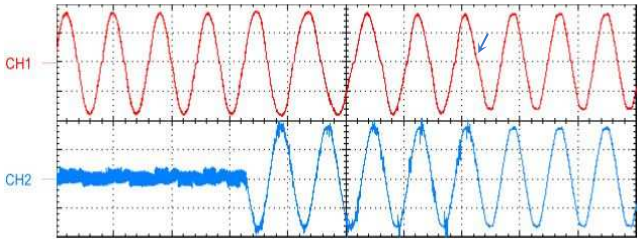

Figure 13. Experimental results duringthe return of the mains, with CH1 the load voltage and CH2 the mains voltage. The arrow mark indicates the switching occurrence. (25 ms/Div – 20V/Div)

Conclusion

A high performance Offline UPS with reduced switching time has been proposed. The inverter control strategy during simulations has shown an improved steady-state response even in presence of nonlinear loads. A reduced switching time was achieved by using the sliding window RMS calculation to detect disturbances on the main supply. The bidirectional DC-DC converter has also shown to be a good compromise in order

to reduce the system size. Furthermore, a simplified prototype of the UPS's inverter has been built in order to get experimental results of the system capability to protect loads.

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