Comparisons between Synchronizing Circuits to Control Algorithms for Single-Phase Active Converters

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Abstract – This paper presents a comparative analysis between synchronizing circuits applied to control algorithms for single-phase active converters. One of these synchronizing circuits corresponds to the single-phase PLL (Phase Locked Loop), implemented in α-β coordinates, whereas the other one corresponds to the E-PLL (Enhanced PLL). These synchronizing circuits are compared in several aspects as processing and settling time and memory space requirements. Moreover, the performance of a single-phase back-to-back converter is also presented, with its control algorithm based on these Synchronizing Circuits. Each one of the control algorithms were implemented in a DSP microprocessor TMS320F2812F from Texas Instruments. Simulation and experimental results, through a back-to-back converter prototype, are presented.

I. INTRODUCTION

The proliferation of nonlinear loads in residences, offices and industries has contributed to increase the harmonic pollution observed in the power grid. Moreover, the harmonic current-components consumed by these nonlinear loads result in harmonic voltage-drop on the supply line impedances, which deteriorates the waveform of the voltages delivered to the load [1]. There are also other events as voltage sags or voltage swells that are resulted, respectively, from connection or disconnection of large loads [2] [3]. All of these events are the most responsible ones for the observed problems in sensitive loads as improperly shut down, reduced lifetime, malfunction, and so others.

Power quality problems can be overcome, in real time, through the utilization of “Custom Power” devices. In this paper a back-to-back converter is used, which is composed by two power converters that are connected in series and in shunt with the power grid. The shunt converter consists in an active rectifier that injects or absorbs energy from the power grid, in order to keep the dc-link voltage regulated. The series converter is responsible to compensate the major power quality problems related with the system voltages, such that the voltage delivered to the load remain regulated and with low harmonic distortion.

To control these converters, control algorithms based on the instantaneous power theory (p – q Theory) are applied [4] together with a synchronizing circuit. The synchronizing circuit is responsible to produce, in real time, sinusoids that are synchronized with the fundamental component of the system voltage. Thus it can be observed its importance, since the voltage produced by the series converter depends, directly, on the generated sinusoid by the synchronizing circuit.

Due to the importance of the synchronizing circuit, this paper investigates two different topologies. The first one corresponds to the single-phase PLL (Phase - Locked - Loop) [4] [5] [6] [7] [8], implemented in α-β coordinates, whereas the other one corresponds to the E-PLL (Enhanced PLL) [9] [10] [11].

The comparison involving these PLL topologies is focused in processing and settling time and memory space requirements. Both controllers where implemented in a DSP microprocessor TMS320F2812F from Texas Instruments. Being a real time processing system, computing speed and memory usage, as well as the settling time are important issues. These characteristics must be enhanced; moreover, they must provide compensated voltages that comprises with the power quality standards [12]. Simulation and experimental results, through a back-to-back converter prototype, are presented.

II. HARDWARE CONFIGURATION

As aforementioned in this paper and indicated in Fig. 1, the back-to-back converter is composed by two power converters that are connected in series and in shunt with the power grid. A step-down transformer (5 kVA – 230 V//115 V) is used to provide galvanic isolation between the power converters and the power grid. Another step-down transformer, with the same characteristics, is used to connect the shunt converter with the power grid. The series converter is directly connected with the power grid.

Each one of the single-phase power converters is composed by two branches (4 IGBTs with anti-parallel diodes) from model Semikron SKM-50GB063D [13]. The IGBTs of this power module present as main features a collector-emitter voltage of 600 V and a collector current of 50 A (peak value).

The dc-link is composed by three 4700 μF capacitors connected in series, which corresponds to an equivalent capacitance of, approximately, 1566.67 μF. Each one of these capacitors presents a dc-voltage rating of 450 V.

The RLC coupling filter of the series converter is composed by a 15 Ω resistor (Rc), an 8.8 μF capacitor (Cp), and an air-core inductor of 0.6 mH (Lc). The RLC filter of the
The shunt converter is comprised of a 0.6 mH inductor ($L_{fp}$), an 4 $\Omega$ resistor ($R_{fp}$), and an 2.2 $\mu$F capacitor ($C_{fs}$).

The nonlinear load consists of a single-phase diode rectifier, with a RC Load on the dc-side ($C_{DC} = 4.7$ mF and $R_{DC} = 25$ $\Omega$). To smooth the current waveform, it is used a 3 mH inductor ($L_1$). There is also a linear load, connected in shunt with the nonlinear load, composed by a 30$\Omega$ resistor ($R_1$) and a 650 $\mu$H inductor ($L_2$).

A diode rectifier, similar to the nonlinear load, is used to increase the harmonic distortion of the supply voltage. This rectifier is located between the transformer, connected in series with the power grid, and the series converter.

A soft-start circuit was implemented to suppress the lack of electric isolation of a coupling transformer that is present in the majority of series converters [13]. It also acts as a protection system to overloads and short-circuits. Moreover, contactors are employed to connect the shunt ($C_3$) and series ($C_4, C_5, C_6$) power converters, as well as to connect the loads with the electrical system ($C_1, C_2$).

The supply voltage is represented in Fig. 1 as being $v_S$, and the load voltage is $v_L$. The produced voltage by the series converter is represented as $v_{comp}$. The load and source currents are represented as $i_L$ and $i_S$, respectively. The controlled current ($i_{ref}$) is produced by the shunt converter in order to regulate the DC link voltage.

### III. CONTROLLER OF THE BACK-TO-BACK CONVERTER

As introduced in section I the controller of the back-to-back converter is constituted by control algorithms to determine the reference signals to be produced by the power converters, plus switching algorithms to command the IGBTs. The control algorithms to determine the reference signals are comprised by a synchronizing circuit, an algorithm to determine the compensating currents and an algorithm to determine the compensating voltages. In Fig. 2 is shown a block diagram that represents the control algorithms to determine the reference signals. The control algorithms denominated in Fig. 2 as “Current-Reference Algorithm” and “Voltage-Reference Algorithm” are based on the concepts involving the instantaneous power theory ($p – q$ Theory) with some simplifications. Hereafter, these control algorithms are described, and, in sequence, the investigated synchronizing circuits are introduced.

#### A. Current-Reference Algorithm

Since there are no power sources on the dc side of the power converter, a controller that keeps the dc-link voltage regulated has to be implemented. It is worth to notice that, with only this control algorithm, the shunt converter does not provide active filtering. In this case, the shunt converter can be considered as an active rectifier. Based on the dc-link voltage ($v_{DC}$), the control signal $p_{ref}$ is determined as described as follows:

$$
 p_{ref} = (v_{Ref} - v_{DC}) \cdot \left( \frac{k_p}{s} + \frac{k_i}{s} \right).
$$

The control signal $p_{ref}$ can be understood as an amount of energy, per time unit, that is drained or injected by the shunt converter in order to keep the dc-link voltage regulated. As indicated in (1), the control signal $v_{ref}$ corresponds to the...
reference value of the dc-link voltage, and the control signals 
\( p \) and \( q \) represent, respectively, to the proportional and
integral gains of the PI-Controller.

In sequence, the mathematical methodology to determine
the reference signal \( I_{ref} \) is described. Since this algorithm is
based on the \( p-q \) Theory, consider that is necessary to
determine the reference signals in \( \alpha\beta \) coordinates \((i_{ref} \alpha, i_{ref} \beta)\)
as described as follows:

\[
\begin{bmatrix}
i_{ref} \alpha \\
i_{ref} \beta
\end{bmatrix} = \frac{1}{p_{ref}^2 + p_{ref}^2} \begin{bmatrix} p_{ll}^\alpha & p_{ll}^\beta \\ p_{ll}^\beta & -p_{ll}^\alpha \end{bmatrix} \begin{bmatrix} p_{re} \\
0
\end{bmatrix} ,
\]

(2)

where, the signals \( p_{ll}^\alpha \) and \( p_{ll}^\beta \) are generated by the
synchronizing circuit. For now, it is assumed that these
signals are sinusoidal waveforms, with unitary amplitude, and
are in phase with the fundamental frequency of the control
signals \( v_{ref} \) and \( v_{ref} \), respectively. After some simplifications in
equation (2), \( i_{ref} \alpha \) and \( i_{ref} \beta \) are given by:

\[
\begin{align*}
i_{ref} \alpha &= \frac{p_{ll}^\alpha \cdot p_{re}}{p_{ll}^\alpha + p_{ll}^\beta} = p_{ll}^\alpha \cdot p_{re} \\
i_{ref} \beta &= \frac{p_{ll}^\beta \cdot p_{re}}{p_{ll}^\alpha + p_{ll}^\beta} = p_{ll}^\beta \cdot p_{re} 
\end{align*}
\]

(3)

Indeed, since the control signals \( p_{ll}^\alpha \) and \( p_{ll}^\beta \) are sinusoids
with unitary amplitude and \( p_{ll}^\alpha \) leads \( 0 \) \( p_{ll}^\beta \), it can be
assumed that the sum of their square values is equal to one.

Based on the Clarke Transformation [13] [14] and
assuming a "fictitious" three-phase three-wire system, the
control signal \( i_{ref} \) is given by:

\[
\begin{bmatrix}
i_{ref} \alpha \\
i_{ref} \beta \\
0
\end{bmatrix} = \frac{2}{\sqrt{3}} \begin{bmatrix} 1 & 0 \\
-1/2 & \sqrt{3}/2 \\
-1/2 & -\sqrt{3}/2
\end{bmatrix} \begin{bmatrix} i_{ref} \alpha \\
i_{ref} \beta \\
0
\end{bmatrix} .
\]

(4)

As it can be observed in (4), \( i_{ref} \) is only associated with
\( i_{ref} \). Combining (3) and (4) the reference signal \( i_{ref} \) can be
determined in a very simple way as described as follows:

\[
i_{ref} = \frac{2}{\sqrt{3}} \cdot p_{ll}^\alpha \cdot p_{re} .
\]

(5)

Based on the aforementioned e planation, it can be noted that
the computational effort to determine \( i_{ref} \) is directly
related with the synchronizing circuit and with the PI-
Controller. In sequence, the control algorithm that determines
the reference voltage \( v_{ref} \) is described.

\text{olt ge-Reference Algorithm}

As illustrated in Fig. 3, this algorithm presents as inputs the
signals derived from the source current \((i_s)\) in \( \alpha\beta \) coordinates
\((i_{sa}, i_{sb})\), the control signal obtained from the system
voltage\((v_{ref})\), plus the signals generated by the synchronizing
circuit \((p_{ll}^\alpha, p_{ll}^\beta)\). In this algorithm there is also a control
block that determines control voltages with the objective to
damp resonance phenomena, denominated as “Damping

Algorithm” block. Indeed, as described in [6], instability
problems due to the resonance phenomena, involving the
passive filters and the system impedance, may occur. In order
to enhance the overall system stability, an auxiliary algorithm
can be added to the controller of the series converter. In
sequence, it is described a mathematical methodology, based
on the \( p-q \) Theory, to determine the control signal \( v_{sa} \).

In a similar way of the presented one in (4) the control
signals \( i_{sa} \) and \( v_{sa} \) are determined, respectively, from the
source current \( i_s \) and system voltage \( v_s \) as described as follows:

\[
i_a = \frac{3}{\sqrt{2}} \cdot i \\
v_a = \frac{3}{\sqrt{2}} \cdot v
\]

(6)

The signal \( i_b \) is shifted by \( 0 \) from \( i_s \). The control signals
\( i_s \), \( i_b \), \( v_s \), and \( v_a \) together with to the ones generated by the
synchronizing circuit \((p_{ll}^\alpha, p_{ll}^\beta)\) are applied to calculate the
real and imaginary powers as described as follows:

\[
\begin{bmatrix}
p \\
q
\end{bmatrix} = \begin{bmatrix} p_{ll}^\alpha & p_{ll}^\beta \\ p_{ll}^\beta & -p_{ll}^\alpha 
\end{bmatrix} \begin{bmatrix} i_a \\
i_b
\end{bmatrix} .
\]

(7)

In sequence, the control signal \( i_a \) is determined according
to the following equation:

\[
\begin{bmatrix}
i_{sa} \\
i_{sb}
\end{bmatrix} = \frac{1}{p_{ll}^\alpha + p_{ll}^\beta} \begin{bmatrix} p_{ll}^\alpha & p_{ll}^\beta \\ p_{ll}^\beta & -p_{ll}^\alpha 
\end{bmatrix} \begin{bmatrix} p \\
q
\end{bmatrix} ,
\]

(8)

where, the powers \( p \) and \( q \) corresponds to the oscillating
components of the real \( p \) and imaginary \( q \) powers, and
they can be obtained through high-pass filters. The direct
product involving the control signal \( i_s \) by a gain
denominated as results in the harmonic controlled-voltage
\( v_s \). The gain can be understood as a resistance only for
the harmonic components. Further details involving the
damping algorithm are described in [14].

Finally, the reference voltage \( v_{ref} \) is determined as
indicated in Fig. 3. hen \( v_{ref} \) is produced by the series
converter, it is expected that power quality problems

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C. Single-Phase Phase-Locked-Loop (Single-Phase PLL)

his single-phase PLL circuit is similar to the one imlemented to three-phase systems with some simlifications as introcie in . n Fig. is illstrate the tracking of the int signal which one is comrehense by its oscillating in its oscillating comonent.

As inicate in Fig. the feeback signals \( p_{\text{ll,}} \) an \( p_{\text{ll,}} \) are bilt b the circit st sing the time integral of \( \omega t ) \) - ontroller. hese feeback signals ha e nit am lit it e an \( p_{\text{ll,}} \) a\( p_{\text{ll,}} \) he circit becomes stable onl if the a erage comonent of the fictitio s imaginari oer reaches ero al e \( q' = 0 \) an has minimi lo -fre enc oscillating com ontent \( q' \). nce the circit is stabili e the a erage al e of \( q' \) is ero an ith this the hase angle of the n amental fre enc is reache . At this conition the feeback signal \( p_{\text{ll,}} \) becomes in hase ith the n amental com ontent of the control signal \( v_{\text{ref}} \). Futher elanations in ol ing this for three-phase systems are resente in 

ereafter it follo s some sim lation res its relate ith the single-phase, nitiall in this case test the in t signal corres on s to \( v_{\text{ref}} = 100 \sin(\omega t + 45^\circ) \). T at \( t = 2.0 \) s the hase angle of the int signal is mo ifie s ch that the mo ifie in t signal corres on s to \( v_{\text{ref}} = 100 \sin(\omega t + 90^\circ) \).

n Fig. is sho n the erformance of the single-phase tracking the in t signal \( v_{\text{ref}} = 100 \sin(\omega t + 45^\circ) \). he starts at \( t = 0.1 \) s. fter c les the control signal \( p_{\text{ll,}} \) tracks the in t signal \( v_{\text{ref}} \).

Fig. illstre the control signal \( p_{\text{ll,}} \) tracking the in t signal \( v_{\text{ref}} \) at the transient \( t = 2.0 \) s hen the hase angle of the in t signal \( \phi_{\text{ref}} \) is increase from to . s it ca be seen in Fig. at \( t = 2.07 \) s the control signal \( p_{\text{ll,}} \) tracks again the in t signal \( v_{\text{ref}} \).

as e on these relliminar sim lation res its it ca be note the feasibilit of this single-phase circuit. n can also be seen in literate re the erformance of this er orse conitions than the resentate ones in this a er.

D. Single-Phase Enhanced PLL

n Fig. the roose algorithm is sho n as a block inagram of the nance . riginnl the com rises a control loo to determine the am lit e anothor control loo that e tracts the fre enc an hase angle of the in t signal. herefore ifferent from the the - reall ermines the n amental com ontent of the in t signal hich one is com rehen e e b its am lit e fre enc an hase angle.

nfort natel it is esire that the generate signals b the single-phase enhance PLL can not be irectl se . n Fig. the single-phase estimate the error signal e corres on s to the total bstance bet een the in t signal \( v_{\text{ref}} \) an the generate one b the 

\[ E_{\text{ PLL,}} \]

he feeback signals \( \cos(\omega t) \) an \( \sin(\omega t) \) are
b l t s ing the time integral of ε t t ω of the
controller, he circ it becomes stable onl if the
average component of the error signal
reaches ero ale.
nce this circ it is stabilie the control signal
EPLL tracks
the int signal vS
as a conse ence the hase angle of
the fnamental fre enc is reache. Frther elanations
in ol ing the are resente in . n Fig. an
Fig. are resente the simlation reslts ith the same test
cases a lie to the single- hase .

V.
A

he s nchroni ng circ its ere imemente on the e as
meths 3 F D micro roessor. For
memor re irements assessement aribles si e as
meas re. n able the aribles n mber an si e are
sho n an total memor s ace eman e for each
s nchroni ng circ it is calc late .

<table>
<thead>
<tr>
<th>Type</th>
<th>Memory Space</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Single-Phase PLL</td>
</tr>
<tr>
<td>double</td>
<td>(4 x 32) 128 bits</td>
</tr>
<tr>
<td>long int</td>
<td>(14 x 32) 448 bits</td>
</tr>
<tr>
<td>long int array</td>
<td>(640 x 32) 20480 bits</td>
</tr>
<tr>
<td>TOTAL</td>
<td>21096 bits</td>
</tr>
</tbody>
</table>

The system voltage is sampled 640 times each grid period.
These instantaneous values are stored in a 640 position array,
which is used to create the 90º shifted signal used in the
Single-Phase PLL. This causes the Single-Phase PLL
memory requirements to be wider than the EPLL. Given the
vast amount of memory available in the selected
microprocessor, this matter has a small importance.

The processing speed of each synchronizing circuits was
also measured. This was made by counting the system clock
cycles of the synchronizing circuit routine. The all control
system has a 31.25 µs available processing time, actuating
640 times by grid cycle. The DSP TMS320F2812F system
clock frequency was set at 135MHz. The EPLL
synchronizing circuit takes 2197 system clock cycles, which
corresponds to 16.27 µs. It occupies 52% of the control
system routine available time. The Three-Phase Adapted PLL
takes 1511 system clock cycles, 11.19 µs, which corresponds
to 35.8% of the available processing time.

To evaluate performance characteristics, the Series Active
Conditioner was set to co mpensate the load voltage
distortion. For each proposed algorithm, the load voltage (vL)
presents a 7.9% THD, and a RMS value of 102.2V before
compensation. In Fig. 10 is shown the systems voltages and
currents when the Conditioner starts with the Single-Phase
PLL. vL THD drops to 2.1%, and the RMS value rises to
114.3 V. In Fig. 11 is showed the same transient, being the
EPLL the synchronizing circuit. vL THD drops to 2.1% and
RMS value is of 114.3 V. The two synchronizing circuits
present the same behavior in this transient analysis. In both
cases it can be seen that iS rises, in order to regulate the DC
link voltage.

Another transient was applied to the system. It consisted in
closing contactor C1 (see Fig. 1,) thus connecting the shunt
Also, the compensated load voltage \(v_L\) delivered to the load is in accordance with international standards that regulate harmonic distortion and RMS value. These standards are CEI 61000 and A SI IEEE 519 1992 for harmonics. For RMS value, the standard taken in account is A SI IEEE 519 1992, that describes power quality problems. This was seen on both synchronizing circuits.

Experimental results also showed that the compensated load voltage \(v_L\) delivered to the load is in accordance with international standards that regulate harmonic distortion and RMS value. These standards are CEI 61000 and A SI IEEE 519 1992 for harmonics. For RMS value, the standard taken in account is A SI IEEE 519 1992, that describes power quality problems. This was seen on both synchronizing circuits.

**Fig. 12.** Series Active Conditioner with Single-Phase PLL under the connection of the shunt rectifier. Dot line marks the connection of the rectifier.

**Fig. 13.** Series Active Conditioner with Single-Phase PLL under the connection of the shunt rectifier. Dot line marks the connection of the rectifier.

rectifier to the system, with the series converter turned on. This action would degrade \(v_i\) THD to 8.8%, and the RMS value to 99.7V if there was no compensation. In Fig. 12 can be seen the system voltages and currents when the rectifier is connected with the Conditioner already compensating, with the Single-Phase PLL algorithm. It can be seen that \(v_S\) becomes more distorted, but \(v_L\) maintains a low THD. It is of 1.8% and the RMS voltage is at 115 V. The same values where obtained when the same transient was applied to the system with the Conditioner compensating using the EPLL algorithm. This can be seen in Fig. 13. Since the distortion in \(v_i\) increases, the series converter has to in ect more power in order to compensate it. This forces the shunt power converter of the Conditioner to draw more power to regulate the DC link. Thus, an increased system current \(i_S\) is also observed. Also, the compensated \(v_L\), THD is improved when compared with the first analysis. This is due to the increasing of \(v_{ref}\) that leads to a better modulation index of the series power converter.

**V. CO CL SIO S**

A comparison between to synchronizing circuits for the control algorithm of a Series Active Converter is made in this paper.

The Single-Phase PLL presents higher memory requirements. ut given the vast amount of memory available in the selected microprocessor, this matter has a relative importance. His synchronizing circuit, however, presents higher speed performance. In a real time processing control system, this is an important advantage, since it releases time for other processing routines. In this particular, the Single-Phase PLL can overtake the Enhanced PLL. Even though the EPLL uses less memory resources, its processing time is long. Thus, one can conclude that the Single-Phase PLL is more suited for real time processing systems such as the one presented in this paper.

**REFERENCES**